ON Semiconductor®

# Product Bulletin

Document # : PB22446X
Issue Date: 11 September 2018

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|---|---|
| **Title of Change:** | AR0144CS Datasheet Update. |
| **Effective date:** | 11 September 2018 |
| **Contact information:** | Contact your local ON Semiconductor Sales Office or <Sonya.Yip@onsemi.com> |
| **Type of notification:** | This Product Bulletin is for notification purposes only. ON Semiconductor will proceed with implementation of this change upon publication of this Product Bulletin. |
| **Change Category:** | ☐ Wafer Fab ☐ Assembly Change ☐ Test Change ☑ Other Documentation |

**Change Sub-Category(s):**

☐ Manufacturing Site Addition
☐ Manufacturing Site Transfer
☐ Manufacturing Process Change
☐ Material Change
☐ Product specific change
☑ Datasheet/Product Doc change
☐ Shipping/Packaging/Marking
☐ Other: _____

| | | |
|---|---|---|
| **Sites Affected:** | ON Semiconductor Sites:<br>None | External Foundry/Subcon Sites:<br>None |

**Description and Purpose:**

AR0144CS Datasheet was updated with new information. These changes do not affect form, fit, or function of the product.

**AR0144CS Datasheet Changes**

**1. Updated Table 1, Key Performance Parameters. Added MIPI 1-lane to "Output" and added MIPI 1-lane 10 and 12-bit frame rates to "Frame Rate".**

**Old Table 1:**

Table 1. KEY PERFORMANCE PARAMETERS

| Parameter | Typical Value |
|---|---|
| Optical Format | 1/4-inch (4.5 mm) |
| Active Pixels | 1280 (H) × 800 (V) = 1.0 Mp |
| Pixel Size | 3.0 μm |
| Color Filter Array | RGB Bayer or Monochrome |
| Chief Ray Angle | 0 or 20° or 28° |
| Shutter Type | Global Shutter |
| Input Clock Range | 6–48 MHz |
| Output Pixel Clock (Maximum) | 74.25 MHz |
| Output<br>Serial<br>Parallel | <br>MIPI, 2-lane<br>12-bit |
| Frame Rate<br>Full Resolution<br>720p | <br>60 fps<br>66 fps |
| Responsivity<br>Monochrome<br>Color | <br>56 Ke/lux*s<br>22.3 ke–/lux*s |
| $SNR_{MAX}$ | 38 dB |
| Dynamic Range | 71.4 dB |
| Supply Voltage<br>I/O<br>Digital<br>Analog | <br>1.8 or 2.8 V<br>1.2 V<br>2.8 V |
| Power Consumption | < 215 mW |
| Operating Temperature | –40°C to + 85°C (Ambient)<br>–40°C to + 105°C (Junction) |
| Package Options | 5.6 × 5.6 mm 69-ball CSP |
| | Bare Die |

**New Table:**

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|---|---|
| Optical Format | 1/4-inch (4.5 mm) |
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| Input Clock Range | 6–48 MHz |
| Output Pixel Clock (Maximum) | 74.25 MHz |
| Output<br>Serial<br>Parallel | <br>MIPI, 1–lane or 2–lane<br>12-bit |
| Frame Rate<br>Full Resolution<br><br><br>720p | <br>60 fps (Parallel, MIPI 2–lane, 12–bit)<br>44 fps (MIPI 1–lane, 12–bit)<br>52 fps (MIPI 1–lane, 10–bit)<br><br>66 fps (Parallel, MIPI 2–lane, 12–bit) |
| Responsivity<br>Monochrome<br>Color | <br>56 Ke/lux*s<br>22.3 ke–/lux*s |
| $SNR_{MAX}$ | 38 dB |
| Dynamic Range | 71.4 dB |
| Supply Voltage<br>I/O<br>Digital<br>Analog | <br>1.8 or 2.8 V<br>1.2 V<br>2.8 V |
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**2. In Features Overview "MIPI", added one lane**

**Old Features Section:**

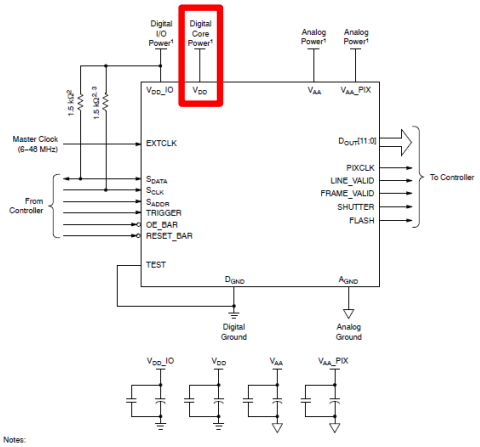
- MIPI
  The AR0144CS Global Shutter image sensor supports two lanes of MIPI data. Compliant to MIPI standards:
  - MIPI Alliance Standard for CSI–2 version 1.2
  - MIPI Alliance Standard for D–PHY version 1.0

**New Features Section:**

- MIPI
  The AR0144CS Global Shutter image sensor supports one or two lanes of MIPI data. Compliant to MIPI standards:
  - MIPI Alliance Standard for CSI–2 version 1.2
  - MIPI Alliance Standard for D–PHY version 1.0

**3. Updated Figure 6, "Parallel Pixel Data Interface".**

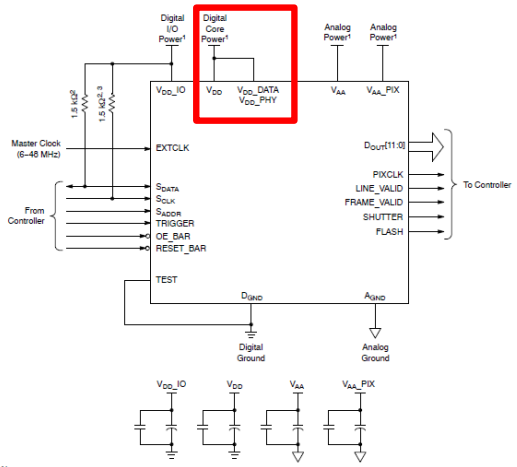
**Old Figure:**




Notes:
1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on $S_{CLK}$ at all times.
4. The serial interface output pads can be left unconnected if the parallel output interface is used.
5. ON Semiconductor recommends that 0.1 µF and 10 µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on the layout and design considerations. Refer to the AR0144CS demo head-board schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.

Figure 6. Parallel Pixel Data Interface

**New Figure:**




Notes:
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Figure 6. Parallel Pixel Data Interface

**3. Updated VDD_PHY Pin Description in Table 3, "Pin Descriptions- 69 Ball CSP Package**

**Old Description:**

| | | | |
|---|---|---|---|
| $V_{DD_PHY}$ | C5 | Power | MIPI power (may leave unconnected if parallel interface is used) |

**New Description:**

| | | | |
|---|---|---|---|
| $V_{DD_PHY}$ | C5 | Power | MIPI power supply (1.2 V) |

**List of Affected Parts:**

AR0144CSSC00SUKA0-CPBR
AR0144CSSC00SUKA0-CRBR
AR0144CSSM00SUKA0-CPBR
AR0144CSSM00SUKA0-CRBR
AR0144CSSC20SUKA0-CPBR
AR0144CSSC20SUKA0-CRBR
AR0144CSSM20SUKA0-CPBR
AR0144CSSM20SUKA0-CRBR
AR0144CSSC00SUD20
AR0144CSSC20SUD20
AR0144CSSM00SUD20
AR0144CSSM20SUD20
AR0144CSSM28SUD20

## Appendix A: Changed Products

| Product | Customer Part Number |
|---|---|
| AR0144CSSC00SUKA0-CPBR | |
| AR0144CSSC00SUKA0-CRBR | |
| AR0144CSSC20SUKA0-CPBR | |
| AR0144CSSC20SUKA0-CRBR | |
| AR0144CSSM00SUKA0-CPBR | |
| AR0144CSSM00SUKA0-CRBR | |
| AR0144CSSM20SUKA0-CPBR | |
| AR0144CSSM20SUKA0-CRBR | |