ISL29501

Time of Flight (ToF) Signal Processing IC

FN8681
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the ISL29501 is a Time of Flight (ToF) based signal processing integrated circuit. The sensor enables low cost, low power, and long range optical distance sensing when combined with an external emitter and detector.

The ISL29501 has a built-in current DAC circuit that drives an external LED or laser. The modulated light from the emitter is reflected off the target and is received by the photodiode. The photodiode then converts the returned signal into current, which is used by the ISL29501 for signal processing.

An on-chip Digital Signal Processor (DSP) calculates the time of flight, which is proportional to the target distance. The ISL29501 is equipped with an I^2C interface for configuration and control.

Use of an external photodiode and emitter allows the user to optimize the system design for performance, power consumption, and distance measurement range that suit their industrial design.

The ISL29501 is wavelength agnostic and permits the use of other optical wavelengths if better suited for applications.

Related Literature

- For a full list of related documents, visit our website
  - ISL29501 product page

Features

- Enables proximity detection and distance measurement
- Modulation frequency of 4.5MHz
- Emitter DAC with programmable current up to 255mA
- Operates in Continuous and Single Shot mode
- On-chip active ambient light rejection
- Auto gain control mechanism
- Interrupt controller
- Supply voltage range of 2.7V to 3.3V
- I^2C interface supporting 1.8V and 3.3V bus
- Low profile 24 Ld 4x5 QFN package

Applications

- Mobile consumer applications
- Industrial proximity sensing
- Power management
- Home automation

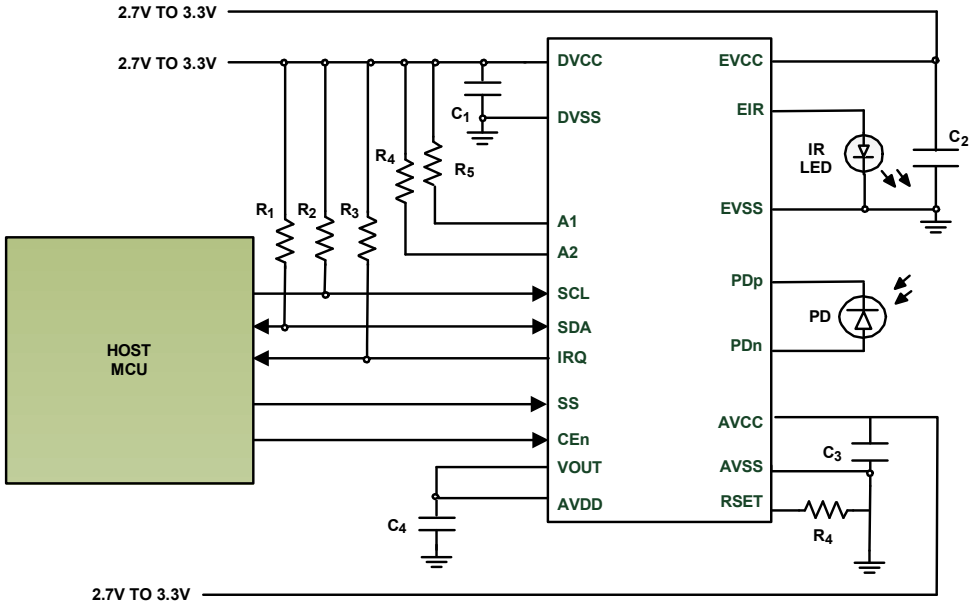


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Block Diagram

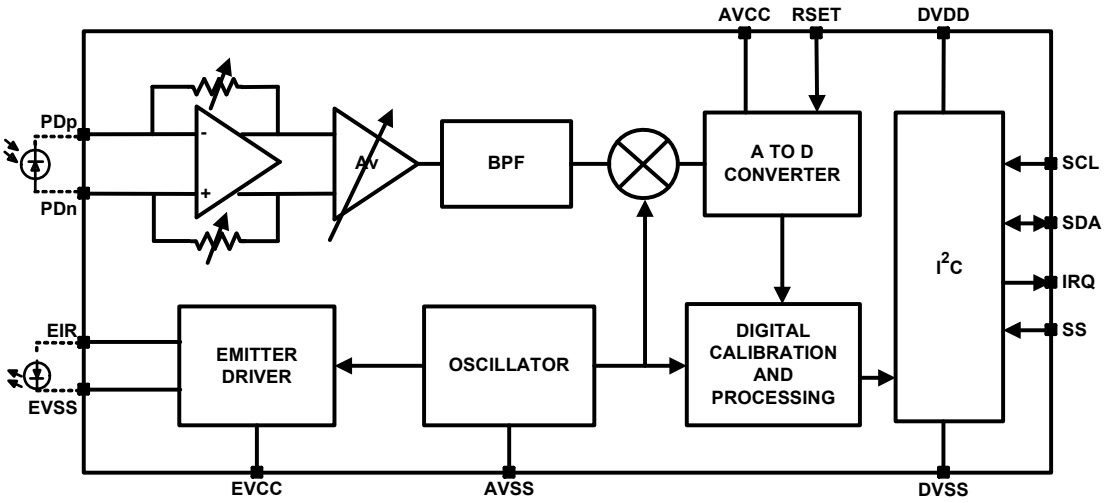


FIGURE 2. BLOCK DIAGRAM

Ordering Information

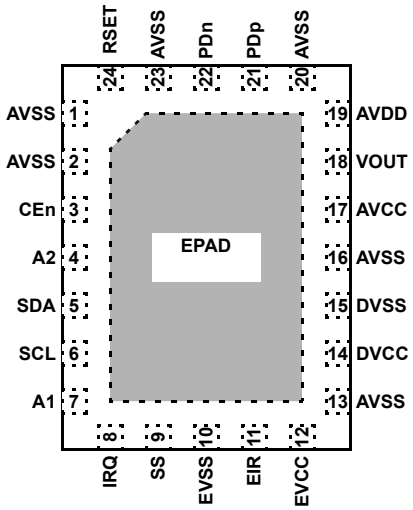
PART NUMBER (Notes 1, 2, 3)	PART MARKING	V_{DD} RANGE (V)	TEMP RANGE (°C)	TAPE AND REEL (UNITS)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL29501IRZ-T7	29501 IRZ	2.7V to 3.3V	-40 to +85	1k	24 Ld QFN	L24.4x5F
ISL29501IRZ-T7A	29501 IRZ	2.7V to 3.3V	-40 to +85	250	24 Ld QFN	L24.4x5F
ISL29501-ST-EV1Z	Sand Tiger Evaluation Board					
ISL29501-CS-EVKIT1Z	Cat Shark Evaluation Board					

NOTES:

1. Refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see device information page for ISL29501. For more information on MSL, see techbrief TB477.

Pin Configuration

ISL29501
(24 LD QFN)
TOP VIEW



Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
1, 2, 13	AVSS	Tie to AVSS
3	CEn	Chip enable, active low
4	A2	I^2C address bit, pull to DVCC or DVSS.
5	SDA	I^2C data bus
6	SCL	I^2C clock bus
7	A1	I^2C ID address bit, pull to DVCC or DVSS.
8	IRQ	Interrupt, active low, open-drain output signal to host. A 2.7kΩ pull-up to supply is required.
9	SS	Sample start: input signal with HIGH to LOW edge active.
10	EVSS	Emitter driver ground. Connects to cathode of emitter.
11	EIR	Emitter driver output. Connects to anode of emitter.
12	EVCC	Emitter driver supply. Decouple with 2.2µF or larger capacitor along with a 0.1µF for high frequency.
14	DVCC	Digital power 2.7V to 3.3V supply
15	DVSS	Digital power ground
16	AVSS	Analog power ground
17	AVCC	Analog power 2.7 to 3.3V supply
18	VOUT	AFE LDO output, tied to AVDD, decouple with 1µF and 0.01µF capacitor pair.
19	AVDD	AFE analog supply
20, 23	AVSS	Analog ground shield
21	PDp	Photodiode cathode input
22	PDn	Photodiode anode input
24	RSET	Sets chip bias current. Tie to 10kΩ resistor 1% to AVSS ground.
	EPAD	Center EPAD: Tied to AVSS

Absolute Maximum Ratings

Supply Voltage Range . . . . . -0.2V to 4V
Voltage on All Other Pins . . . . . (-0.3V to V_{CC}) + 0.3V
ESD Rating
Human Body Model (Tested per JESD22-A114E) (Note 6) 2kV
Machine Model (Tested per JESD22-A115-A) 200V
Latch-Up (Tested per JESD-78C; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 4, 5)	35	1.2

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Temperature . . . . . -40°C to +85°C
Supply Voltage . . . . . 2.7V to 3.3V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
6. ESD HBM passed 2kV with exception to pins IRQ and SDA, which passed 1kV.

Electrical Specifications

Unless otherwise indicated, all the following tables are at DVCC, AVCC, and EVCC at 3V, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
SENSOR PARAMETERS						
Modulation Frequency	f_{mod}	Modulation frequency of emitter	**4.45**	4.5	**4.65**	MHz
Chip Power Supply	DVCC, AVCC, EVCC		**2.7**	3.0	3.3	V
Delay from Chip Enable to First Sample	tcen_fs	Note 7		500		µs
Delay between Sleep Mode to Start of First Sample	tsleep_fs	Note 7			**3**	µs
Quiescent Current - Sleep Mode, DVCC+AVCC+EVCC	I_{S-HS}	CEn = 1; I^2C disable; register values are retained; SS = SDA = SCL = V_{CC}			**2.5**	µA
Quiescent Current - Shutdown, DVCC+AVCC+EVCC	I_{S-SD}	CEn = 0; I^2C enable; register values are retained; all other functions are disabled			**1**	µA
Chip Current While Measuring, DVCC+AVCC+EVCC	IDDact	Emitter duty cycle = 50%, 0x90 = 06h, 0x91 = 00h		55		mA
AFE SPECIFICATIONS						
Maximum AFE Input Current PDp/PDn	Imax_PD	Design recommendation		12.8		µA
Voltage at PDp	VPDp			1.7		V
Voltage at PDn	VPDn			0.75		V
Low Noise Amplifier	LNA	Provides unity gain		1x		N/A
Differential I to V Conversion Range	TIA Gain	0x97[0:1], b0 = 0 and b1 = 0 default		8k		kΩ
Maximum Photodiode Capacitance Recommended	Cmax	Design recommendation			15	pF

I^2C Electrical Specifications

For SCL, SDA, A1, A2, and IRQ. UNLESS otherwise stated, V_{DD} = 3V, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP (Note 9)	MAX (Note 8)	UNIT
Supply Voltage Range for I^2C Specification	V_{I2C}		**1.8**		**3.3**	V
Input Leakage	I_{IL}	V_{IN} = GND to V_{CC}			**1**	µA
Input LOW Voltage	V_{IL}		**-0.3**		**0.3 x V_{CC}**	V
Input HIGH Voltage	V_{IH}		**0.7 x V_{CC}**		**V_{CC} + 0.3**	V
SDA and SCL Input Buffer Hysteresis	Vhys		**0.05 x V_{CC}**			V
SDA Output Buffer low Voltage	V_{OL}	I_{OL} = 3mA	**0**		**0.4**	V
Pin Capacitance (Note 10)	C_{pin}			10		pF
SCL Frequency	f_{SCL}				**400**	kHz
Pulse Width Suppression Time At SDA and SCL Inputs	t_{sp}	Any pulse narrower than the maximum specification is suppressed			**50**	ns
SCL Falling Edge to SDA Output Data Valid	t_{AA}	SCL falling edge crossing 30% of V_{CC} until SDA exits the 30% to 70% of V_{CC} window			**900**	ns
Time the Bus Must Be Free Before the Start of a New Transmission	t_{BUF}	SDA crossing 70% of V_{CC} during a STOP condition to SDA crossing 70% of V_{CC} during the following START condition	**1300**			ns
Clock Low Time	t_{LOW}	Measured at the 30% of V_{CC} crossing	**1300**			ns
Clock High Time	t_{HIGH}	Measured at the 70% of V_{CC} crossing	**600**			ns
START Condition Set-Up Time	$t_{SU:STA}$	SCL rising edge to SDA falling edge; both crossing 70% of V_{CC}	**600**			ns
START Condition Hold Time	$t_{HD:STA}$	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}	**600**			ns
Input Data Set-Up Time	$t_{SU:DAT}$	From SDA exiting the 30% to 70% of V_{CC} window to SCL rising edge crossing 30% of V_{CC}	**100**			ns
Input Data Hold Time	$t_{HD:DAT}$	From SCL rising edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window	**0**			ns
STOP Condition Set-Up Time	$t_{SU:STO}$	From SCL rising edge crossing 70% of V_{CC} to SDA rising edge crossing 30% of V_{CC}	**600**			ns
STOP Condition Hold Time for Read or Volatile Only Write	$t_{HD:STO}$	From SDA rising edge to SCL falling edge; both crossing 70% of V_{CC}	**1300**			ns
Output Data Hold Time	t_{DH}	From SCL falling edge crossing 30% of V_{CC} until SDA enters the 30% to 70% of V_{CC} window	**0**			ns
SDA and SCL Rise Time	t_R	From 30% to 70% of V_{CC}	**20 + 0.1 x cb**		**250**	ns
SDA and SCL Fall Time	t_F	From 70% to 30% of V_{CC}	**20 + 0.1 x cb**		**250**	ns
Capacitive Loading of SDA or SCL	Cb	Total on-chip and off-chip	**10**		**400**	pF
SDA and SCL Bus Pull-Up Resistor Off-Chip	Rpu	Maximum is determined by t_R and t_F For Cb = 400pF, maximum is about 2kΩ ~ 2.5kΩ For Cb = 40pF, maximum is about 15kΩ ~ 20kΩ	**1**			kΩ
Output Leakage Current (SDA only)	I_{LO}	V_{OUT} = GND to V_{CC}			**1**	µA
A1, A2, SDA, and SCL Input Buffer low Voltage	V_{IL}		**-0.3**		**V_{CC} x 0.3**	V
A1, A2, SDA, and SCL Input Buffer high Voltage	V_{IH}		**V_{CC} x 0.7**		**V_{CC}**	V

I²C Electrical Specifications

For SCL, SDA, A1, A2, and IRQ. UNLESS otherwise stated, V_{DD} = 3V, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP (Note 9)	MAX (Note 8)	UNIT
SDA Output Buffer LOW Voltage	V_{OL}		**0**		**0.4**	V
Capacitive Loading of SDA or SCL	C_L		**10**		**400**	pF

NOTES:

7. Product characterization data.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. Typical values are for T_A = +25°C and V_{CC} = 3.3V.
10. Cb = total capacitance of one bus line in pF.

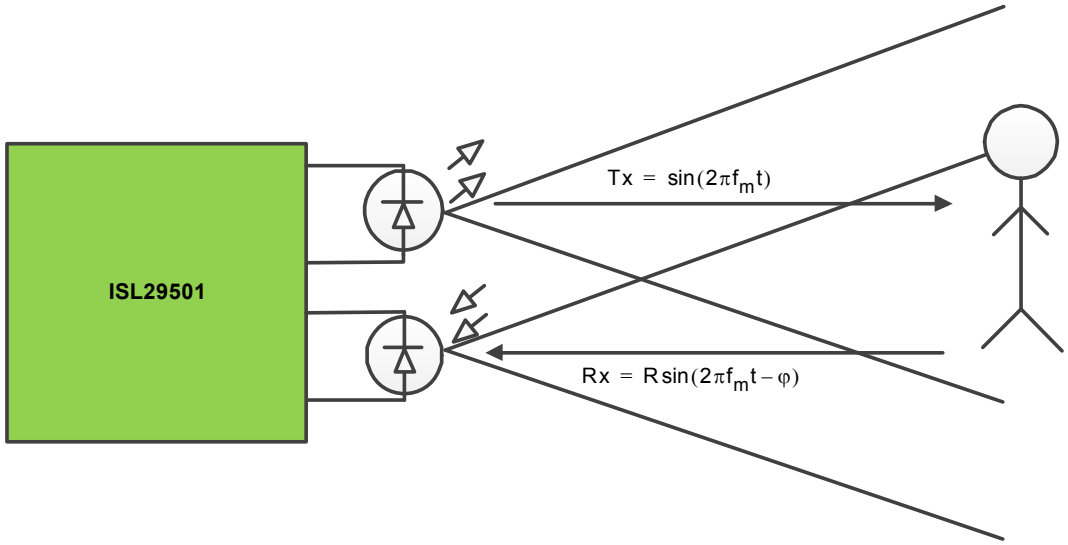


FIGURE 3. TRANSMITTED AND RECEIVED SIGNAL IN A SYSTEM

Principles of Operation

The ISL29501 operates using the principle of Square Wave Modulated Indirect Time of Flight (SWM-ITOF). The sensor operates in frequency domain and takes advantage of the analog signal processing techniques to obtain distance measurements from phase shift.

The ISL29501 IC partnered with an external emitter and detector functions as a distance and ranging sensor.

The chip emitter driver transmits a modulated square wave (Tx) at a given frequency optical signal (f_{mod}) through the emitter, the received optical signal (Rx) returns with phase shift and attenuation dependent on object distance and reflectivity (see Figure 3 on page 7).

The phase difference between emitted and received signals of the modulated square wave is determined in frequency domain and is converted to a distance measurement.

The distance is computed using an internal DSP with the results provided to the host through an I^2C interface.

The phase shift of the return signal is dependent on the distance of the object from the system and is relatively independent from the object reflectivity.

The distance of the object can be calculated by determining the phase shift of the return signal using Equation 1.

$$D = \frac{C}{4\pi f_{mod}}\Delta\varphi \quad \text{(EQ. 1)}$$

where:

D is the distance of the object from the sensor system.

f_{mod} is the modulation frequency.

$\Delta\varphi$ is the phase difference between emitted and return signals.

C is the speed of light.

Key constants can be derived from this expression for f_{mod} = 4.5MHz (the system frequency) whose values can be useful in developing a general understanding of the system.

- 5.3m/radian
- 33.3m for cycle (2π radians)
- 15cm/ns delay

The range of the system can be optimized for each application by selecting different components (emitter, detector) and optics.

The sensor takes advantage of analog quadrature signal processing techniques to obtain the phase difference between the emitted and received signals. Some of the processing steps in the signal chain are listed in the following paragraph.

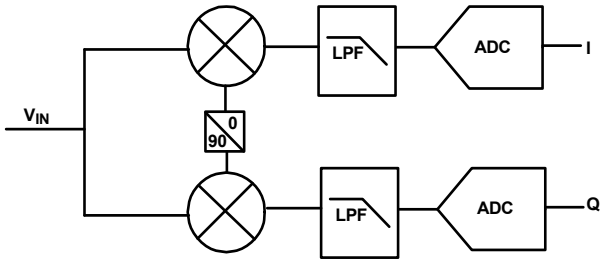


FIGURE 4. I AND Q PROCESSING OF THE SIGNAL

The Analog Front End (AFE) converts the photocurrent into a voltage, which it does in two stages. The first stage is a Transimpedance Amplifier (TIA), which converts the photodiode current into voltage. The second stage is a Low Noise Amplifer (LNA) that buffers this voltage for rest of the analog signal chain. The demodulator translates this signal into In phase (I) and Quadrature (Q) components.

I and Q values are filtered and then digitized by the ADC. The DSP calculates the distance based on the amplitude, phase, and frequency values.

The AFE in conjunction with the gain from the AGC loop allows for selection of different detectors in application design. The ADC relies on the automatic gain control loop to evaluate the optimal setting for data conversion. This prevents saturation when the target is at short range.

Functional Overview

The following paragraphs provide additional detail to the function of the important blocks in the ISL29501. Additional information may be available in the related documentation.

Power Supply Pins

The ISL29501 will operate with a voltage range from 2.7V to 3.3V. There are three power rails: AVCC, DVCC, and EVCC. The AVCC and DVCC supply the digital and analog part of circuits and the EVCC is dedicated to the emitter driver section.

Intersil recommends decoupling the analog and digital supplies to minimize supply noise. Noise can be random or deterministic in nature. Random noise is decoupled like in any other system. Synchronous noise (4.5MHz) is seen as crosstalk by the chip and directly affects distance measurements. Crosstalk calibration will mitigate this effect but it is better to target this frequency directly, particularly on EVCC.

Power-On Reset

When power is first applied to the DVCC pin, the ISL29501 generates an internal reset. The reset forces all registers to their default values and sets the sequencer to an initial state.

Chip Enable (CEn) Pin

The CEn pin is an active low input pin. When asserted (pulled low), the device will bias the internal circuit blocks, band gaps, references, and I^2C interface. When CEn is enabled, writing 0x01 b0 = '1' will disable the chip. It can be re-enabled by writing it back to '0' providing CEn stays low. This allows software control. Register 0x01 defaults to 0 or enabled.

Changing the chip enable does not alter register values.

Sample Start (SS) Pin

The Sample Start (SS) pin is an input logic signal, which triggers a measurement cycle. This signal is needed to start measurements in Free Run mode and for each measurement in Single Shot mode.

If a trigger is received during an active measurement, the request is ignored.

Command Register

The Command Register (0xB0) allows the user to operate under software control. There are three commands that each perform useful functions without hardware interaction.

- A soft-start can be initiated by writing 0xB0 to 0x49. This register bit emulates the single shot pin and acts like the SS pin to start measurements.
- A soft-reset can be initiated by writing 0xB0 to 0xD7. This action resets all registers to power-on default values with the exception of brownout bit. This function performs similarly to the power cycle.
- A soft-clear can be initiated by writing to 0xB0 to 0xD1, which stops all conversions and resets the accumulators. The sensor will stop if it is in Continuous mode. This function is a sequencer reset.

Interrupt (IRQ) Pin

The ISL29501 can be configured to generate interrupts at the completion of a sensing cycle. These interrupts allow the host to perform other tasks while a measurement is running.

The IRQ pin is an active low output logic pin. It is an open-drain output pin and requires a pull-up resistor to DVCC.

The host should service the IRQ request by reading the 0x60 register. The register is cleared upon reading (self clear). If the sensor is set to signal sample mode, then the sensing stops and awaits for the next sample start signal.

If the ISL29501 is set to Continuous mode, then the IC will begin the next sensing sample according to the preconfigured sampling time period.

Sampling Modes

The ISL29501 provides two operating sample modes: Single Shot mode and Continuous mode.

TABLE 1. Reg0x13 SAMPLING MODES

REGISTER	BIT PREFERENCE	MODE OF OPERATION
0x13[0]	0	Continuous sampling
0x13[0]	1	Single shot sampling

Single Shot

In Single Shot mode, one measurement is made. The sampling period is normally not important since the MCU is controlling each measurement. The duration of the measurement is controlled by the integration time and the MCU latency, which allows the greatest flexibility of the measurement duty cycle and therefore, the power consumption.

Continuous Mode

Continuous mode operation is used for systems where the sensor is continuously gathering data at a predefined integration and sampling period using the internal timing controller. This is the chip default.

The data is available to the host after every sample period and the sensor will keep operating in this mode until changed by the MCU. If the interrupt is enabled, the IRQ pin will toggle after each measurement.

By adjusting the sample period and the sample period range (Registers 0x11 and 0x12), a latency of 3.5 seconds between measurements is possible. For greater measurement intervals, Single Shot mode must be used.

Emitter Driver

Integrated in the ISL29501 is an emitter driver circuit. It is a current source designed to drive either the IR LED or laser. The circuit is enhanced to provide fast turn-on and turn-off of either LED or lasers. The driver needs about 1V of headroom to operate properly. It will still operate with lower voltages but the driver becomes less linear the lower you go. Headroom is defined as the voltage across the driver EVDD - $V_{forward\ emitter}$. This may limit the optical power of certain lasers.

EIR Pin

Figure 5 on page 10 shows a simplified block diagram of the emitter driver. The circuit consists of two primary current DACs, main and threshold DAC.

The EIR pin is connected to the emitter anode while the cathode is tied to ground (EVSS).

The drive current is derived from a combination of range (0x90) and value (0x91) DACs allowing a wide range of values.

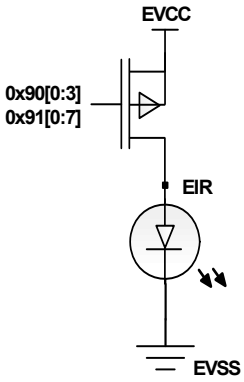


FIGURE 5. EMITTER CONNECTIVITY

Main DAC

The main DAC is implemented in two separate DACs. Combined they are designed to output a maximum current of 255mA of switched (pulsed) current. The current value is set by programming Registers 0x90 and 0x91. Register 0x90 is the range control and Register 0x91 for fine control.

Depending on the application's desired range and the type of emitter employed, the current level can be set to give the best SNR performance. The system designer will have to determine this value based on component selection. In addition, this fine tuning allows the application to compensate for production variation in the external components.

The emitter current is governed by the following formula:

$I_{Emitter}$ ~ = 0x90[3:0]/15*0x91[7:0]/255*255mA

Threshold DAC

In addition to the main DAC, there is a threshold DAC that can provide DC current to the emitter. This might be useful in some laser applications by raising the off current to just below its threshold. The threshold current is active only during integration time to limit power consumption. Threshold current is not needed in most applications.

A maximum of 30mA can be driven by the threshold DAC. The current is programmed in Register 0x93. The detailed description can be found in the "Register Map" on page 16.

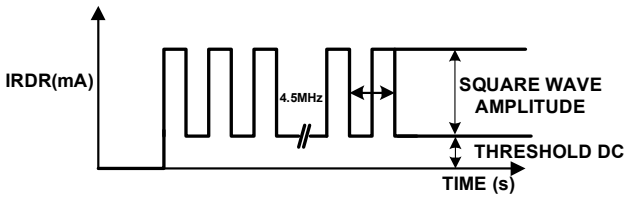


FIGURE 6. TYPICAL EMITTER WAVEFORM AND FEATURES

Connecting the Photodiode

The photodiode should be connected between the PDn and PDp pins as shown in Figure 7. The photodiode operates in photoconductive mode. The voltages at PDp and PDn nodes are listed in the AFE specifications. The photodiode is reverse biased with anode at 0.7V and the cathode at 1.7V (1V reverse bias). Biasing the diode in photoconductive mode enables lower effective capacitance/faster operation and efficient collection of photo energy.

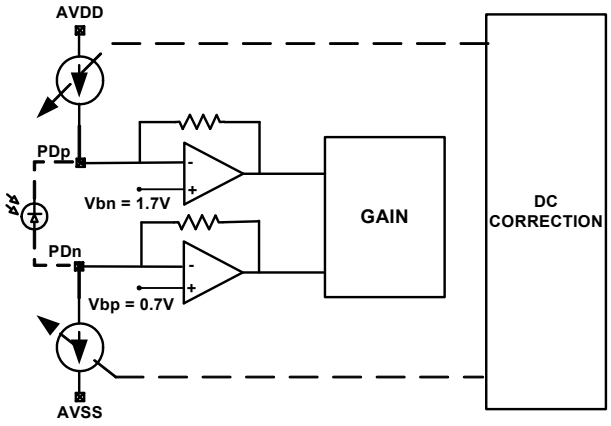


FIGURE 7. CONNECTING PD TO AFE

Selecting the Photodiode

This section provides general guidelines for the selection of the photodiode for receiver.

Three key parameters that must be considered:

1. Peak wavelength
2. Collected light
3. Rise/fall time

A detector with narrow band sensitivity in the NIR or MWIR are best for proximity sensing as most ambient light will be naturally rejected. The ideal PD would be a narrow band pass that is centered on the emitter peak wavelength. Diodes with no filter offer poor performance and should not be considered.

The user must ensure that the emitter peak wavelength is aligned with the detector wavelength to achieve high SNR.

Maximizing the collected light can be achieved with the largest active area the mechanical constraints allow or through the use of a lens. PDs in a traditional LED package have a built-in lens so the effective active area can be 20 times more than the silicon area would suggest.

Large area diodes are accompanied with larger intrinsic capacitances leading to slow rise and fall times. There is a trade-off between detector area and capacitance that need to be considered for system performance.

The fully differential front-end converts the photo current into voltage and allows for common-mode noise/crosstalk to be rejected.

An effective capacitance of less than 15pF is recommended for robust performance, in applications where distance measurement is required. Using larger capacitance will cause increase in noise and not functional failure. The decision to use a small or large photodiode (i.e., capacitance) has to be made by the system engineer based on the application.

Emitter Selection

The ISL29501 supports the use of light sources such as LEDs, VCSELS, and lasers. The sensor will drive any emitter within the maximum current range supported by the emitter DAC.

The sensor working principle is wavelength agnostic and determination of wavelength can be made based on application.

The emitter wavelength should be an NIR or MWIR (i.e., 800nm to 1300nm) to minimize the influence of ambient light on the precision.

The selection between an LED or laser depends on the user application. Some general system considerations are distance, field of view, and precision requirements. While an LED is a reliable light source, it might not be the best suited for long distance due to its dispersion characteristics. However, it is good for short range and large area coverage. For higher optical power, lasers/VCSEL may offer an advantage.

Lasers are more efficient but are more complicated to implement due to eye safety requirements and higher forward voltages.

Ambient Light Rejection

Ambient light results in a DC current in the TIA.

A feedback loop negates this current to prevent impact to the signal path. Subsequent stages of the analog signal chain are AC coupled and are not susceptible to DC shifts at AFE.

Ambient light will alter the photon to current delay in the photodiode. This is not an issue if the ambient light is constant, but it is if it changes. A delay in the photodiode due to ambient light changes directly translates into distance error.

To minimize the effect of ambient light on the system distance measurements, the sensor enables correction algorithms (linear and second order polynomial to correct for any diode related behaviors). After coefficients are determined and programmed, the ambient induced delay (distance error) is subtracted in real time in the chip DSP.

The ambient current value can be found by reading Register 0xE3.

Power Consumption

In a Time of Flight (TOF) application, power consumption has two components: the power consumed within the ISL29501 device and the power consumed by the emitter LED or VSCEL. Although the emitter current is load current and not part of the ISL29501 power dissipation, it is included in this discussion to help the user understand the entire TOF contribution to the total application power budget (see Equation 2).

$$IDD_{ToF} = IDD_{IC} + IDD_{Load} \quad \text{(EQ. 2)}$$

IC POWER CONSUMPTION

The power consumed in the ISL29501 has two components. The first is the standby current, which is present whenever the chip is not integrating (making a measurement). The second is the current consumed during a measurement. Chip current is calculated by multiplying the overall duty cycle by 102mA and adding the standby current (~2mA). The overall duty cycle is defined as (integration time/sampling period/2) in Continuous mode or the (integration time/user measurement repetition rate/2) in single sample mode see Equation 3.

$$IDD_{IC} = 102mA \bullet DC_{Overall} + I_{Standby} \quad \text{(EQ. 3)}$$

Typical values for $I_{Standby}$ can be found in the “Electrical Specification Table” on page 5. Total Time of Flight Power Consumption

To calculate the total TOF module current, the load current contribution must be added to the chip current. As with the chip current, the measurement duty cycle has a large effect on the load current. The load current is defined as the product of the emitter current and the overall measurement duty cycle (see Equation 4).

$$I_{Load} = DC_{Overall} \bullet I_{Emitter} \quad \text{(EQ. 4)}$$

The emitter current is calculated using Equation 5:

$$I_{Emitter} = (reg0x90/15) \bullet (reg0x91/255) \bullet 255mA \quad \text{(EQ. 5)}$$

The duty cycle for this calculation is the same as described in the IC power consumption section. In the application, the best emitter current setting is a balance of the required optical power and the acceptable power consumption. Similarly, the duty cycle is a balance between the precision of a measurement and power consumption. It should be noted that choosing high duty cycles can cause heating of the emitter introducing drift in distance measurements.

For additional details, refer to “Emitter Selection” and “Integration Time” on page 12.

Shutdown

Shutdown disables all the individual components that actively consume power, with the exception of the I^2C interface. There are multiple options for the system designer based on the time to bring up the system.

The CEn (Chip Enable), in conjunction with shutdown, can be used to keep the system passive based on power consumption and speed of response.

Sampling Time

The sampling waveform in Figure 8 on page 12 dictates the sensor operation. The key elements to understand are integration time and sampling interval.

Integration time dictates the driver waveform active period and sampling frequency provides the data output rate of the sensor. Optimal values for integration time and sampling interval (duty cycle) determine the power consumption and performance of the system (precision). A typical emitter driver waveform is shown in Figure 9 on page 12 to indicate the controls that are available to the user.

The sampling interval determines the sensor response time or rate of output from the sensor; this is user-defined with Equation 6:

$$\text{Sampling frequency} = \frac{1}{450\mu s \bullet (1 + \text{sample_period}[7:0] \bullet 2^{\text{sample_skip}[3:0]})} \quad \text{(EQ. 6)}$$

The value for sampling frequency ranges from 1ms to 1843ms. For a more detailed description of the register, refer to the "Register Map" on page 16.

The ratio of integration time to sampling frequency is the sensor duty cycle. Duty cycle determines the power consumption of the sensor.

When building an optical system, a determination of an effective duty cycle will help optimize power and performance trade-offs in the system.

Integration Time

Integration time sets the emitter DAC active time. The value is user controlled by the register interface.

If the sample integration time is set to be greater than the sample period, then the integration time will default to maximum allowable within the sample period.

Integration time impacts precision and power consumption of the chip and can be used as a measure to optimize the system performance.

$$\text{Integration time} = 71.1\mu s \bullet 2^{\text{sample_len}[3:0]} \quad \text{(EQ. 7)}$$

$$\text{Maximum integration time} = 71.1\mu s \bullet 2^{11} \text{ (145.6ms)}$$

For a more detailed description of the register, refer to the "Register Map" on page 16.

Automatic Gain Control

The ISL29501 has an advanced automatic gain control loop, which sets the analog signal levels at an optimum level by controlling programmable gain amplifiers. The internal algorithms determine the criteria for optimal gain.

The goal of the AGC controller is to achieve the best SNR response for the given application.

Ambient Light ADC

The ambient light ADC measures the amount of ambient light present in the sensor environment. Although this does not directly effect the ISL29501 chip, it does introduce changes in the photodiode that will effect distance measurements.

The ambient ADC operation does not interfere with sensor operation. The ambient light magnitude can be read from Register 0xE3[7:0]. This register holds a code proportional to the ambient photocurrent.

The ADC value is used directly when ambient light correction is programmed, no software manipulation is required.

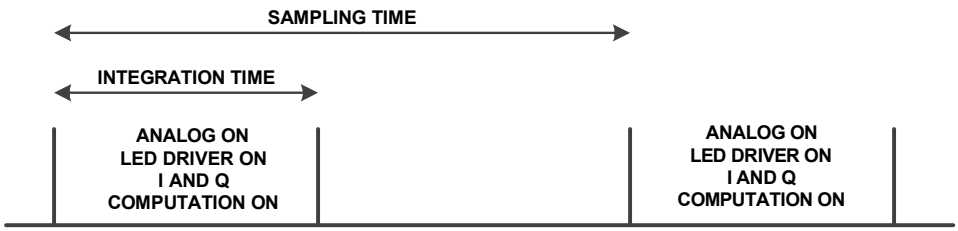


FIGURE 8. WAVEFORM FOR FUNCTIONAL OPERATION

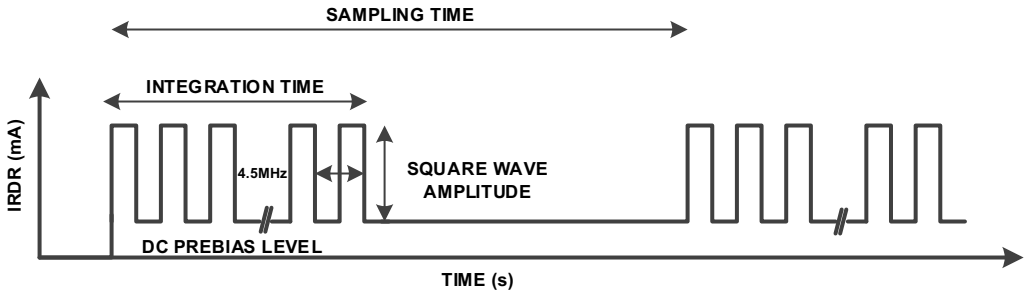


FIGURE 9. EMITTER DRIVER WAVE FORM

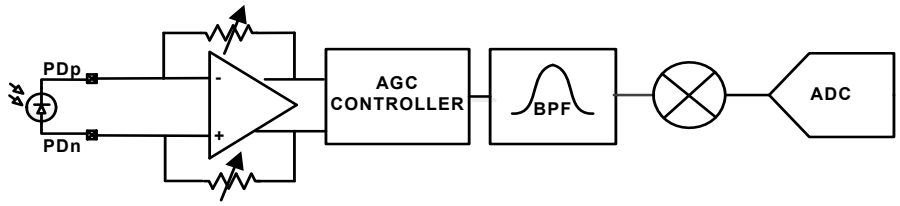


FIGURE 10. AUTOMATIC GAIN CONTROL

Data Outputs

The sensor outputs a wide variety of information that can be used by the MCU for processing. A list of parameters that can be obtained from the sensor are identified in the following.

The information can be relied upon by the digital logic to generate interrupts for quick decision making or used for other off-chip processing functions.

- Distance = (0xD1 * 256 + 0xD2)/65536 * 33.31 (m)
- Precision = (0xD3 * 256 + 0xD4)/65536 * 33.31 (m)
- Magnitude = (0xD6 * 256 + 0xD7) * (2.0 ^ 0xD5)/100000 (nA)
- Phase = (0xD8 * 256 + R0xD9) / 65536 * 2pi (rad)
- Raw I and Q values
- Chip junction temperature
- Emitter forward voltage
- Enable motion computation based on time stamped distance values

Details for these registers are contained in Table 3 on page 19.

Interrupt Controller

The interrupt controller is a useful block in the digital core of the ISL29501. The interrupt controller generates interrupts based on sensor state. This allows the user to free up the MCU to do other tasks while measurements are in progress.

Noise Rejection

Electrical AC power is distributed worldwide at either 50Hz or 60Hz and may interfere with sensor operation. The ISL29501 sensor operation compensates for this interference and rejects these noise sources.

I^2C Serial Interface

The ISL29501 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL29501 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first. This device supports multibyte reads.

Chip Identification (Address)

The ISL29501 has an I^2C base address of 0xA8.

TABLE 2. IDENTIFICATION BYTE FORMAT

1	0	1	0	1	A2	A1	0
(MSB)							(LSB)

A2 and A1 Pins

A2 and A1 are address select pins and can be used to select one of four valid chip addresses. A2 and A1 must be set to their correct logic levels, see I^2C Electrical Specifications on page 6 for details. The LSB Chip Address is the Read/$\overline{\text{Write}}$ bit. The value is “1” for a Read operation, and “0” for a $\overline{\text{Write}}$ operation (see Table 2).

A1 and A2 should be tied to DVSS for default operation.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. The SDA state changes during SCL high are reserved for indicating START and STOP conditions (see Figure 11 on page 14). On power-up of the ISL29501, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL29501 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 11). A START condition is ignored during the power-up sequence.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 11). A STOP condition at the end of a Read operation, or at the end of a Write operation places the device in its standby mode.

An Acknowledge (ACK), is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line low to acknowledge the reception of the eight bits of data (see Figure 12 on page 14).

The ISL29501 responds with an ACK after recognition of a START condition followed by a valid identification (I^2C address) byte. The ISL29501 also responds with an ACK after receiving a data byte of a Write operation. The master must respond with an ACK after receiving a data byte of a Read operation.

Write Operation

A Write operation requires a START condition, followed by a valid identification byte, a valid address byte, a data byte, and a STOP condition. After each of the three bytes, the ISL29501 responds with an ACK.

STOP conditions that terminate Write operations must be sent by the master after sending at least one full data byte and its associated ACK signal. If a STOP byte is issued in the middle of a data byte, or before one full data byte + ACK is sent, then the ISL29501 resets itself without performing the write.

Read Operation

A Read operation is shown in Figure 14 on page 15. It consists of a minimum four bytes: A START followed by the ID byte from the master with the R/$\overline{W}$ bit set to 0, then an ACK followed by a register address byte. The master terminates the Read operation by not responding with an ACK and then issuing a STOP condition. This operation is useful if the master knows the current address and desires to read one or more data bytes.

A random address Read operation consists of a two-byte “write” instruction followed by a register Read operation (see Figure 14). The master performs the following sequence: a START, a chip identification byte with the R/$\overline{W}$ bit set to “0”, a register address byte, a second START and a second chip identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL29501 responds with an ACK. While the master continues to issue the SCL clock, ISL29501 will transmit data bytes as long as the master responds with an ACK with the 9th clock. The register address will automatically increment by one after ACK so the next register’s data will come out with succeeding SCL clocks. The master terminates the Read operation by issuing a STOP condition following the last bit of the last data byte (see Figure 14).

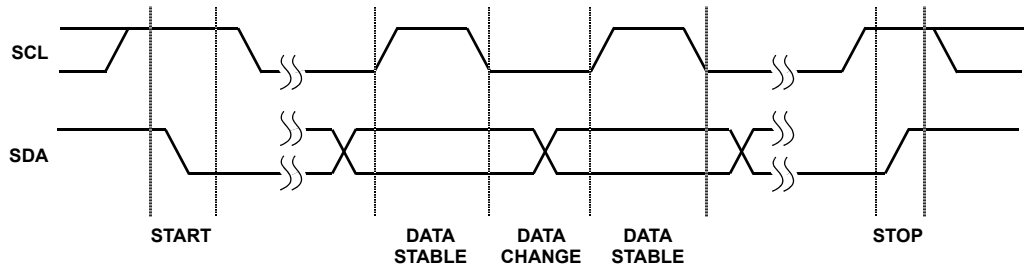


FIGURE 11. VALID DATA CHANGES, START AND STOP CONDITIONS

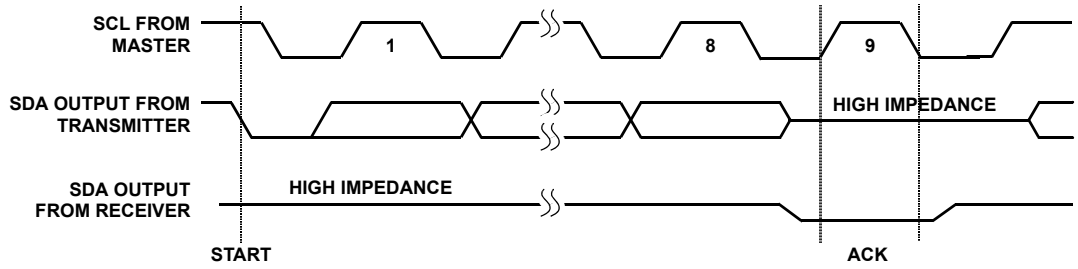


FIGURE 12. ACKNOWLEDGE RESPONSE FROM RECEIVER

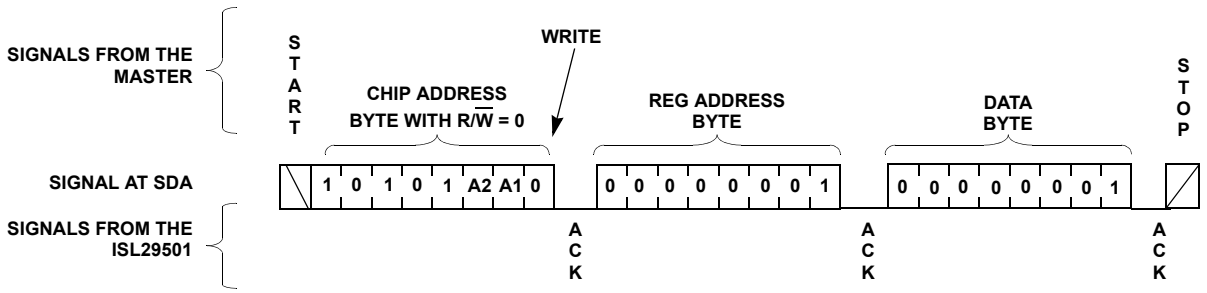


FIGURE 13. EXAMPLE BYTE WRITE SEQUENCE

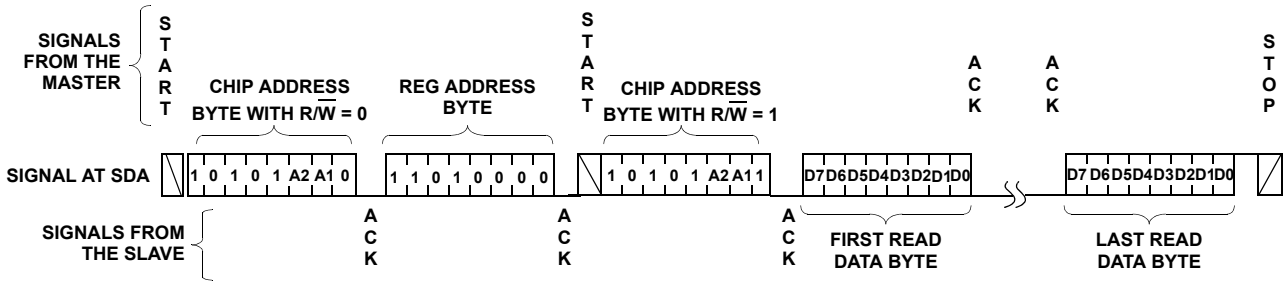


FIGURE 14. MULTIBYTE READ SEQUENCE

Standard Calibration

The goal of standard calibration on the ISL29501 is to compensate sensor performance for production variation in the chip and the optical components as a system. For most applications, these three calibrations must be performed on every board. In a proximity sensing application, accurate distance is not required and it might be possible to use a single set of calibration values for all boards.

There is no nonvolatile memory on the chip, so the user will have to use the I^2C to program calibration register values during initialization every time the board is power cycled.

Crosstalk Calibration

Crosstalk is defined as signal that reaches the ISL29501 chip directly without bouncing off the target. This can be electrical or optical. At close range, a large return signal value crosstalk has a minor impact on distance measurements. At the far end of the distance range, the crosstalk might exceed the signal and add error to measurements. The ISL29501 has the ability to do a real time subtraction of crosstalk from the returned signal resulting in a more accurate measurement. If the crosstalk remains constant, this subtraction is very effective. This is normally a one-time calibration performed at the factory in controlled conditions.

For this calibration, the user makes a distance measurement with the return signal blocked from reaching the photodiode. Since the chip sees none of the emitted signal, anything received is crosstalk. With little to no signal, Gaussian noise will dominate these measurements. To eliminate this noise, the crosstalk measurement needs to be averaged. The averaged value is then written into the chip where it will be subtracted in real time from all succeeding distance measurements.

A detailed description of registers is provided in the "Register Map" on page 16, Registers 0x24 to 0x2b hold the crosstalk calibration values. If these registers remain at default values (0x00), no correction will occur.

Distance Offset Calibration

Variation in delay of emitter types, photodiodes, and circuit board design will change the signal path delay. To compensate for this, a reference point at a known distance needs to be established. This reference is calculated during distance calibration. The process involves making a distance measurement at a known distance, subtracting that distance from a raw measurement, and writing the difference into the distance calibration Registers 0x2F/0x30.

After these calibration registers are written, all succeeding distance will have this value subtracted real time from the measured value. To ensure the correct value is subtracted an average of several measurements needs to be collected. Depending on the emitter and photodiode choice this calibration should be required once per family (emitter/photodiode/board) type.

Optical System Design Considerations

A system designed with the ISL29501 requires that the emitter and detector are optically isolated for better performance. There needs to be a physical barrier or isolation between the emitter and detector to minimize direct optical signal coupling between the emitter and detector.

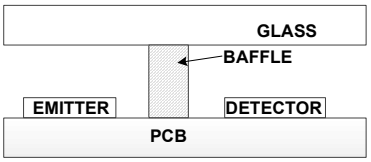


FIGURE 15. SIMPLIFIED OPTICAL SYSTEM

If a glass or other material is placed above the emitter detector, light from the LED can reflect off the glass and enter the sensor. This reflection can limit the range of the proximity measurement and manifests as faint objects in measurements.

Careful attention must be paid to some of the following design parameters:

- Spacing between emitter and detector
- Optical isolation between emitter and detector
- Distance of the PCB from glass or from optical co-package

The ISL29501 architecture rejects most ambient optical interference signals that are lower or higher than the modulation frequency. A review of the ambient sources in the system will help you understand the amount of ambient light and the impacts on the precision measurements.

Register Map

ADDR	REGISTER NAME	ACCESS	DEFAULT	BIT(S)	BIT NAME	FUNCTION	COMMENT
PAGE 0: CONTROL, SETTING, AND STATUS REGISTERS							
0x00	Device ID	RO	0xA	7:0	chip_id[7:0]	Device ID	Default to '0A'
0x01	Master Control	RW	0x00	0	c_en	Chip enable	Same meaning as CEn pin 0: Enabled (default) 1: Disabled
0x02	Status Registers	RO		0	enout	'1' = Output enabled	
				1	ready	'1' = Chip ready	
				2	vdd ok	'1' = Internal power-good	Internal regular output voltage
SECTION 0.1: SAMPLING CONTROL REGISTERS							
0x10	Integration Period	RW	0x02				
			2	3:0	sample_len[3:0] ≅ 71.1µs*$2^{\{sample_len[3:0]\}}$ Maximum = 71.1µs*2^{11} = 145.6ms	Controls the length of each sample, which is equal to the time during which the optical pulse is active.	Sample_len is also called integration time. This value dictates the number of pulses of the 4.5MHz clock on the EIR pin.
0x11	Sample Period	RW	0x00	7:0	sample_period[7:0]	Controls the time between the start of each sample	Sample period = 450µs*(sample_period[7:0]+1)
0x12	Sample Period Range	RW	0x00				
				1:0	sample_skip[1:0]	Sample skipping select	0: Sample period multiplied by 2^0 1: Sample period multiplied by 2^1 2: Sample period multiplied by 2^2 3: Sample period multiplied by 2^3 (default)
0x13	Sample Control	RW	0x7C				
			0	0	adc_mode	Single shot/free running	0: Free running, a single TRIGGER to start is required 1: Single Shot, will only sample off external trigger
			0	1	cali_mode	Calibration vs light order for Single Shot mode	0: Calibration happens before light samples for Single Shot mode 1: Calibration happens after light samples for Single Shot mode
			3	3:2	cali_freq[1:0]	Sets frequency of calibration samples for free running mode	0: Calibration sample after every 16 light samples 1: Calibration sample after every 32 light samples 2: Calibration sample after every 64 light samples 3: Calibration sample after every 128 light samples
			1	4	light_en	Light sample enable	0: Calibration disabled 1: Calibration enabled

Register Map (Continued)

ADDR	REGISTER NAME	ACCESS	DEFAULT	BIT(S)	BIT NAME	FUNCTION	COMMENT
0x19	AGC Control	RW	0x22				
				2	min_vga1_exp[2:0]	Set VGA1 minimum	Set minimum allowed value of VGA1
				4	min_vga2_exp[2:0]	Set VGA2 minimum	Set minimum allowed value of VGA2
SECTION 0.4A: CLOSED LOOP CALIBRATION REGISTERS							
0x24	Crosstalk I Exponent	RW	0x00	7:0	i_xtalk_exp[7:0]	Crosstalk I channel exponent	Unsigned 8-bit exponent
0x25	Crosstalk I MSB	RW	0x00	7:0	i_xtalk[15:8]	Crosstalk I channel MSB	Signed 16-bit mantissa
0x26	Crosstalk I LSB	RW	0x00	7:0	i_xtalk[7:0]	Crosstalk I channel LSB	
0x27	Crosstalk Q Exponent	RW	0x00	7:0	q_xtalk_exp[15:8]	Crosstalk Q channel exponent	Unsigned 8-bit exponent
0x28	Crosstalk Q MSB	RW	0x00	7:0	q_xtalk[15:8]	Crosstalk Q channel MSB	Signed 16-bit mantissa
0x29	Crosstalk Q LSB	RW	0x00	7:0	q_xtalk[7:0]	Crosstalk Q channel LSB	
0x2A	Crosstalk Gain MSB	RW	0xFF	7:0	gain_xtalk[15:8]	Crosstalk gain MSB	Unsigned 16-bit integer
0x2B	Crosstalk Gain LSB	RW	0x00	7:0	gain_xtalk[7:0]	Crosstalk gain LSB	
0x2C	Magnitude Reference Exp	RW	0x00	3:0	mag_ref_exp[3:0]	Magnitude reference exponent	Unsigned 4-bit exponent
0x2D	Magnitude Reference MSB	RW	0x00	7:0	mag_ref[15:8]	Magnitude reference significant	Unsigned 16-bit integer
0x2E	Magnitude Reference LSB	RW	0x01	7:0	mag_ref[7:0]		
0x2F	Phase Offset MSB	RW	0x00	7:0	phase_offset[15:8]	Fixed distance offset calibration MSB	Unsigned 16-bit integer
0x30	Phase Offset LSB	RW	0x00	7:0	phase_offset[7:0]	Fixed distance offset calibration LSB	
SECTION 0.4B: AMBIENT LIGHT AND TEMPERATURE CORRECTIONS							
0x31	Temperature Reference	RW	0x00	7:0	ol_temp_ref[7:0]	Temperature reference	Reference for temperature correction
0x33	Phase Exponent	RW	0x00	3:0	ol_phase_co_exp[3:0]‘	Correction exponent	Unsigned 4-bit exponent for all corrections
0x34	Phase Temperature B	RW	0x00	7:0	ol_phase_temp_B[7:0]	Temperature correction coefficient B	Equation format Ax^2+Bx+C
0x36	Phase Ambient B	RW	0x00	7:0	ol_phase_amb_B[7:0]	Ambient correction coefficient B	Equation format Ax^2+Bx+C
0x39	Phase Temperature A	RW	0x00	7:0	ol_phase_temp_A[7:0]	Temperature correction coefficient A	Equation format Ax^2+Bx+C
0X3B	Phase Ambient A	RW	0x00	7:0	ol_phase_amb_A[7:0]	Ambient correction coefficient A	Equation format Ax^2+Bx+C

Register Map (Continued)

ADDR	REGISTER NAME	ACCESS	DEFAULT	BIT(S)	BIT NAME	FUNCTION	COMMENT
SECTION 0.4: INTERRUPT REGISTERS							
0x60	Interrupt Control	RW	0x00				
				2:0	interrupt_ctrl[2:0]	Select which interrupt mode to be used.	0: Interrupts disabled 1: Data ready 3: Interrupts disabled
SECTION 0.7: ANALOG CONTROL REGISTERS							
0x90	Driver Range	RW	0x06				
				3:0	driver_s[3:0]	Current DAC scale	Sets the maximum emitter driver 4.5MHz current (i.e., the peak of the square wave)
0x91	Emitter DAC	RW	0xFA				
				7:0	emitter_current[7:0]	Current DAC value	Emitter current calculation: Peak current = (0x90[3:0])*emitter_current[7:0]/255
0x92	Driver Control	RW	0x00				
				0	driver_thresh_en	Enable threshold DAC	0 - Threshold DAC disabled 1 - Threshold DAC enabled
0x93	Threshold DAC	RW	0x00	7:0	driver_t[7:0]	DC current added to signal current (Register 0x90 & 0x91)	Double write required to update all bits in this register.
0xA5	Emitter Offset	RW		3:0		Emitter voltage meas offset	LSB ≅ 0.125V, scales ADC range for 0xE1 measurement
0xB0	Command Register	RW	0x10		Specific codes defined		
					soft_start	Emulates sample start pin	Write 0xB0 = 0x49
					soft_reset	Resets all registers	Write 0xB0 = 0xD7
					soft_clear	Resets internal state machine	Write 0xB0 = 0xD1

Data Output Registers

TABLE 3. DATA OUTPUT REGISTERS AND BIT DEFINITIONS

ADDR	REGISTER NAME	ACCESS	BIT(s)	BIT NAME	FUNCTION	COMMENT
0xD1	Distance Readout MSB	RL	7:0	distance[15:8]	Distance output	Unsigned 16-bit integer
0xD2	Distance Readout LSB	RL	7:0	distance[7:0]	Distance output	
0xD3	Precision MSB	RL	7:0	precision[15:8]	Measurement noise approximation	Unsigned 16-bit integer
0xD4	Precision LSB	RL	7:0	precision[7:0]	Measurement noise approximation	
0xD5	Magnitude Exponent	RL	3:0	mag_exp[3:0]	Return signal magnitude	Unsigned 4-bit exponent
0xD6	Magnitude Significand MSB	RL	7:0	mag[15:8]	Return signal magnitude MSB	Unsigned 16-bit integer, LSB = 10fA
0xD7	Magnitude Significand LSB	RL	7:0	mag[7:0]	Return signal magnitude LSB	
0xD8	Phase Readout MSB	RL	7:0	phase[15:8]	Phase output MSB	Unsigned 16-bit integer, /2pi for radians
0xD9	Phase Readout LSB	RL	7:0	phase[7:0]	Phase output LSB	
0xDA	I Raw Exponent	RL	7:0	i_raw_exp[7:0]	In phase exponent	Unsigned 8-bit exponent
0xDB	I Raw MSB	RL	7:0	i_raw[15:8]	In phase MSB	Unsigned 16-bit integer
0xDC	I Raw LSB	RL	7:0	i_raw[7:0]	In phase LSB	
0xDD	Q Raw Exponent	RL	7:0	q_raw_exp[7:0]	Quadrature phase exponent	Unsigned 8-bit exponent
0xDE	Q Raw MSB	RL	7:0	q_raw[15:8]	Quadrature phase MSB	Unsigned 16-bit integer
0xDF	Q Raw LSB	RL	7:0	q_raw[7:0]	Quadrature phase LSB	
0xE1	Emitter Voltage After	RL	7:0	ev_after[7:0]	Emitter voltage	Unsigned 8-bit integer, LSB ~1.5mV
0xE2	Die Temperature	RL	7:0	temperature[7:0]	Die temperature sensor measurement	Unsigned 8-bit integer, LSB ~1.25°C
0xE3	Ambient Light	RL	7:0	ambient[7:0]	Ambient light measurement	Unsigned 8-bit integer, LSB ~3.5µA
0xE4	VGA1	RL	7:0	vga1_setting[7:0]	VGA1 programmed setting	Unsigned 8-bit integer
0xE5	VGA2	RL	7:0	vga2_setting[7:0]	VGA2 programmed setting	Unsigned 8-bit integer
0xE6	Gain MSB	RL	7:0	gain_msb[15:8]	AGC gain MSB	Unsigned 16-bit integer
0xE7	Gain LSB	RL	7:0	gain_lsb[7:0]	AGC gain LSB	

PCB Design Practices

- **This product is sensitive to noise and crosstalk. Precision analog layout practices can be applied to this chip as well.**
- PCB traces greater than 1" begin to exhibit transmission line characteristics with signal rise/fall times of 1ns or less. High frequency performance may be degraded for traces greater than one inch, unless strip line is used.
- Match channel-to-channel analog I/O trace lengths and layout symmetry. This will minimize propagation delay mismatches.
- Maximize the use of AC decoupled PCB layers. All signal I/O lines should be routed over continuous ground planes (i.e., no split planes or PCB gaps under these lines). Place vias in the signal I/O lines.
- Use proper value and location of termination resistors. Termination resistors should be as close to the device as possible.
- When testing use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum.
- A minimum of two power supply decoupling capacitors are recommended (1000pF, 0.01µF), place as close to the devices as possible. Do not use vias between the capacitor and the device because vias add unwanted inductance. Larger capacitors can be farther away from the device. When vias are required in a layout, they should be routed as far away from the device as possible.

PCB Layout Considerations

The use of multilayer PCB stack up is recommended to separate analog and emitter supplies. Placing a power supply plane located adjacent to the ground plane creates a large capacitance with little or no inductance. This will minimize ground bounce and improve power supply noise. The dielectric thickness separating these layers should be as thin as possible to minimize capacitive coupling.

It is important that power supplies be bypassed over a wide range of frequencies. A combination of large and small width capacitors that self resonate around the modulation frequency will provide ample suppression of fundamental and harmonics that can be coupled to the sensor power supplies (check ESR ratings).

Ensure that photodiode inputs pins (PDp and PDn) have symmetric and short traces and minimize placing aggressors around these routes. The guard shields provided on the IC should help minimize interference.

Ensure that emitter power (EVCC and EVSS) and ground traces are low resistance paths with a short return path to emitter ground.

Minimize trace length and vias to minimize inductance and minimize noise rejection.

The QFN Package Requires Additional PCB Layout Rules for the Thermal Pad

The thermal pad is electrically connected to V- supply through the high resistance IC substrate. Its primary function is to provide heat sinking for the IC. However, because of the connection to the V1- and V2- supply pins through the substrate, the thermal pad must be tied to the V- supply to prevent unwanted current flow to the thermal pad. Maximum AC performance is achieved if the thermal pad is attached to a dedicated decoupled layer in a multilayered PC board. In cases where a dedicated layer is not possible, AC performance may be reduced at upper frequencies.

The thermal pad requirements are proportional to power dissipation and ambient temperature. A dedicated layer eliminates the need for an individual thermal pad area. When a dedicated layer is not possible, an isolated thermal pad on another layer should be used. Pad area requirements should be evaluated on a case-by-case basis.

For additional information on PCB layout information, see AN1917, “ISL29501 Layout Design Guide”.

General Power PAD Design Considerations

The following is an example of how to use vias to remove heat from the IC.

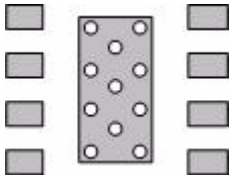


FIGURE 16. PCB VIA PATTERN

We recommend that you fill the thermal pad area with vias. A typical via array would be to fill the thermal pad footprint spaced such that they are center-on-center three times the radius apart from each other. Keep the vias small, but not so small that their inside diameter prevents solder wicking through the holes during reflow.

Connect all vias to the potential outlined in the datasheet for the pad, which typically the ground plane but not always, so check the pin description. It is important the vias have a low thermal resistance for efficient heat transfer. Do not use “thermal relief” patterns to connect the vias. It is important to have a complete connection of the plated through-hole to each plane.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure that you have the latest revision.

DATE	REVISION	CHANGE
May 5, 2017	FN8681.5	Changed the base address from 0xA4 to 0xA8 in “Chip Identification (Address)” on page 13.
Mar 17, 2017	FN8681.4	-Updated Related Literature section. -Changed terminology to “Standard Calibration” and added a high level description on page 15. -Simplified distance readout MSB comment in register listing on page 19. -Updated comments for Die Temperature register changed LSB from 1.15°C to 1.25°C page 19. -Data outputs on page 13, added formulas for distance, precision, magnitude, and phase. -Revised and elaborated the “Ambient Light ADC” on page 12.
Jun 29, 2016	FN8681.3	-Related Literature on page 1: Added “Cat Shark User Guide”. -Pin Description on page 4: Updated pins 4 and 5 from "tie to DVCC or DVSS" to "pull to DVCC or DVSS". -Ordering Information table on page 3 as follows: Added "ISL29501-CS-EVKIT1Z- Cat Shark Evaluation Board" and part number ISL29501IRZ-T7A. Renamed "ISL29501-ST-EV1Z" from "Evaluation Board" to "Sand Tiger Evaluation Board". -Principles of Operation on page 8: Reworded the entire section. -Updated Functional Overview on page 8. -Updated Interrupt Controller on page 13: Removed all the subsections excluding Noise Rejection, which was updated as well. -Updated Register Map table on page 16.
Mar 8, 2016	FN8681.2	“Electrical Specifications” on page 5: Changed I_{S-HS} sleep current from 1.5µA to 2.5µA. “Electrical Specifications” on page 5: Removed min and max values for VPDp and VPDn.
Oct 7, 2015	FN8681.1	page 16: Corrected and added bit definitions for registers 0x01 and 0x02. page 19: Moved output registers to their correct numerical order in the register space. page 16: Corrected the bit definitions for register 0x97. page 16: Added registers 0x19, 0xB0, 0xE2, 0xE3, 0xE4, 0xE5, 0xE6, 0xE7. page 8: Reworked I2C descriptions in the Functional Overview. page 15: Corrected I2C timing diagrams, former FIGURE 16 was deleted. page 16: Reworded and added significant content to the crosstalk and distance cal descriptions in Calibration section. Removed all references to collision detection on page12.
Jul 1, 2015	FN8681.0	Initial Release

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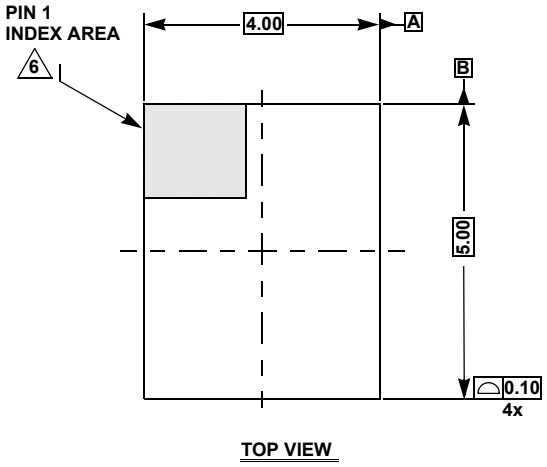
Package Outline Drawing

For the most recent package outline drawing, see L24.4x5F.

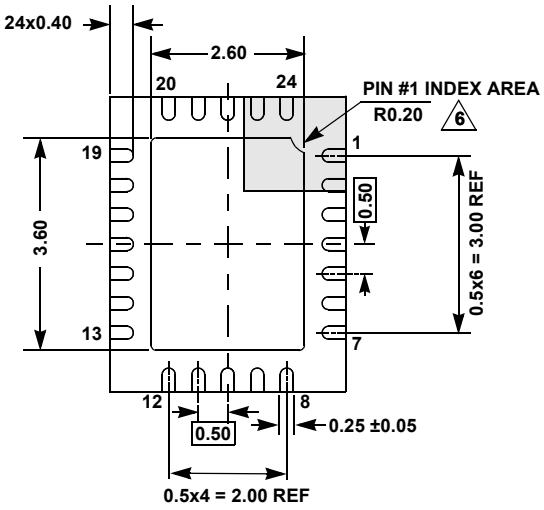
L24.4x5F

24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

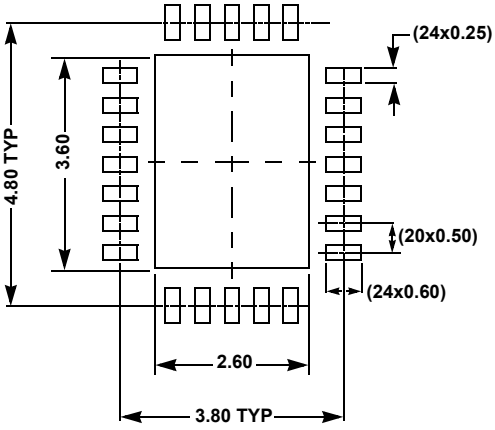
Rev 0, 5/14



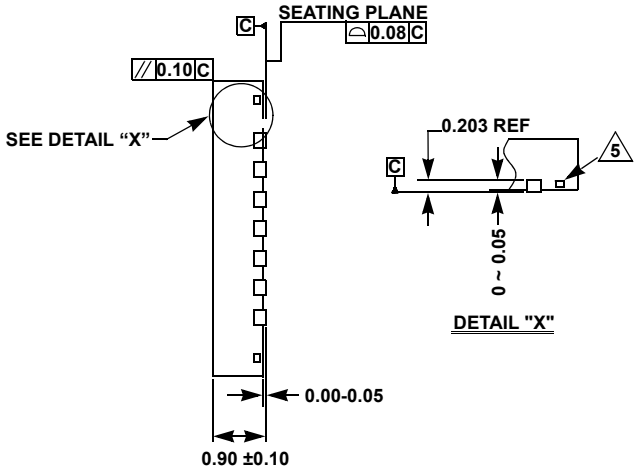
TOP VIEW



BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) are for Reference Only.
2. Dimensioning and tolerancing conform to ASMEY14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.20mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.