

钛地半导体
Tudi Semiconductor

# Product Specification

## TUDI-SN65HVD10-EP/SN65HVD12-EP

3.3 V RS-485 TRANSCEIVERS

网址 www.sztdbdt.com

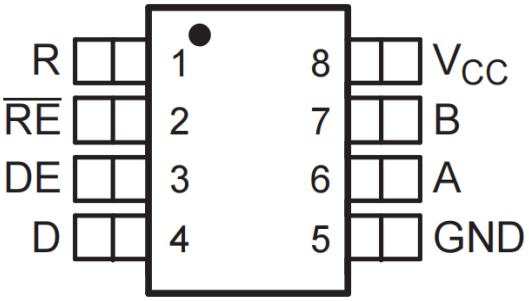
**用芯智造·卓越品质**

**semiconductor device manufacturer**

- Design
- research and development
- production
- and sales

## FEATURES

●Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
●Extended Temperature Performance of Up to -40℃ to 125℃ and-55℃ to 125℃
●Enhanced Diminishing Manufacturing Sources (DMS) Support
● Enhanced Product-Change Notification
●Qualification Pedigree(1)
●Operates With a 3.3 V Supply
● Bus-Pin ESD Protection Exceeds 16kV HBM
●1/8 Unit-Load Option Available (Up to 256 Nodes on the Bus)
●Optional Driver Output Transition Times for Signaling Rates of 1 Mbps,10 Mbps, and 25 Mbps(2)
●Meets or Exceeds the Requirements of ANSITIA /EIA-485-A
● Bus-Pin Short Circuit Protection From-7V to 12V
● Low-Current Standby Mode1 μA(Typ)
●Open-Circuit, Idle-Bus, and Shorted-Bus Failsafe Receiver
●Thermal Shutdown Protection
●Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications
● SN75176 Footprint

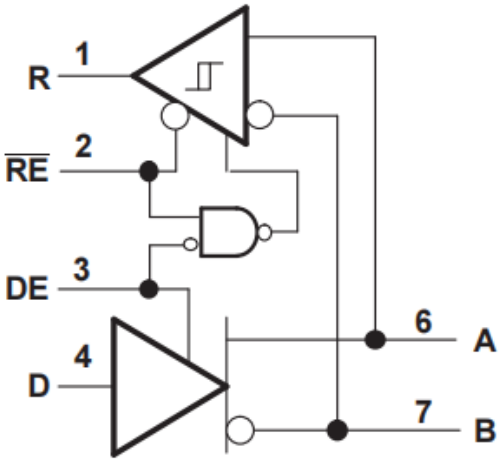



D PACKAGE
(TOP VIEW)

## APPLICATIONS

●Digital Motor Control
●Utility Meters
●Chassis-to-Chassis Interconnects
●Electronic Security Stations
●Industrial Process Control
●Building Automation
● Point-of-Sale(POS)Terminals and Networks

## LOGIC DIAGRAM (POSITIVE LOGIC)




## ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

| | | | SN65HVD10-EP<br>SN65HVD11-EP<br>SN65HVD12-EP |
|---|---|---|---|
| Supply voltage range, $V_{CC}$ | | | –0.3 V to 6 V |
| Voltage range at A or B | | | –9 V to 14 V |
| Input voltage range at D, DE, R, or $\overline{RE}$ | | | –0.5 V to $V_{CC}$ + 0.5 V |
| Voltage input range, transient pulse, A and B, through 100 Ω (see Figure 11) | | | –50 V to 50 V |
| Electrostatic discharge | Human body model(3) | A, B, and GND | 16 kV |
| | | All pins | 4 kV |
| | Charged-device model(4) | All pins Charge | 1 kV |
| Continuous total power dissipation | | | See Package Dissipation Rating Table |
| Storage temperature range, $T_{stg}$ | | | –65°C to 150°C |
| Lead temperature 1,6 mm (1/16 in) from case for 10 s | | | 260°C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

## PACKAGE DISSIPATION RATINGS

| PACKAGE | $T_A \leq 25°C$ POWER RATING | DERATING FACTOR(1) ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|---|
| D(2) | 597 mW | 4.97 mW/°C | 373 mW | 298 mW | 100 mW |
| D(3) | 990 mW | 8.26 mW/°C | 620 mW | 496 mW | 165 mW |

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) Tested in accordance with the Low-K thermal metric definitions of EIA/JESD51-3.
(3) Tested in accordance with the High-K thermal metric definitions of EIA/JESD51-7.

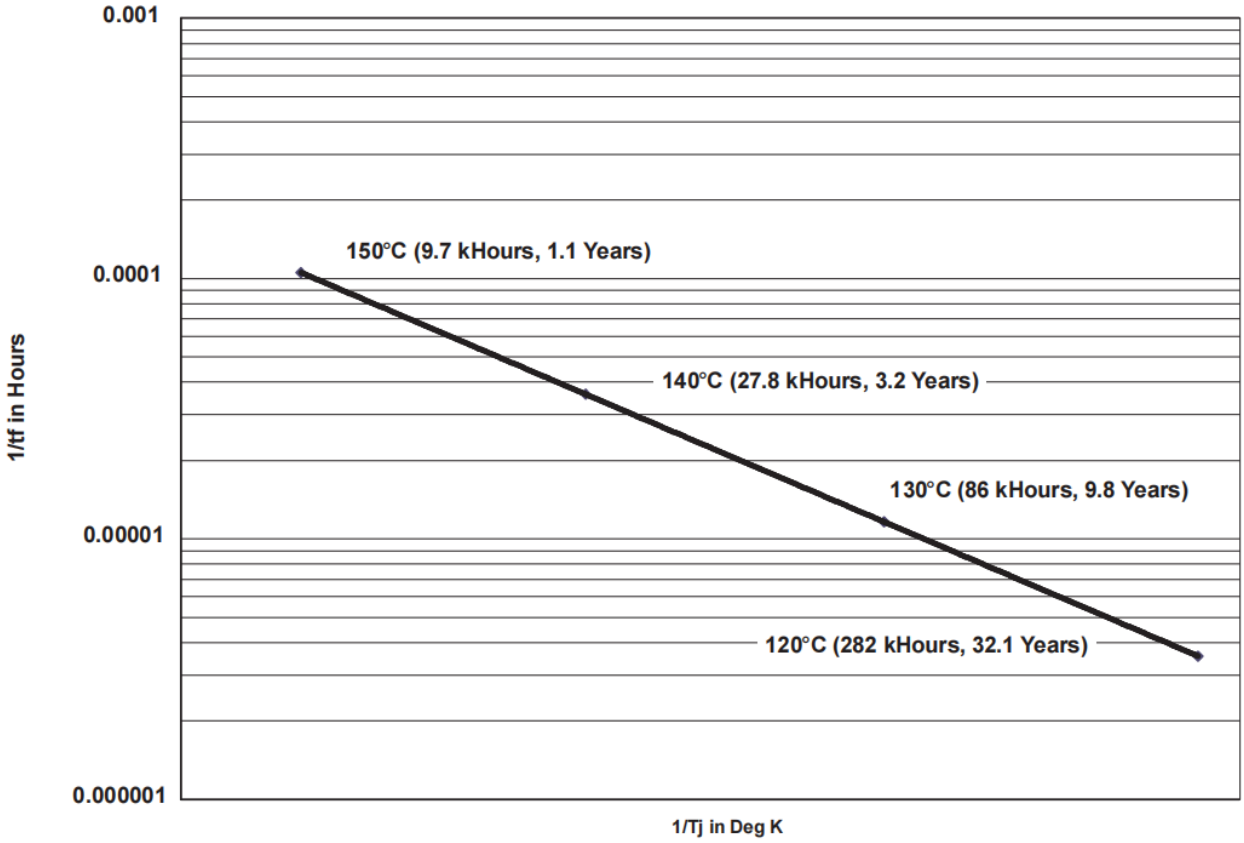



**Figure 1. Estimated Device Life Based Kirkendall Voiding Failure Mode**

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 3 | | 3.6 | V |
| Voltage at any bus terminal (separately or common mode) $V_I$ or $V_{IC}$ | | –7 (1) | | 12 | V |
| High-level input voltage, $V_{IH}$ | D, DE, $\overline{RE}$ | 2 | | $V_{CC}$ | V |
| Low-level input voltage, $V_{IL}$ | D, DE, $\overline{RE}$ | 0 | | 0.8 | V |
| Differential input voltage, $V_{ID}$ (see Figure 8) | | –12 | | 12 | V |
| High-level output current, $I_{OH}$ | Driver | –60 | | | mA |
| | Receiver | –8 | | | |
| Low-level output current, $I_{OL}$ | Driver | | | 60 | mA |
| | Receiver | | | 8 | |
| Differential load resistance, $R_L$ | | 54 | 60 | | Ω |
| Differential load capacitance, $C_L$ | | | 50 | | pF |
| Signaling rate | HVD10 | | | 25 | Mbps |
| | HVD11 | | | 10 | |
| | HVD12 | | | 1 | |

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

## DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP (1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | | $I_I$ = –18 mA | | –1.5 | | | V |
| $\lvert V_{OD}\rvert$ | Differential output voltage (2) | | $I_O$ = 0 | | 2 | | $V_{CC}$ | V |
| | | | $R_L$ = 54 Ω, See Figure 2 | | 1.5 | | | |
| | | | $V_{test}$ = –7 V to 12 V, See Figure 3 | | 1.5 | | | |
| $\Delta\lvert V_{OD}\rvert$ | Change in magnitude of differential output voltage | | See Figure 2 and Figure 3 | | –0.2 | | 0.2 | V |
| $V_{OC(PP)}$ | Peak-to-peak common-mode output voltage | | See Figure 4 | | | 400 | | mV |
| $V_{OC(SS)}$ | Steady-state common-mode output voltage | | | | 1.4 | | 2.5 | V |
| $\Delta V_{OC(SS)}$ | Change in steady-state common-mode output voltage | | | | –0.05 | | 0.05 | V |
| $I_{OZ}$ | High-impedance output current | | See receiver input currents | | | | | |
| $I_I$ | Input current | D | | | –100 | | 0 | μA |
| | | DE | | | 0 | | 100 | |
| $I_{OS}$ | Short-circuit output current | | –7 V ≤ $V_O$ ≤ 12 V | | –250 | | 250 | mA |
| $C_{(OD)}$ | Differential output capacitance | | $V_{OD}$ = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V | | | 16 | | pF |
| $I_{CC}$ | Supply current | | $\overline{RE}$ at $V_{CC}$, D and DE at $V_{CC}$, No load | Receiver disabled and driver enabled | | 9 | 15.5 | mA |
| | | | $\overline{RE}$ at $V_{CC}$, D at $V_{CC}$, DE at 0 V, No load | Receiver disabled and driver disabled (standby) | | 1 | 5 | μA |
| | | | $\overline{RE}$ at 0 V, D and DE at $V_{CC}$, No load | Receiver enabled and driver enabled | | 9 | 15.5 | mA |

(1) All typical values are at 25°C and with a 3.3 V supply.
(2) For $T_A$ > 85°C, $V_{CC}$ is ±5%.

## DRIVER SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high level output | HVD10 | $R_L$ = 54 Ω, $C_L$ = 50 pF, See Figure 5 | 5 | 8.5 | 16 | ns |
| | | HVD11 | | 18 | 25 | 40 | |
| | | HVD12 | | 135 | 200 | 330 | |
| $t_{PHL}$ | Propagation delay time, high-to-low level output | HVD10 | | 5 | 8.5 | 16 | ns |
| | | HVD11 | | 18 | 25 | 40 | |
| | | HVD12 | | 135 | 200 | 330 | |
| $t_r$ | Differential output signal rise time | HVD10 | | 3 | 4.5 | 11.5 | ns |
| | | HVD11 | | 10 | 20 | 30 | |
| | | HVD12 | | 100 | 170 | 330 | |
| $t_f$ | Differential output signal fall time | HVD10 | | 3 | 4.5 | 11.5 | ns |
| | | HVD11 | | 10 | 20 | 30 | |
| | | HVD12 | | 100 | 170 | 330 | |
| $t_{sk(p)}$ | Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$) | HVD10 | | | | 1.5 | ns |
| | | HVD11 | | | | 2.5 | |
| | | HVD12 | | | | 9 | |
| $t_{sk(pp)}$ (2) | Part-to-part skew | HVD10 | | | | 6 | ns |
| | | HVD11 | | | | 11 | |
| | | HVD12 | | | | 100 | |
| $t_{PZH}$ | Propagation delay time, high impedance-to-high level output | HVD10 | $R_L$ = 110 Ω, $\overline{RE}$ at 0 V, See Figure 6 | | | 33 | ns |
| | | HVD11 | | | | 55 | |
| | | HVD12 | | | | 320 | |
| $t_{PHZ}$ | Propagation delay time, high level-to-high-impedance output | HVD10 | | | | 26 | ns |
| | | HVD11 | | | | 55 | |
| | | HVD12 | | | | 320 | |
| $t_{PZL}$ | Propagation delay time, high impedance-to-low-level output | HVD10 | $R_L$ = 110 Ω, $\overline{RE}$ at 0 V, See Figure 7 | | | 26 | ns |
| | | HVD11 | | | | 55 | |
| | | HVD12 | | | | 320 | |
| $t_{PLZ}$ | Propagation delay time, low level-to-high-impedance output | HVD10 | | | | 26 | ns |
| | | HVD11 | | | | 75 | |
| | | HVD12 | | | | 420 | |
| $t_{PZH}$ | Propagation delay time, standby-to-high-level output | I and Q-temp | $R_L$ = 110 Ω, $\overline{RE}$ at 3 V, See Figure 6 | | | 6 | µs |
| | | M-temp | | | | 14 | |
| $t_{PZL}$ | Propagation delay time, standby-to-low-level output | I and Q-temp | $R_L$ = 110 Ω, $\overline{RE}$ at 3 V, See Figure 7 | | | 6 | µs |
| | | M-temp | | | | 14 | |

(1) All typical values are at 25°C and with a 3.3 V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

## RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | $I_O$ = –8 mA | | | | | –0.01 | V |
| $V_{IT-}$ | Negative-going input threshold voltage | $I_O$ = 8 mA | | | –0.2 | | | V |
| $V_{hys}$ | Hysteresis voltage ($V_{IT+} – V_{IT-}$) | | | | | 35 | | mV |
| $V_{IK}$ | Enable-input clamp voltage | $I_I$ = –18 mA | | | –1.5 | | | V |
| $V_{OH}$ | High-level output voltage | $V_{ID}$ = 200 mV, | $I_{OH}$ = –8 mA, | See Figure 8 | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $V_{ID}$ = –200 mV, | $I_{OL}$ = 8 mA, | See Figure 8 | | | 0.4 | V |
| $I_{OZ}$ | High-impedance-state output current | $V_O$ = 0 or $V_{CC}$ | $\overline{RE}$ at $V_{CC}$ | | –1 | | 1 | µA |
| $I_I$ | Bus input current | $V_A$ or $V_B$ = 12 V | | HVD11, HVD12, Other input at 0 V | | 0.05 | 0.11 | mA |
| | | $V_A$ or $V_B$ = 12 V, | $V_{CC}$ = 0 V | HVD11, HVD12, Other input at 0 V | | 0.06 | 0.13 | mA |
| | | $V_A$ or $V_B$ = –7 V | | HVD11, HVD12, Other input at 0 V | –0.1 | –0.05 | | mA |
| | | $V_A$ or $V_B$ = –7 V, | $V_{CC}$ = 0 V | HVD11, HVD12, Other input at 0 V | –0.05 | ÷0.04 | | mA |
| | | $V_A$ or $V_B$ = 12 V | | HVD10, Other input at 0 V | | 0.2 | 0.5 | mA |
| | | $V_A$ or $V_B$ = 12 V, | $V_{CC}$ = 0 V | HVD10, Other input at 0 V | | 0.25 | 0.5 | mA |
| | | $V_A$ or $V_B$ = –7 V | | HVD10, Other input at 0 V | –0.4 | –0.2 | | mA |
| | | $V_A$ or $V_B$ = –7 V, | $V_{CC}$ = 0 V | HVD10, Other input at 0 V | –0.4 | –0.15 | | mA |
| $I_{IH}$ | High-level input current, $\overline{RE}$ | $V_{IH}$ = 2 V | | | –30 | | 0 | µA |
| $I_{IL}$ | Low-level input current, $\overline{RE}$ | $V_{IL}$ = 0.8 V | | | –30 | | 0 | µA |
| $C_{ID}$ | Differential input capacitance | $V_{ID}$ = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V | | | | 15 | | pF |
| $I_{CC}$ | Supply current | $\overline{RE}$ at 0 V, D and DE at 0 V, No load | Receiver enabled and driver disabled | | | 4 | 8 | mA |
| | | $\overline{RE}$ at $V_{CC}$, D at $V_{CC}$, DE at 0 V, No load | Receiver disabled and driver disabled (standby) | | | 1 | 5 | µA |
| | | $\overline{RE}$ at 0 V, D and DE at $V_{CC}$, No load | Receiver enabled and driver enabled | | | 9 | 15.5 | mA |

(1) All typical values are at 25°C and with a 3.3 V supply.

## RECEIVER SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high level output | HVD10 | $V_{ID}$ = –1.5 V to 1.5 V, $C_L$ = 15 pF, See Figure 9 | 12.5 | 20 | 25 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low level output | HVD10 | | 12.5 | 20 | 25 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high level output | HVD11 HVD12 | | 30 | 55 | 70 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low level output | HVD11 HVD12 | | 30 | 55 | 70 | ns |
| $t_{sk(p)}$ | Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$) | HVD10 | | | | 1.5 | ns |
| | | HVD11 | | | | 4 | |
| | | HVD12 | | | | 4 | |
| $t_{sk(pp)}$(2) | Part-to-part skew | HVD10 | | | | 8 | ns |
| | | HVD11 | | | | 15 | |
| | | HVD12 | | | | 15 | |
| $t_r$ | Output signal rise time | | $C_L$ = 15 pF, See Figure 9 | 1 | 2 | 6 | ns |
| $t_f$ | Output signal fall time | | | 1 | 2 | 6 | |
| $t_{PZH}$(1) | Output enable time to high level | | $C_L$ = 15 pF, DE at 3 V, See Figure 10 | | | 16 | ns |
| $t_{PZL}$(1) | Output enable time to low level | | | | | 16 | |
| $t_{PHZ}$ | Output disable time from high level | | | | | 21 | |
| $t_{PLZ}$ | Output disable time from low level | | | | | 16 | |
| $t_{PZH}$(2) | Propagation delay time, standby-to-high-level output | I and Q-temp | $C_L$ = 15 pF, DE at 0, See Figure 11 | | | 6 | µs |
| | | M-temp | | | | 14 | |
| $t_{PZL}$(2) | Propagation delay time, standby-to-low-level output | I and Q-temp | | | | 6 | |
| | | M-temp | | | | 14 | |

(1) All typical values are at 25°C and with a 3.3 V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

## THERMAL CHARACTERISTICS(1)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance(2) | High-K board(3), No airflow | D package | | 121 | | °C/W |
| $\theta_{JB}$ | Junction-to-board thermal resistance | High-K board | D package | | 67 | | °C/W |
| $\theta_{JC}$ | Junction-to-case thermal resistance | | D package | | 41 | | °C/W |
| $P_D$ | Device power dissipation | $R_L$ = 60 Ω, $C_L$ = 50 pF, DE at $V_{CC}$, $\overline{RE}$ at 0 V, Input to D a 50% duty cycle square wave at indicated signaling rate | HVD10 (25 Mbps) | | 198 | 233 | mW |
| | | | HVD11 (10 Mbps) | | 141 | 176 | mW |
| | | | HVD12 (500 kbps) | | 133 | 161 | mW |
| $T_{JSD}$ | Thermal shutdown junction temperature | | | | 165 | | °C |

(1) See *Application Information* section for an explanation of these parameters.
(2) The intent of $\theta_{JA}$ specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.
(3) JSD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.

## PARAMETER MEASUREMENT INFORMATION

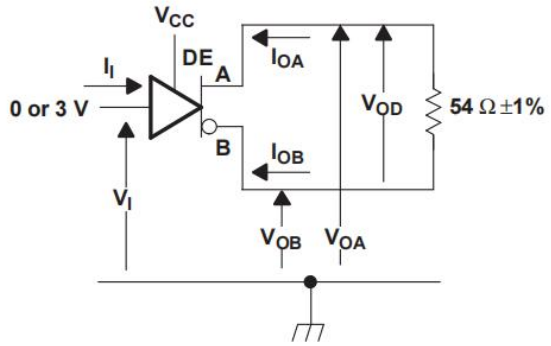



Figure 2. Driver $V_{OD}$ Test Circuit and Voltage and Current Definitions

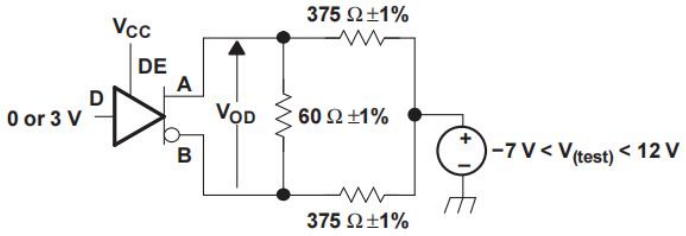
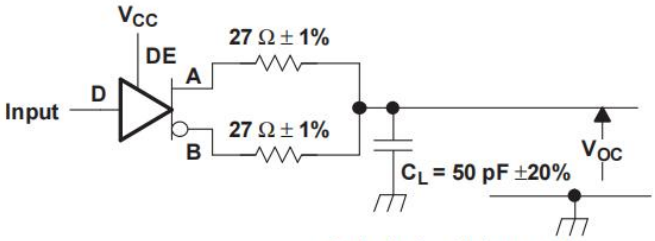
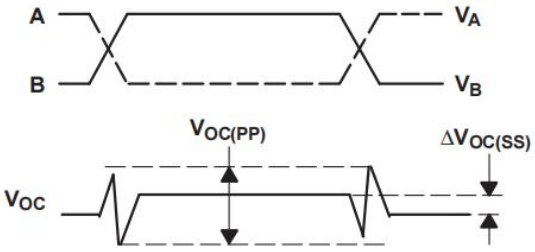



Figure 3. Driver $V_{OD}$ With Common-Mode Loading Test Circuit

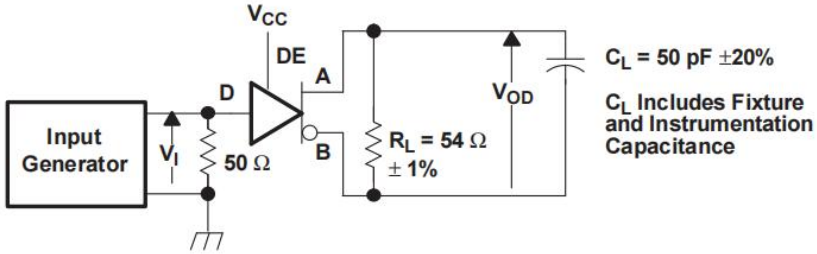


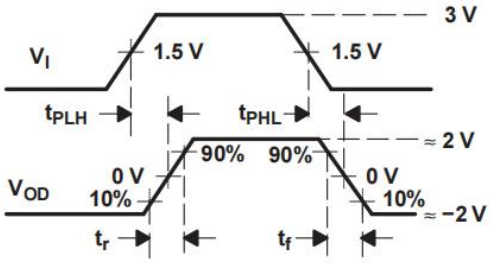

$C_L$ Includes Fixture and Instrumentation Capacitance




Input: PRR = 500 kHz, 50% Duty Cycle, $t_r$ < 6 ns, $t_f$ < 6 ns, $Z_O$ = 50 Ω

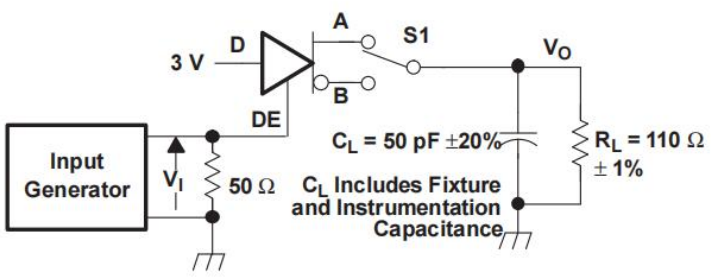
**Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage**

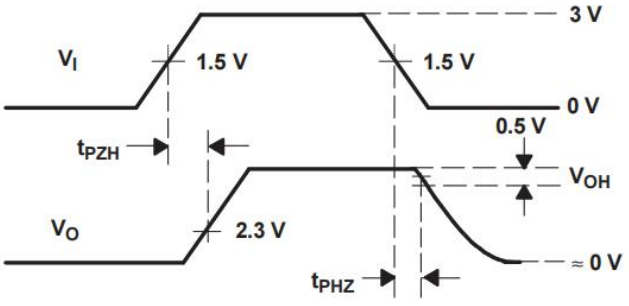



Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r$ < 6 ns, $t_f$ < 6 ns, $Z_o$ = 50 Ω

**Figure 5. Driver Switching Test Circuit and Voltage Waveforms**

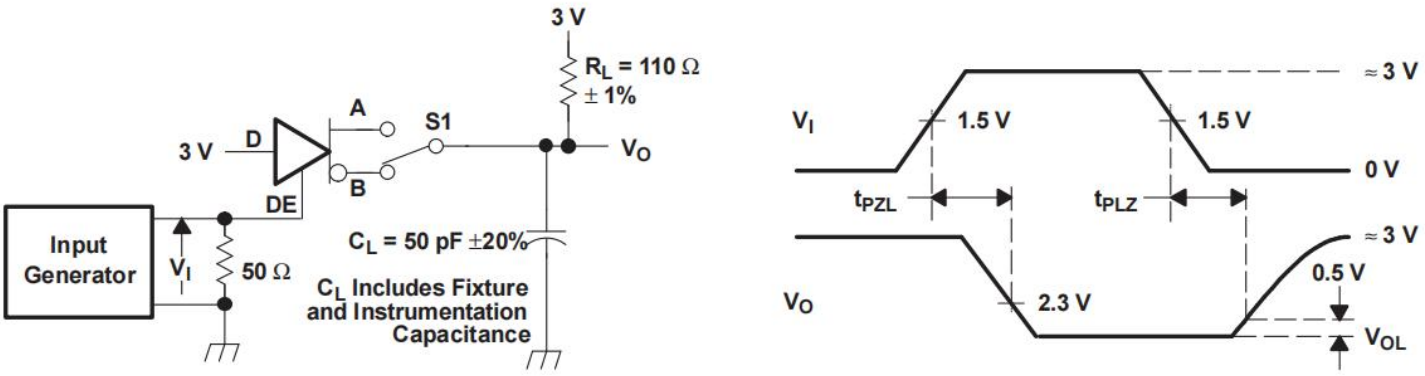



Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r$ < 6 ns, $t_f$ < 6 ns, $Z_o$ = 50 Ω

**Figure 6. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION (continued)




Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r$ < 6 ns, $t_f$ < 6 ns, $Z_o$ = 50 Ω

**Figure 7. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms**

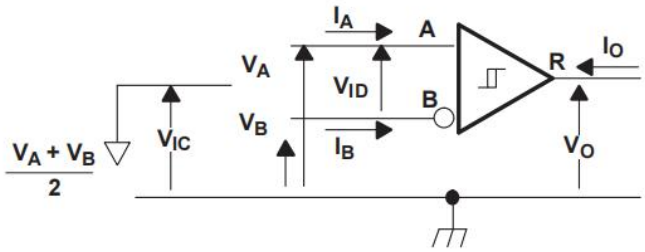
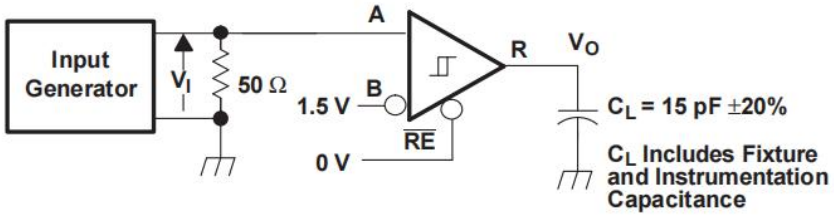



**Figure 8. Receiver Voltage and Current Definitions**




Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r$ < 6 ns, $t_f$ < 6 ns, $Z_o$ = 50 Ω

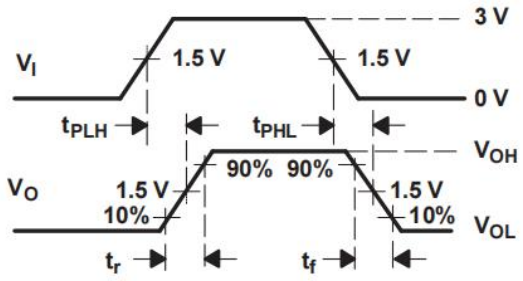
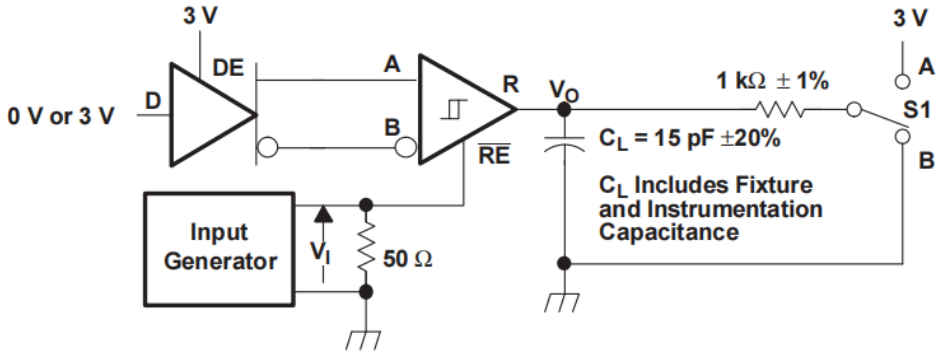



**Figure 9. Receiver Switching Test Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION (continued)




Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r$ < 6 ns, $t_f$ < 6 ns, $Z_o$ = 50 Ω

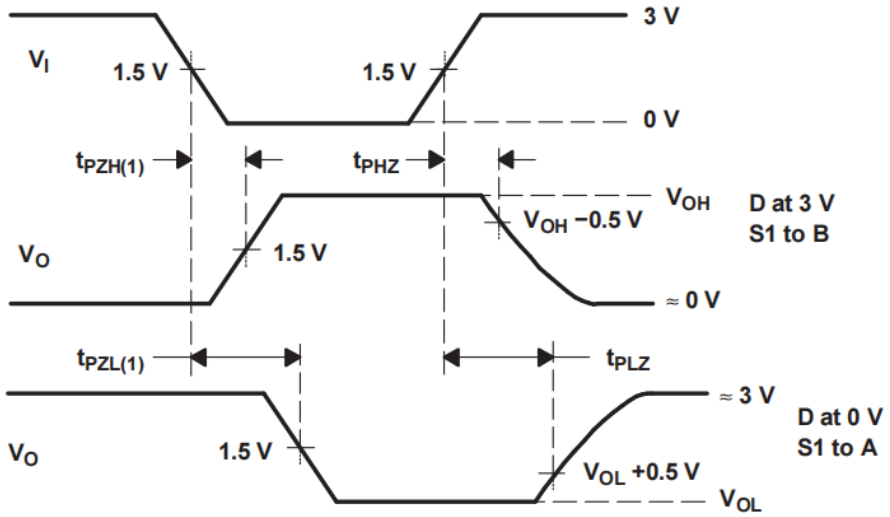
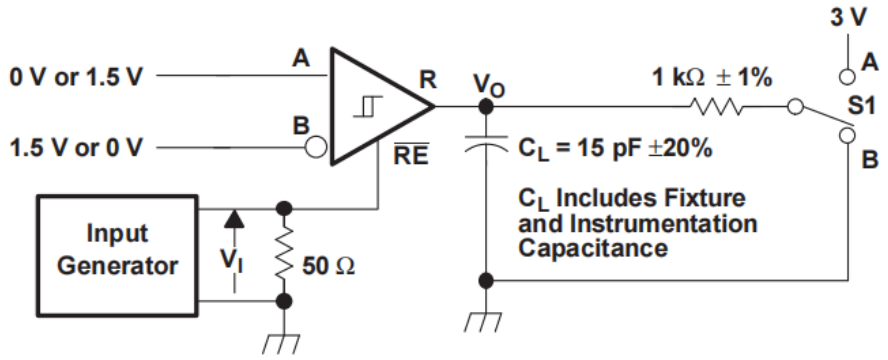



**Figure 10. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled**

## PARAMETER MEASUREMENT INFORMATION (continued)




Generator: PRR = 100 kHz, 50% Duty Cycle, $t_r$ < 6 ns, $t_f$ < 6 ns, $Z_o$ = 50 Ω

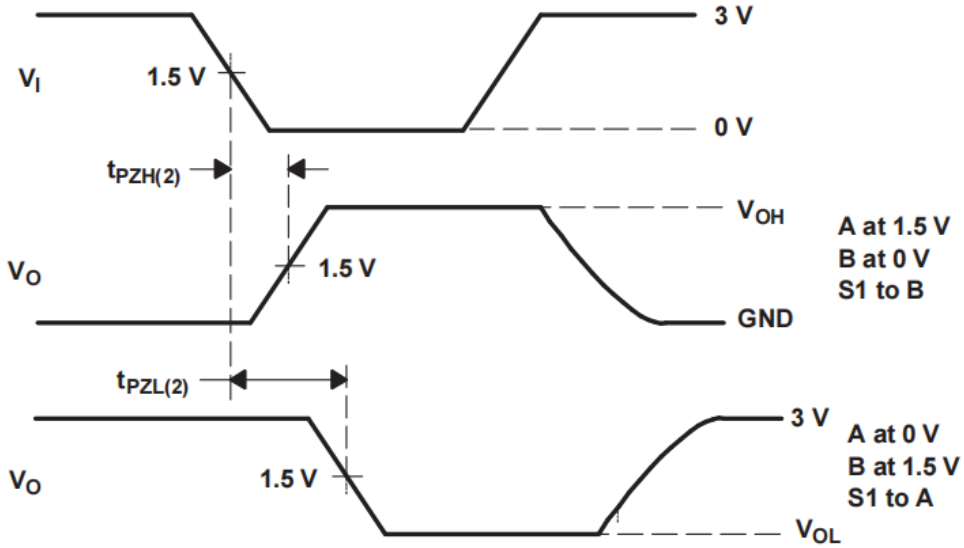
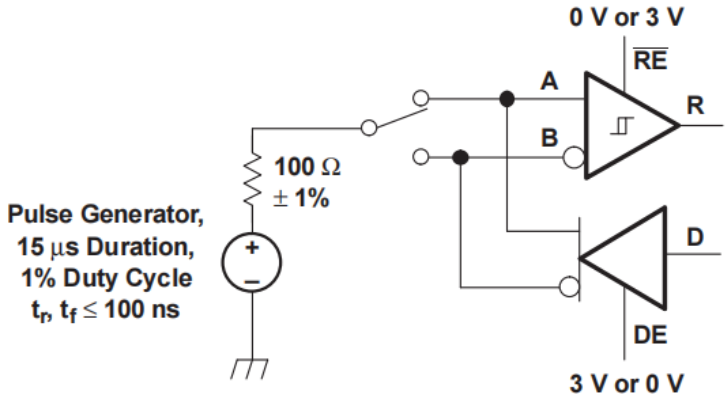



**Figure 11. Receiver Enable Time From Standby (Driver Disabled)**




NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

**Figure 12. Test Circuit, Transient Over Voltage Test**

## Function Tables

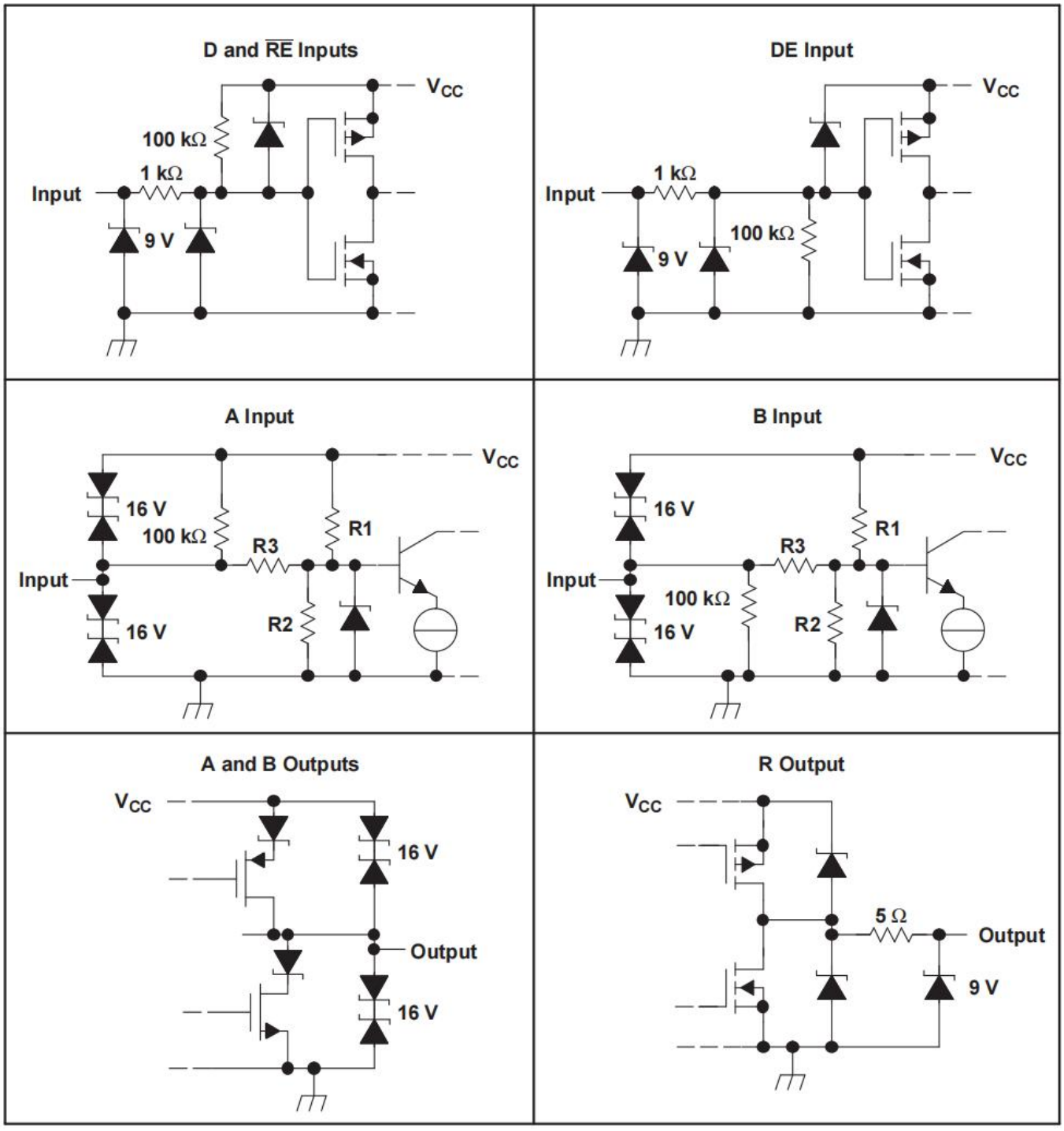
### DRIVER

| INPUT D | ENABLE DE | OUTPUTS | |
|---|---|---|---|
| | | A | B |
| H | H | H | L |
| L | H | L | H |
| X | L | Z | Z |
| Open | H | H | L |

### RECEIVER

| DIFFERENTIAL INPUTS $V_{ID} = V_A - V_B$ | ENABLE $\overline{RE}$ | OUTPUT R |
|---|---|---|
| $V_{ID} \leq -0.2$ V | L | L |
| $-0.2$ V $< V_{ID} < -0.01$ V | L | ? |
| $-0.01$ V $\leq V_{ID}$ | L | H |
| X | H | Z |
| Open Circuit | L | H |
| Short Circuit | L | H |

## EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

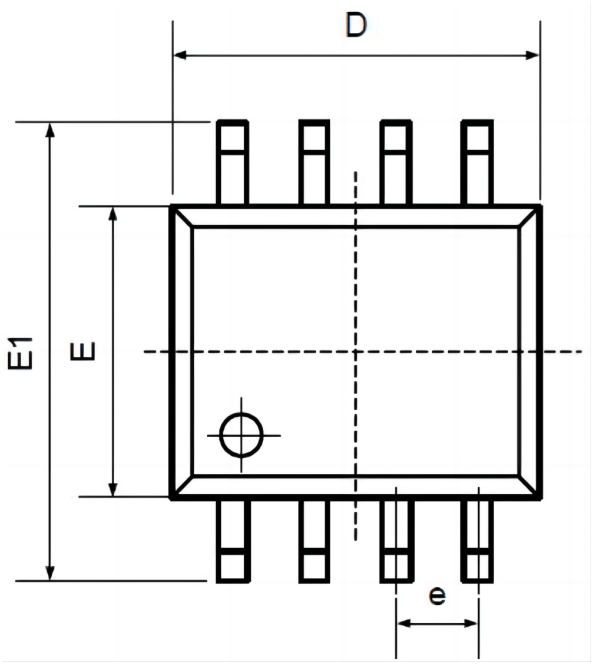


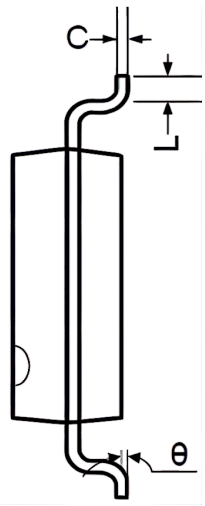

| | R1/R2 | R3 |
|---|---|---|
| SN65HVD10 | 9 kΩ | 45 kΩ |
| SN65HVD11 | 36 kΩ | 180 kΩ |
| SN65HVD12 | 36 kΩ | 180 kΩ |

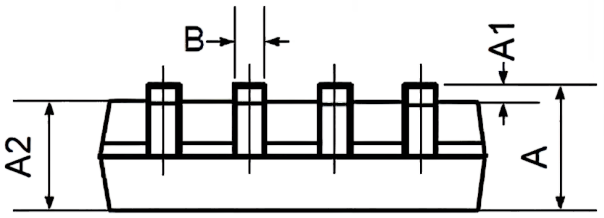
# Order information

| Order Number | Package | Package Quantity | Marking On The park |
|---|---|---|---|
| SN65HVD10MDREP-TUDI | SOP8 | Tape,Reel,2500 | V10MEP |
| SN65HVD10QDREP-TUDI | SOP8 | Tape,Reel,2500 | V10QEP |
| SN65HVD12IDREP-TUDI | SOP8 | Tape,Reel,2500 | V12IEP |

# Package SOP8




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| B | 0.330 | 0.510 | 0.013 | 0.020 |
| C | 0.190 | 0.250 | 0.007 | 0.010 |
| D | 4.780 | 5.000 | 0.188 | 0.197 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.300 | 0.228 | 0.248 |
| e | 1.270TYP | | 0.050TYP | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

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