

钍地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65HVD82DR

Robust and durable RS-485 transceiver

网址 www.sztdbdt.com

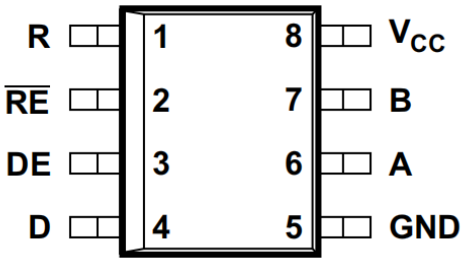
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- Bus I/O protection
  - ±16kV Human Body Model (HBM) protection
  - ±12kV IEC 6100-4-2 contact discharge
  - 4kV IEC61000-4-4 fast transient burst
- Industrial temperature range: -40°C to 85C
- Larger receiver hysteresis for noise immunity (typical value 60mV)
- Low power consumption
  - <1μA standby current
  - <1mA static current
- Optimized transmission rate up to 250kbps
- Create custom designs with SN65HVD82 using WEBENCH® Power Designer



D Package
16-Pin SOIC
(Top View)

Applications

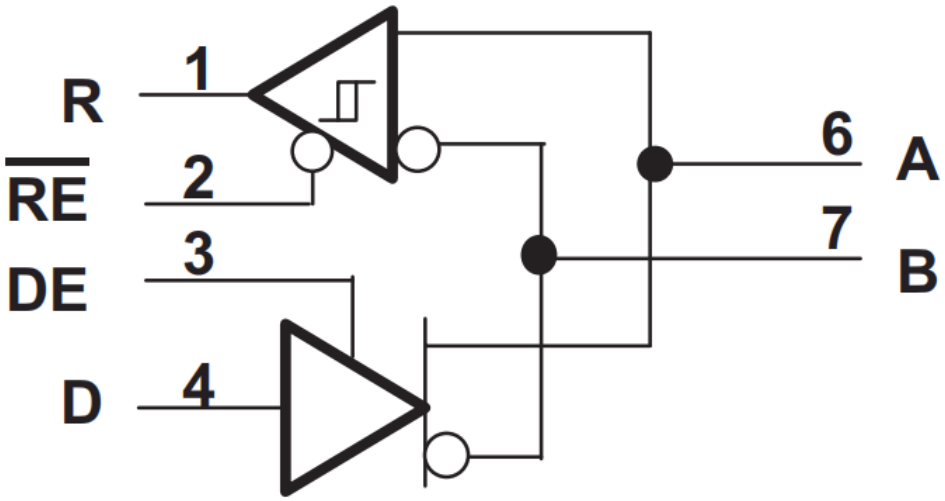
- Smart meters
- Building automation
- Industrial networks
- Secure electronic devices

Description

This device combines driver and receiver functions, is robust and durable, and can meet the strict requirements of specific industrial applications. These bus pins are ESDtolerant and feature a high level of protection compliant with Human Body Model, Air Gap Discharge, and Contact Discharge standards.

The device combines a differential driver and a differential receiver, both powered single 5V supply. The driver differential outputs and receiver differential inputs are internally connected to form a bus port suitable for half-duplex (two-wire bus) communication. The device has common-mode voltage range, making it suitable for multi-point applications over long cables. The device's rated temperature range is between -40°C and 85°

逻辑图（正逻辑）



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low
V_{CC}	8	Supply	4.5-V to 5.5-V supply

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	7	V
	Voltage range at A or B Inputs	–18	18	V
	Input voltage range at any logic pin	–0.3	5.7	V
	Voltage input range, transient pulse, A and B, through 100Ω	–100	100	V
	Receiver output current	–24	24	mA
T_J	Junction temperature		170	°C
	Continuous total power dissipation	See *Thermal Information*		
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1500	
		Machine model (MM), JEDEC Standard 22		±400	
		IEC 61000-4-2 ESD (Contact Discharge)	Bus terminals and GND	±12000	
		IEC 60749-26 ESD (Human Body Model)	Bus terminals and GND	±16000	
		IEC 61000-4-4 EMC (Fast Transient Burst Immunity)	Bus terminals and GND	±4000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)(1)	–7		12	V
V_{IH}	High-level input voltage (D, DE and $\overline{RE}$ inputs)	2		V_{CC}	V
V_{IL}	Low-level input voltage (D, DE and $\overline{RE}$ inputs)	0		0.8	V
V_{ID}	Differential input voltage (A and B inputs)	–12		12	V
I_O	Output current, Driver	–60		60	mA
	Output current, Receiver	–8		8	mA
R_L	Differential load resistance	54	60		Ω
C_L	Differential load capacitance		50		pF
$1/t_{UI}$	Signaling rate			250	kbps
T_A	Operating free-air temperature (see *Application and Implementation* section for thermal information)	–40		85	°C
T_J	Junction Temperature	–40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

6.4 Thermal Information

THERMAL METRIC(1)		SN65HVD82 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential output voltage magnitude	See Figure 5, R_L = 60 Ω, 375 Ω on each output to –7 V to 12 V		1.5			V
		R_L = 54 Ω (RS-485)	See Figure 6	1.5	2		V
		R_L = 100 Ω (RS-422)		2	2.5		V
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L = 54 Ω, C_L = 50 pF	See Figure 6	–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	Center of two 27-Ω load resistors	See Figure 6	1	V_{CC}/2	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage			–0.2	0	0.2	V
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage				850		mV
C_{OD}	Differential output capacitance				8		pF
V_{IT+}	Positive-going receiver differential input voltage threshold			See (1)	–70	-20	mV
V_{IT-}	Negative-going receiver differential input voltage threshold			–200	–150	See (1)	mV
V_{HYS}	Receiver differential input voltage threshold hysteresis ($V_{IT+} – V_{IT-}$)			40	60		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = -8 mA		4	V_{CC}–0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA			0.2	0.4	V
I_I	Driver input, driver enable, and receiver enable input current			–2		2	µA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}		–10		10	µA
I_{OS}	Driver short-circuit output current	$\|I_{OS}\|$ with V_A or V_B from –7 V to +12 V				150	mA
I_I	Bus input current (disabled driver)	V_{CC} = 4.5 to 5.5 V or V_{CC} = 0 V, DE at 0 V	V_I = 12 V		75	125	µA
			V_I = –7 V	–100	–40		
I_{CC}	Supply current (quiescent)	Driver and Receiver enabled	DE = V_{CC}, RE=GND, No load			900	µA
		Driver enabled, receiver disabled	DE = V_{CC}, RE = V_{CC}, No load			650	
		Driver disabled, receiver enabled	DE = GND, RE = GND, No load			650	
		Driver and receiver disabled	DE = GND, D=GND, RE = V_{CC}, No load		0.4	2	
	Supply current (dynamic)	See *Typical Characteristics*					

(1) Under any specific conditions, V_{IT+} is assured to be at least V_{HYS} higher than V_{IT-}.

6.6 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 7		400	700	1200	ns
t_{PHL}, t_{PLH}	Driver propagation delay			90	700	1000	ns
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$				25	200	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 8 and Figure 9		50	500	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			500	1000	ns
		Receiver disabled			3	9	µs
RECEIVER							
t_r, t_f	Receiver output rise/fall time	C_L = 15 pF, See Figure 10			18	30	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				85	195	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$				1	15	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				50	500	ns
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled, See Figure 11			20	130	ns
		Driver disabled, See Figure 12			2	8	µs

7 Parameter Measurement Information

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω.

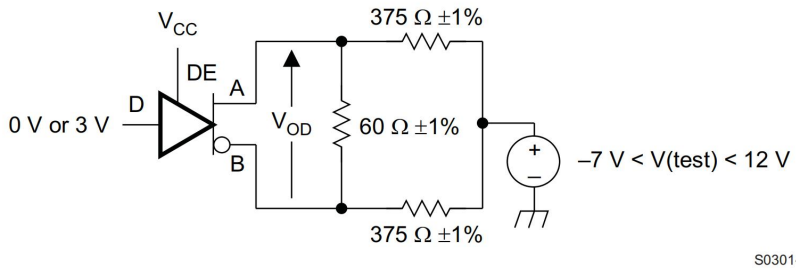


Figure 5. Measurement of Driver Differential Output Voltage With Common-Mode Load

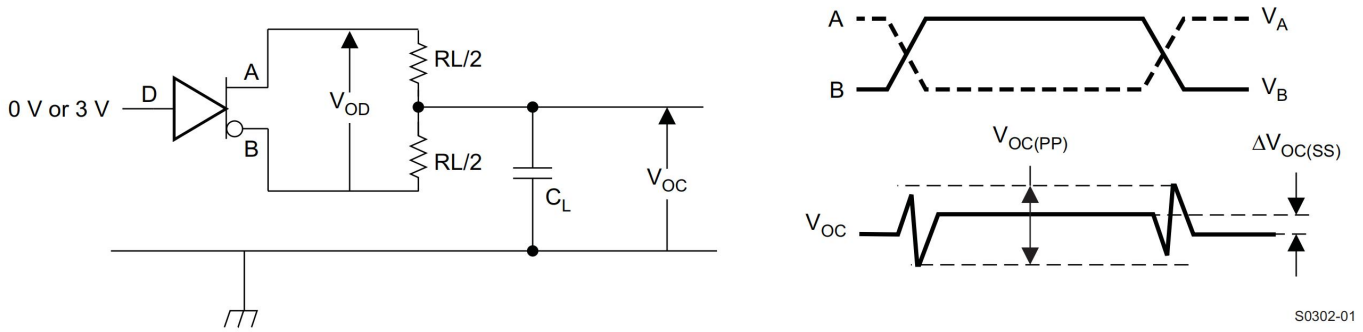
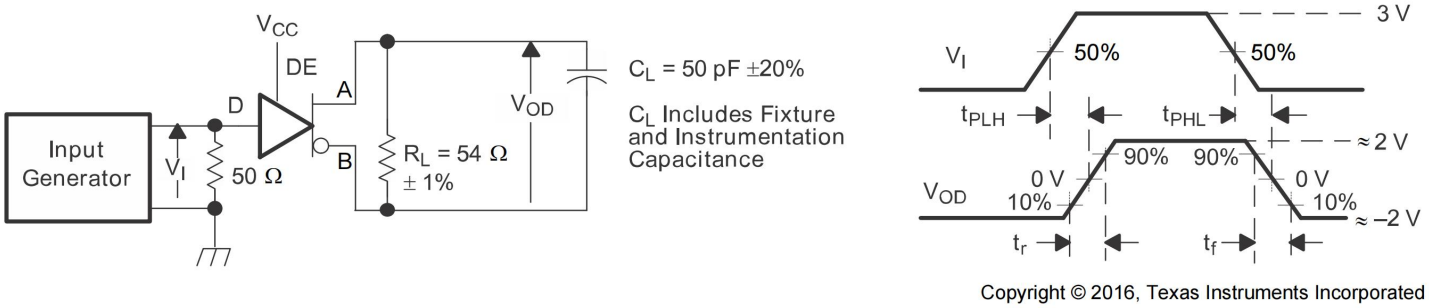
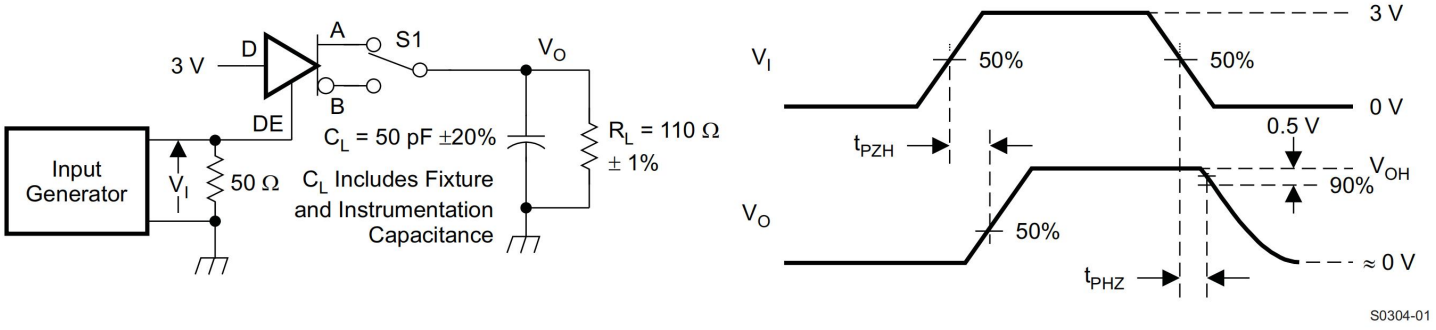


Figure 6. Measurement of Driver Differential and Common-Mode Output With RS-485 Load



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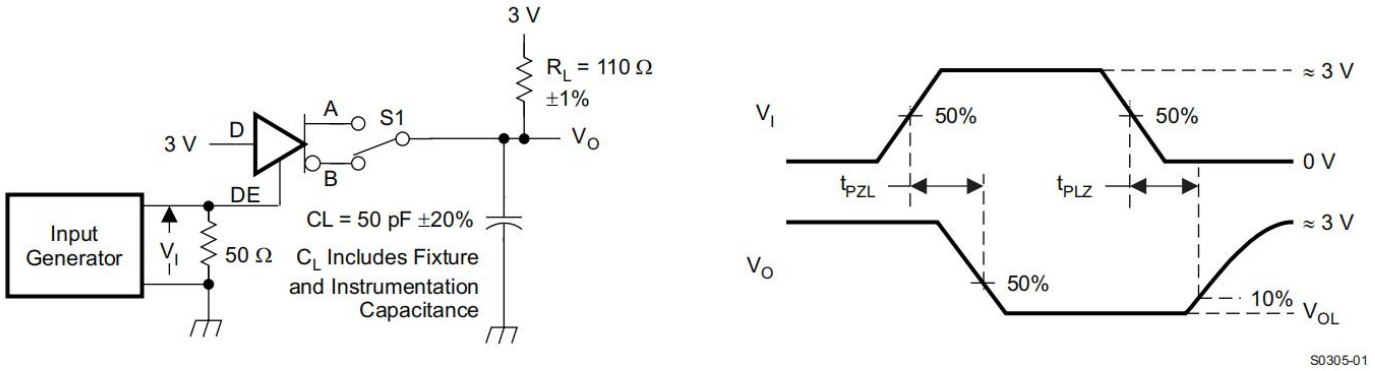
Figure 7. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



D at 3V to test non-inverting output, D at 0V to test inverting output.

Figure 8. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

Parameter Measurement Information (continued)



D at 0V to test non-inverting output, D at 3V to test inverting output.

Figure 9. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

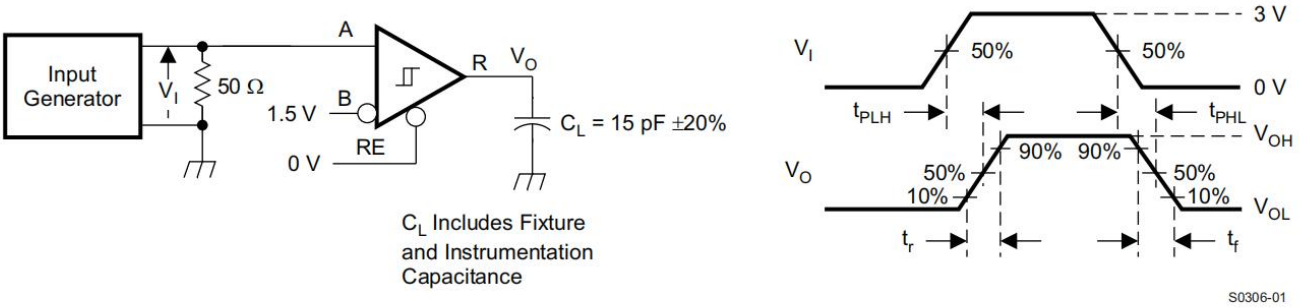


Figure 10. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

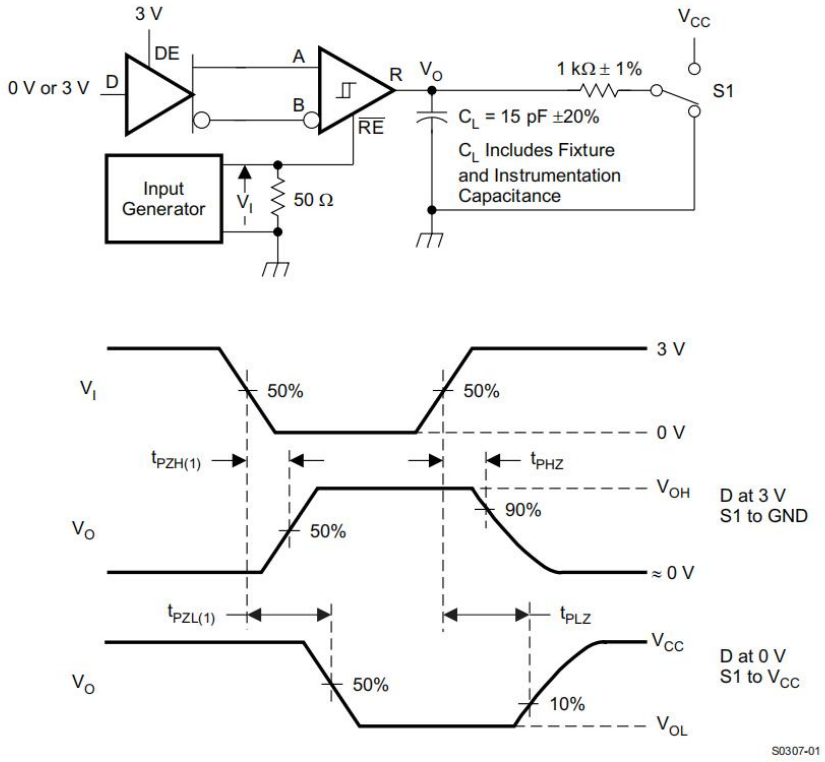


Figure 11. Measurement of Receiver Enable/Disable Times With Driver Enabled

Parameter Measurement Information (continued)

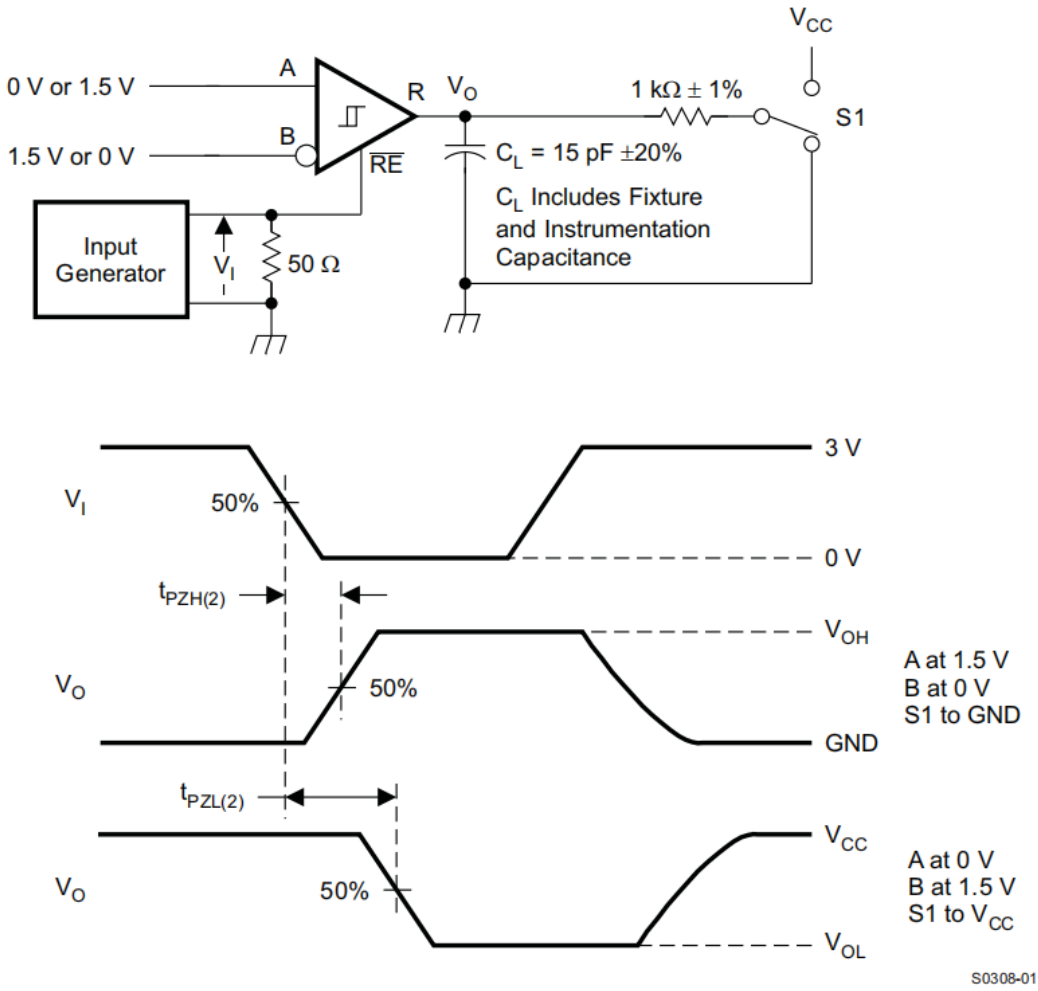


Figure 12. Measurement of Receiver Enable Times With Driver Disabled

8 Detailed Description

8.1 Overview

The SN65HVD82 device is a half-duplex RS-485 transceiver suitable for data transmission at rates up to 250 kbps over controlled-impedance transmission media (such as twisted-pair cabling). The device features a high level of internal transient protection, making it able to withstand up ESD strikes up to 12 kV (per IEC 61000-4-2) and EFT transients up to 4 kV (per IEC 61000-4-4) without incurring damage. Up to 256 units of SN65HVD82 may share a common RS-485 bus due to the device's low bus input currents. The device also features a low standby current consumption of 400 nA (typical).

8.2 Functional Block Diagram

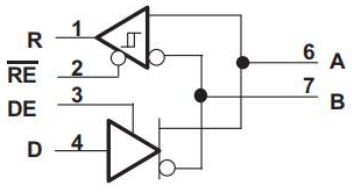


Figure 13. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Receiver Failsafe

The differential receiver is *failsafe* to invalid bus states caused by:

- open bus conditions such as a disconnected connector
- shorted bus conditions such as cable damage shorting the twisted-pair together, or
- idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic High state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds so that the "input indeterminate" range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than 200 mV, and must output a Low when the V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are V_{IT+} and V_{IT-} and V_{HYS}. As seen in the Electrical Characteristics table, differential signals more negative than –200 mV will always cause a Low receiver output. Similarly, differential signals more positive than 200 mV will always cause a High receiver output.

When the differential input signal is close to zero, it will still be above the V_{IT+} threshold, and the receiver output will be High. Only when the differential input is more negative than V_{IT-} will the receiver output transition to a Low state. So the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value V_{HYS} (the separation between V_{IT+} and V_{IT-}) as well as the value of V_{IT+}.

Signals which transition from positive to negative (or from negative to positive) will transition only once, ensuring no spurious bits.

8.3.2 Low-Power Standby Mode

When both the driver and receiver are disabled (DE transitions to a low state and RE transitions to a high state) the device enters standby mode. If the enable inputs are in this state for a brief time (e.g. less than 100 ns), the device does not enter standby mode. This prevents inadvertently entering standby mode during driver/receiver enabling. Only when the enable inputs are held in this state a sufficient duration (e.g. for 300 ns or more), the device is assured to be in standby mode. In this low-power standby mode, most internal circuitry is powered down, and the steady-state supply current is typically less than 400 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

8.4 Device Functional Modes

Table 1. Driver Function Table

INPUT	ENABLE	OUTPUTS		
D	DE	A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus High by default

Table 2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	
$V_{ID} = V_A - V_B$	RE	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

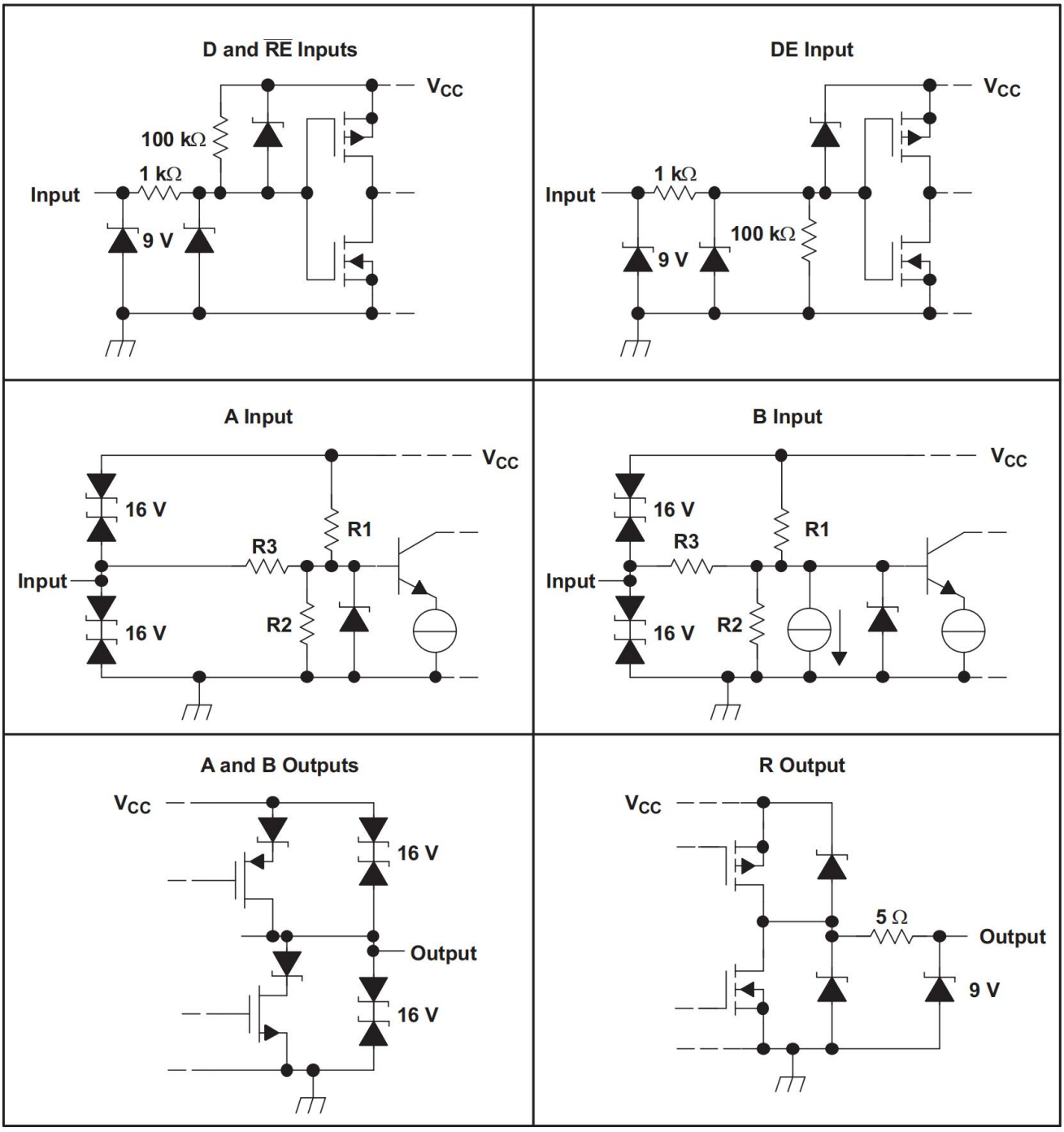
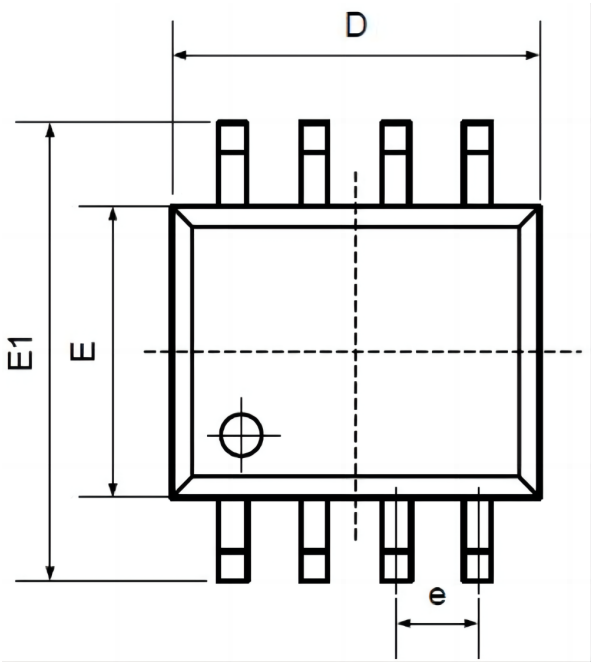


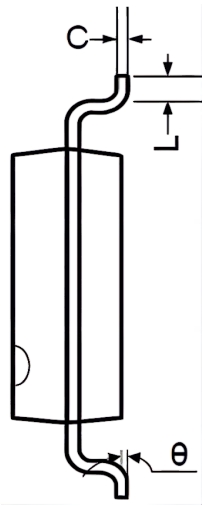
Figure 14. Equivalent Input and Output Schematic Diagrams

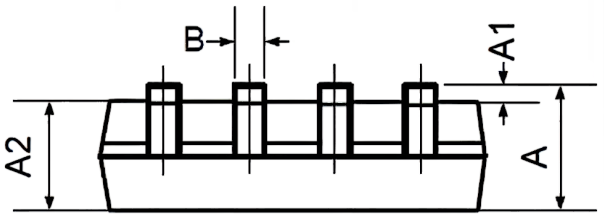
Order information

Order Number	Package	Package Quantity	Marking On The park
SN65HVD82DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD82DR

Package SOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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