SI7322ADN-T1-GE3-VB Datasheet

N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ.)
100	0.036 at V_{GS} = 10 V	21	23 nC
	0.0375 at V_{GS} = 8 V	17	

FEATURES

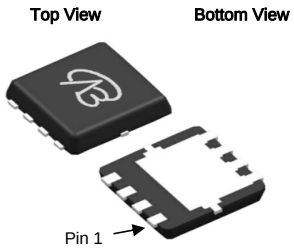
- **Halogen-free According to IEC 61249-2-21 Definition**
- Extremely Low Q_{gd} for Switching Losses
- 100 % R_g Tested
- 100 % Avalanche Tested
- Compliant to RoHS Directive 2002/95/EC

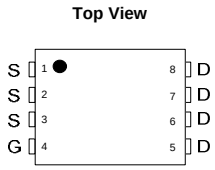
RoHS COMPLIANT
HALOGEN FREE Available

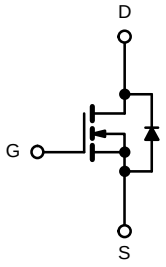
APPLICATIONS

- Primary Side Switch

DFN 3x3







N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	21	A
	T_C = 70 °C		17	
	T_A = 25 °C		15 [b, c]	
	T_A = 70 °C		13 [b, c]	
Pulsed Drain Current		I_{DM}	50	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	4.5	
	T_A = 25 °C		2.6 [b, c]	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	20	
Single Pulse Avalanche Energy		E_{AS}	20	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	5.9	W
	T_C = 70 °C		3.8	
	T_A = 25 °C		3.1 [b, c]	
	T_A = 70 °C		2 [b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b, f]	t ≤ 10 s	R_{thJA}	33	40	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	17	21	

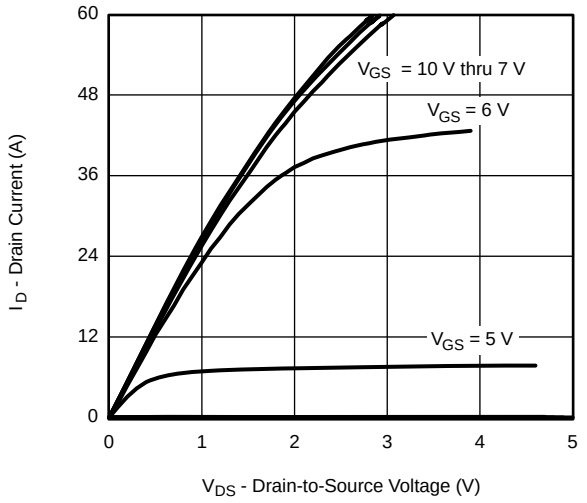
Notes:
a. Based on T_C = 25 °C.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. Maximum under steady state conditions is 80 °C/W.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	100			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		172		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 10		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 250 µA	2.5		4.5	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			1	µA
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 10 V, V_{GS} = 10 V	30			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 5 A		0.036		Ω
		V_{GS} = 8 V, I_D = 5 A		0.0375		
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 5 A		23		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		1735		pF
Output Capacitance	C_{oss}			160		
Reverse Transfer Capacitance	C_{rss}			37		
Total Gate Charge	Q_g	V_{DS} = 75 V, V_{GS} = 10 V, I_D = 5 A		28.5	43	nC
		V_{DS} = 75 V, V_{GS} = 8 V, I_D = 5 A		23	35	
Gate-Source Charge	Q_{gs}			8		
Gate-Drain Charge	Q_{gd}			6.5		
Gate Resistance	R_g	f = 1 MHz		0.85	1.3	Ω
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 50 V, R_L = 10 Ω I_D ≅ 5 A, V_{GEN} = 10 V, R_g = 1 Ω		14	21	ns
Rise Time	t_r			12	18	
Turn-Off Delay Time	$t_{d(off)}$			22	33	
Fall Time	t_f			6	10	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, R_L = 10 Ω I_D ≅ 5 A, V_{GEN} = 8 V, R_g = 1 Ω		16	24	
Rise Time	t_r			12	18	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	t_f			7	12	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			7.7	A
Pulse Diode Forward Current[a]	I_{SM}				50	
Body Diode Voltage	V_{SD}	I_S = 2.6 A		0.77	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 5 A, dI/dt = 100 A/µs, T_J = 25 °C		63	95	ns
Body Diode Reverse Recovery Charge	Q_{rr}			110	165	nC
Reverse Recovery Fall Time	t_a			49		ns
Reverse Recovery Rise Time	t_b			14		

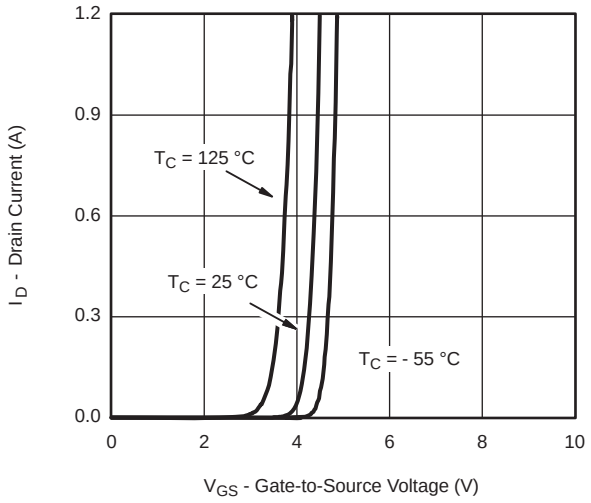
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
a. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

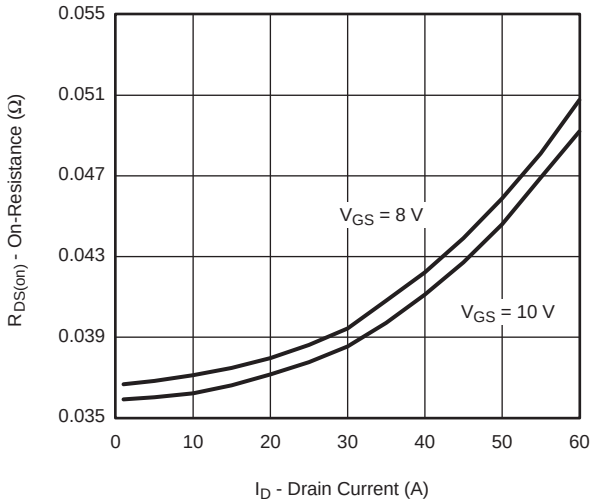
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



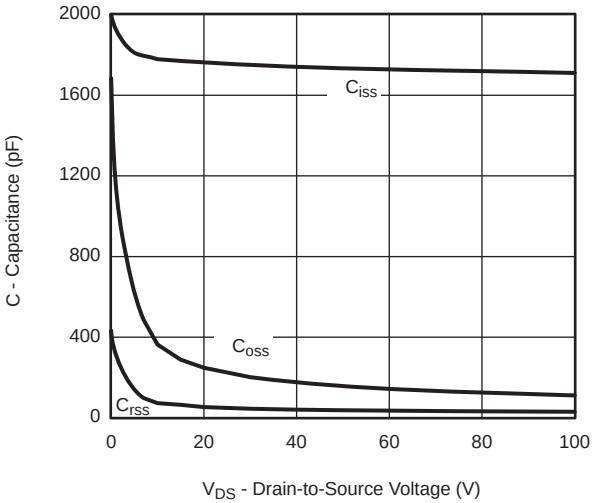
Output Characteristics



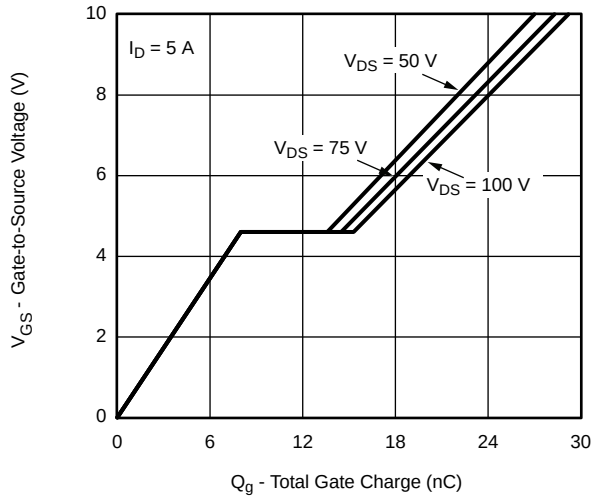
Transfer Characteristics



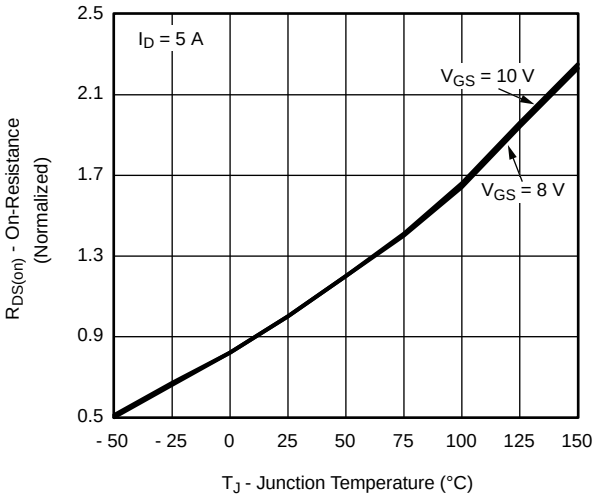
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

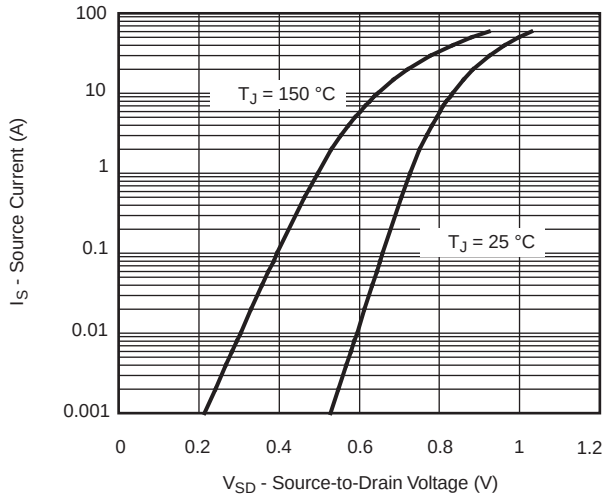


Gate Charge

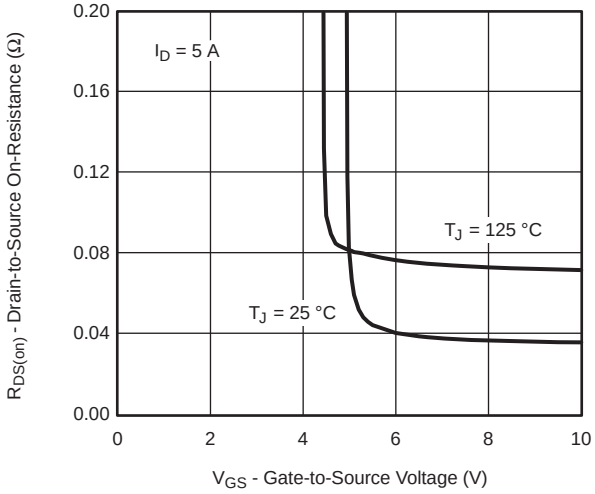


On-Resistance vs. Junction Temperature

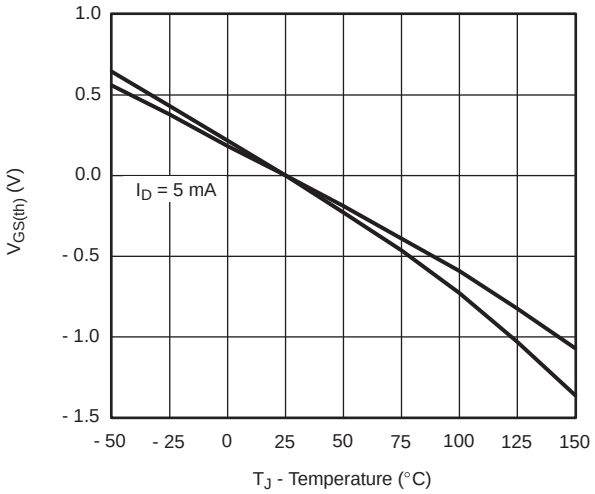
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



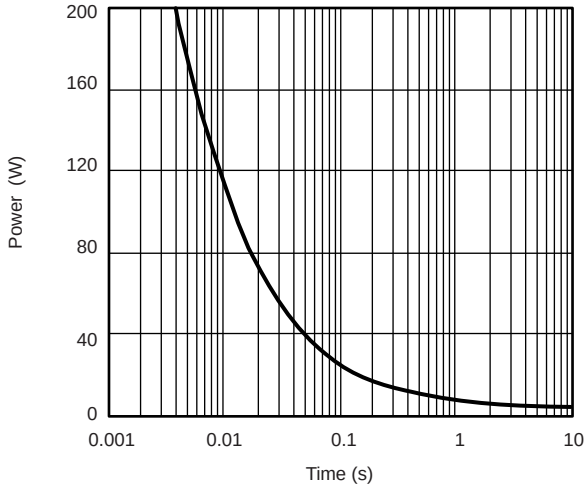
Source-Drain Diode Forward Voltage



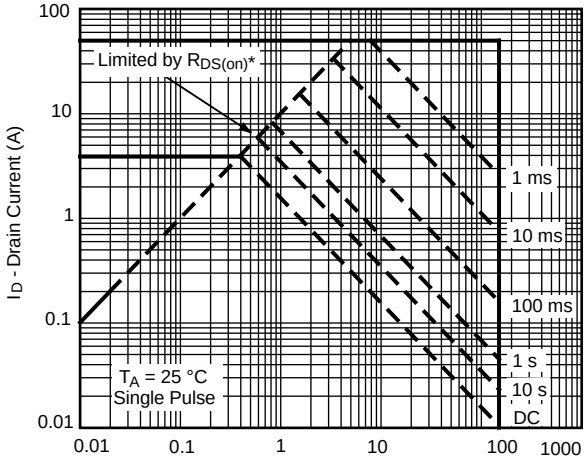
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



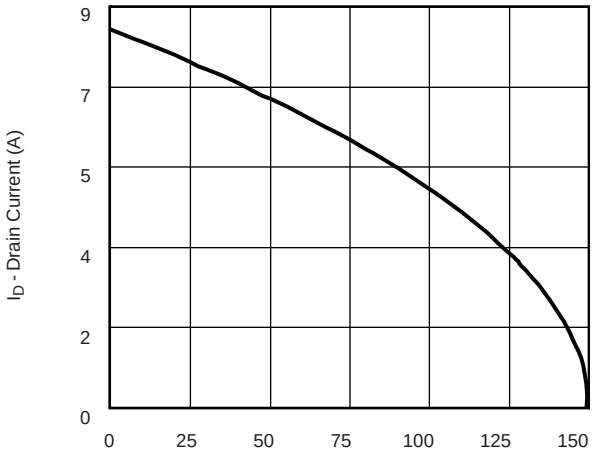
Single Pulse Power, Junction-to-Ambient



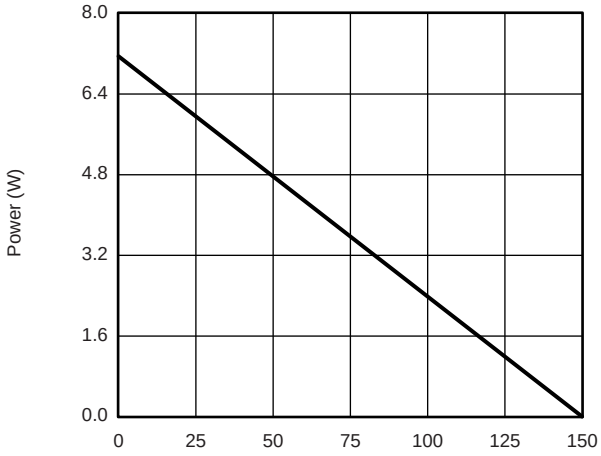
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

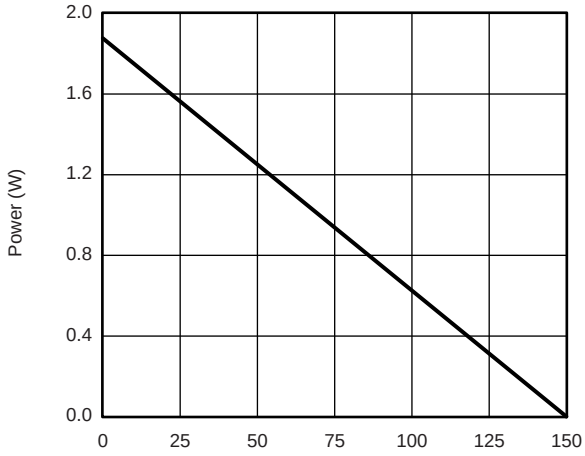
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



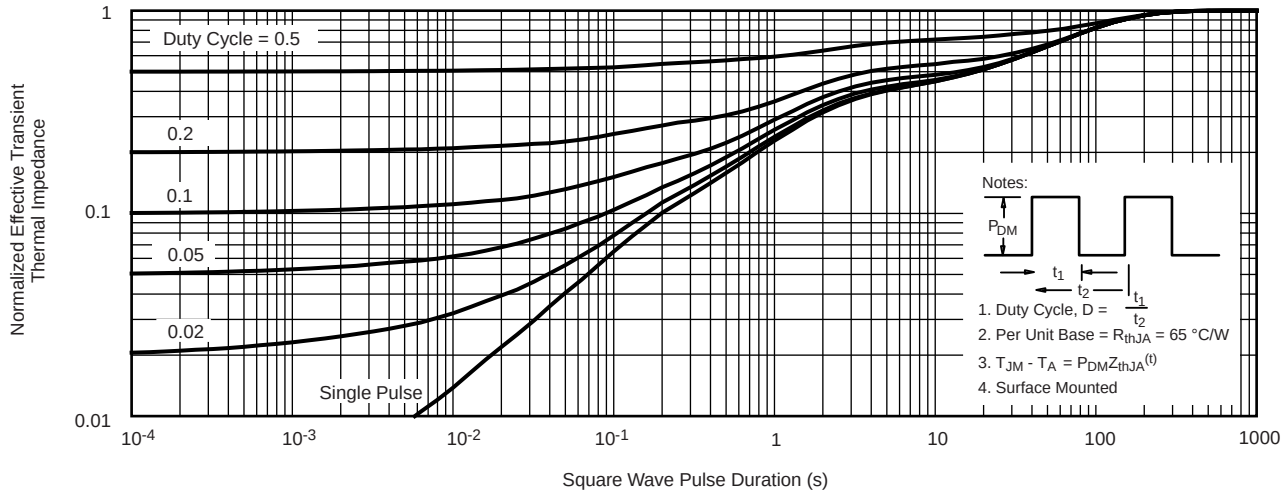
Power, Junction-to-Case



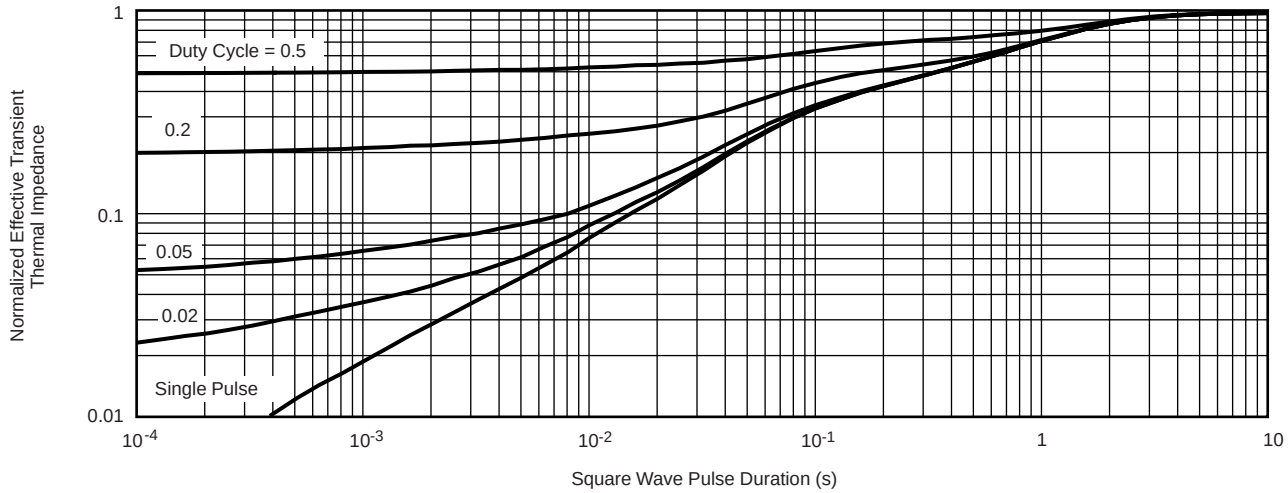
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

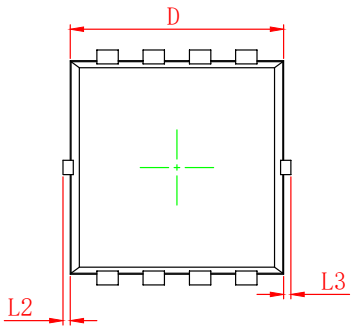


Normalized Thermal Transient Impedance, Junction-to-Ambient

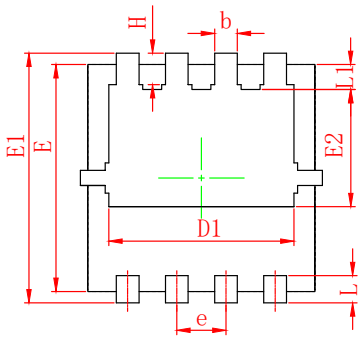


Normalized Thermal Transient Impedance, Junction-to-Foot

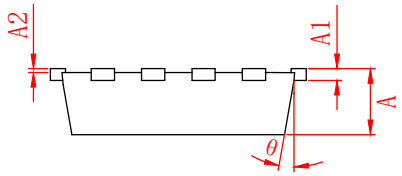
PDFNWB3×3-8L Package Outline Dimensions



Top View
[顶视图]



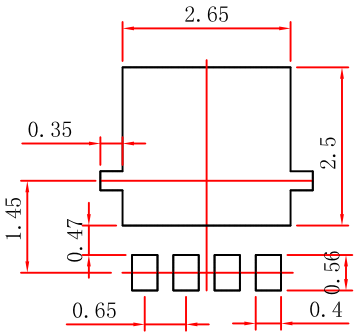
Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.650	0.850	0.026	0.033
A1	0.203REF.		0.008REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.050	2.550	0.081	0.100
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.450	1.650	0.057	0.065
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
Φ	9°	13°	9°	13°

Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

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