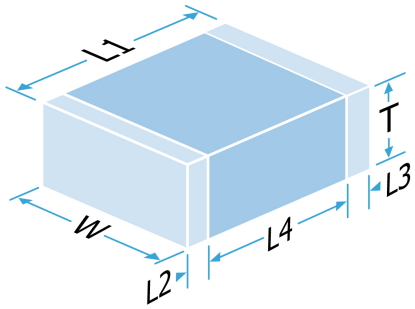
Multilayer Ceramic Chip Capacitor

Part Number: 1808JA250102JGTS2X

Description: 1808 250Vac (X2) 50/60Hz / 1000Vdc 1.0nF ±5% C0G/NP0 (1B)

Approval Specifications:	IEC/EN60384-14:2013+A1 UL60384-14, CAN/CSA E60384-14:14
Certification:	TÜV R60153659 / ID1111233476 UL/cUL E228790-20200917
Classification:	IEC/EN 60384-14:2013+A1 Class X2 UL/cUL FOWX2, FOWX8



Component Marking and Certification Bodies:

Material Group I : CTI >= 600

Mechanical Specification

Size Code	1808
Length (L1) in mm (")	4.5 ± 0.35 (0.180 ± 0.014)
Width (W) in mm (")	2.0 ± 0.30 (0.08 ± 0.012)
Thickness (T) in mm (")	2.0 Max (0.08 Max)
Minimum Termination Band (L2,L3) in mm (")	0.50 (0.020)
Maximum Termination Band (L2,L3) in mm (")	0.80 (0.030)
Minimum Band Gap (L4) in mm (")	3.0 (0.118)
Termination Material	Nickel Barrier, Sn Plated Solder (RoHS compliant)
Solderability	IEC-60068-2-58
Packaging	7" Reel Horizontal Orientation, 1500 per reel

General Electrical Specification

Rated Voltage	Class X2 (250Vac), 50/60Hz, 2.5kV impulse
Humidity Grade	Grade III (IEC/EN60384-14:2013 Annex 1)
Maximum DC Working Voltage	1000Vdc certified / (2500Vdc outside scope of any specification)
Nominal Capacitance Value	1.0nF
Capacitance Tolerance	±5%
Tangent of Loss Angle (Tan δ)	≤0.0015
Capacitance and Tan δ Test Conditions	1.0Vrms @ 1MHz
Voltage Proof (50mA max charging current for DC tests)	100% test: 3000Vdc 1s min / 5s max AQL test: 3225Vdc / 1500Vac 60s min / 2.5kV 1.2x50µs impulse
Min Insulation Resistance (IR)	100.00GOhm @ 100Vdc
Dielectric Classification	C0G/NP0 (1B)
Rated Temperature Range	-55°C / +125°C
Maximum Capacitance Change over Temperature Range	No DC Voltage 0±30ppm/°C Rated DC Voltage -
Climatic Category (IEC)	55/125/56
Ageing Characteristic	Zero

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Data is correct to the best of our knowledge, errors and omissions excepted.

Date: Thursday, September 02, 2021

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Multilayer Ceramic Chip Capacitor

Part Number: 1808JA250102JGTS2X	**Description:** 1808 250Vac (X2) 50/60Hz / 1000Vdc 1.0nF ±5% C0G/NP0 (1B)

Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU	Compliant
REACH Compliant	211 compliant
California Proposition 65	No exposure risk

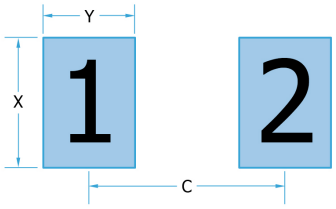
Board Layout

Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover. Refer to application note AN0043 for further information.

IPC-7351 pad design

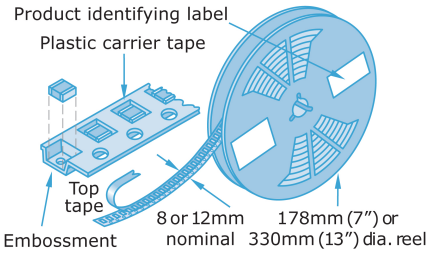
	1808	
C	4.10mm	0.161"
Y	1.50mm	0.059"
X	2.30mm	0.091"



Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.

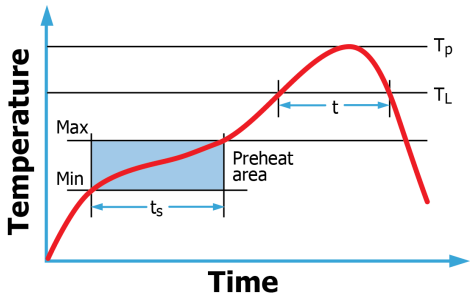


Soldering

Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness >1.0mm. Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.



Application notes with mounting and handling guidance are available on request.

Compex DLI Johanson MFG Novacap Syfer Voltronics

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