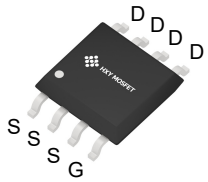
# FDS8876-F40

N-Channel Enhancement Mode MOSFET

## Description

The FDS8876-F40 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



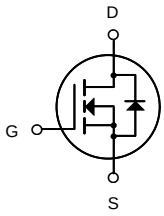

SOP-8

## General Features

$V_{DS}$ = 30V $I_D$ = 18A

$R_{DS(ON)}$ < 6.5mΩ @ $V_{GS}$=10V

$R_{DS(ON)}$ < 12mΩ @ $V_{GS}$=4.5V




N-Channel MOSFET

## Application

Battery protection

Load switch

Uninterruptible power supply

## Package Marking and Ordering Information

| Product ID | Pack | Brand | Qty(PCS) |
|---|---|---|---|
| FDS8876-F40 | SOP-8 | HXY MOSFET | 3000 |

## Absolute Maximum Ratings ($T_C$=25°C unless otherwise noted)

| Symbol | Parameter | Limit | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage | 30 | V |
| $V_{GS}$ | Gate-Source Voltage | ±20 | V |
| $I_D$ | Drain Current-Continuous | 18 | A |
| $I_D$ (70°C) | Drain Current-Continuous($T_C$=70°C) | 8.2 | A |
| $I_{DM}$ | Pulsed Drain Current | 42 | A |
| $P_D$ | Maximum Power Dissipation | 1.5 | W |
| $T_J$,$T_{STG}$ | Operating Junction and Storage Temperature Range | -55 To 150 | °C |
| $R_{\theta JC}$ | Thermal Resistance,Junction-to-Case(Note 2) | 36 | °C/W |

## Electrical Characteristics ($T_J$=25°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V , $I_D$=250uA | 30 | --- | --- | V |
| $\triangle BV_{DSS}/\triangle T_J$ | BVDSS Temperature Coefficient | Reference to 25°C , $I_D$=1mA | --- | 0.027 | --- | V/°C |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance[2] | $V_{GS}$=10V , $I_D$=10A | --- | 5.5 | 6.5 | mΩ |
| | | $V_{GS}$=4.5V , $I_D$=8A | --- | 9 | 12 | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS}$=$V_{DS}$ , $I_D$ =250uA | 1.2 | 1.5 | 2.5 | V |
| $\triangle V_{GS(th)}$ | $V_{GS(th)}$ Temperature Coefficient | | --- | -5.8 | --- | mV/°C |
| $I_{DSS}$ | Drain-Source Leakage Current | $V_{DS}$=24V , $V_{GS}$=0V , $T_J$=25°C | --- | --- | 1 | uA |
| | | $V_{DS}$=24V , $V_{GS}$=0V , $T_J$=55°C | --- | --- | 5 | |
| $I_{GSS}$ | Gate-Source Leakage Current | $V_{GS}$=±20V , $V_{DS}$=0V | --- | --- | ±100 | nA |
| gfs | Forward Transconductance | $V_{DS}$=5V , $I_D$=10A | --- | 5.8 | --- | S |
| $R_g$ | Gate Resistance | $V_{DS}$=0V , $V_{GS}$=0V , f=1MHz | --- | 2.2 | 3.8 | Ω |
| $Q_g$ | Total Gate Charge (4.5V) | $V_{DS}$=15V , $V_{GS}$=4.5V , $I_D$=10A | --- | 12.6 | 17.6 | nC |
| $Q_{gs}$ | Gate-Source Charge | | --- | 4.2 | 5.9 | |
| $Q_{gd}$ | Gate-Drain Charge | | --- | 5.1 | 7.1 | |
| $T_{d(on)}$ | Turn-On Delay Time | $V_{DD}$=15V , $V_{GS}$=10V , $R_G$=3.3Ω $I_D$=10A | --- | 6.2 | 12.4 | ns |
| $T_r$ | Rise Time | | --- | 59 | 106 | |
| $T_{d(off)}$ | Turn-Off Delay Time | | --- | 27.6 | 55 | |
| $T_f$ | Fall Time | | --- | 8.4 | 16.8 | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$=15V, $V_{GS}$=0V, f=1MHz | --- | 1317 | 1845 | pF |
| $C_{oss}$ | Output Capacitance | | --- | 163 | 228.2 | |
| $C_{rss}$ | Reverse Transfer Capacitance | | --- | 131 | 183.4 | |
| $I_S$ | Continuous Source Current[1,5] | $V_G$=$V_D$=0V, Force Current | --- | --- | 18 | A |
| $I_{SM}$ | Pulsed Source Current[2,5] | | --- | --- | 42 | A |
| $V_{SD}$ | Diode Forward Voltage[2] | $V_{GS}$=0V, $I_S$=1A, $T_J$=25°C | --- | --- | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | IF=10A, dI/dt=100A/μs, $T_J$=25°C | --- | 12.5 | --- | nS |
| $Q_{rr}$ | Reverse Recovery Charge | | --- | 5 | --- | nC |

Note :
1.The data tested by surface mounted on a 1 inch$^2$ FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is $V_{DD}$=25V,$V_{GS}$=10V,L=0.1mH,$I_{AS}$=35A
4.The power dissipation is limited by 150℃ junction temperature
5.The data is theoretically the same as $I_D$ and $I_{DM}$ , in real applications , should be limited by total power dissipation.

## Typical Characteristics

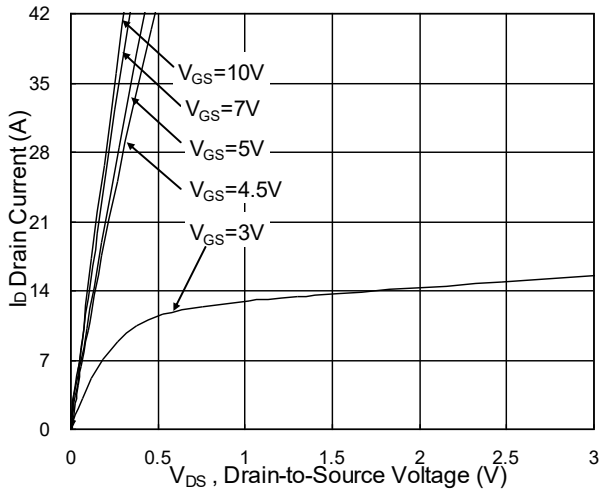



**Fig.1 Typical Output Characteristics**

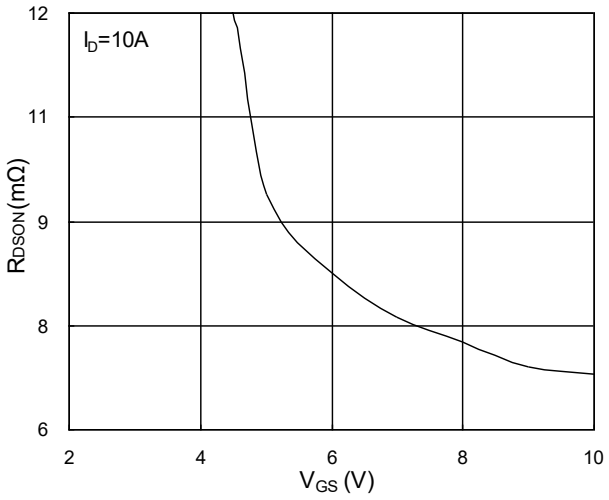



**Fig.2 On-Resistance vs. Gate-Source**

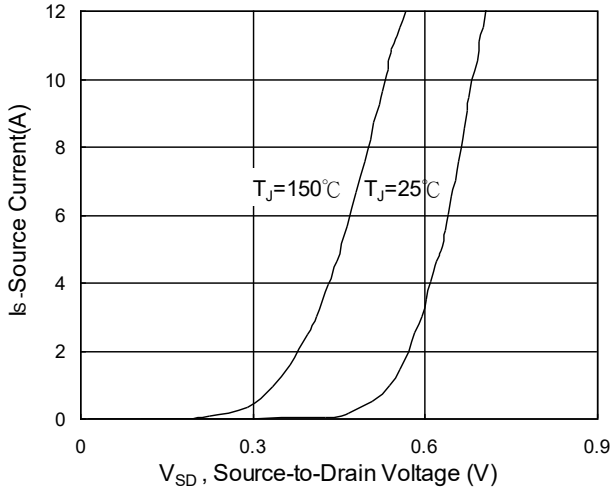



**Fig.3 Forward Characteristics of reverse**

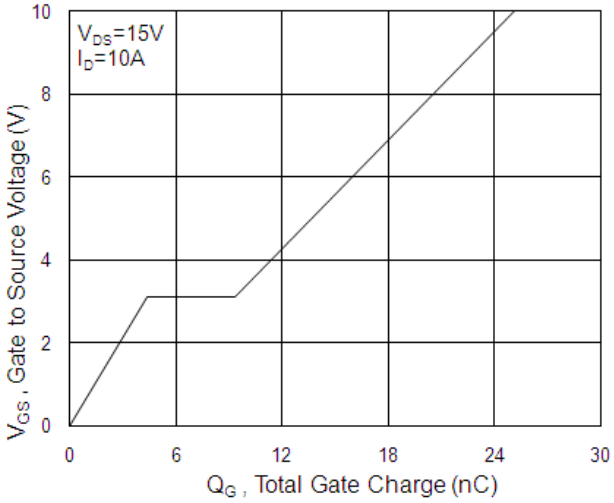



**Fig.4 Gate-Charge Characteristics**

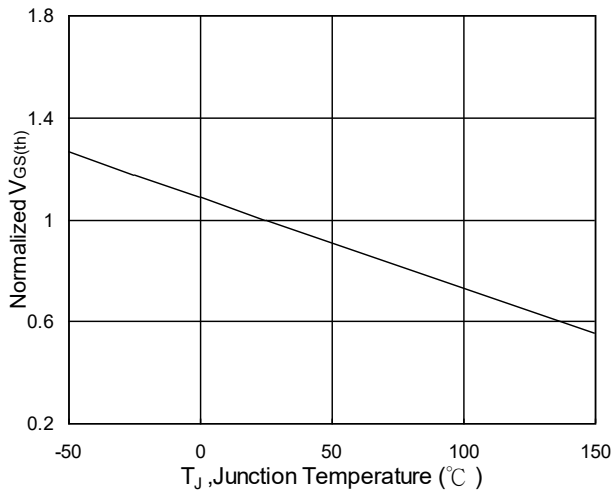



**Fig.5 Normalized $V_{GS(th)}$ vs. $T_J$**

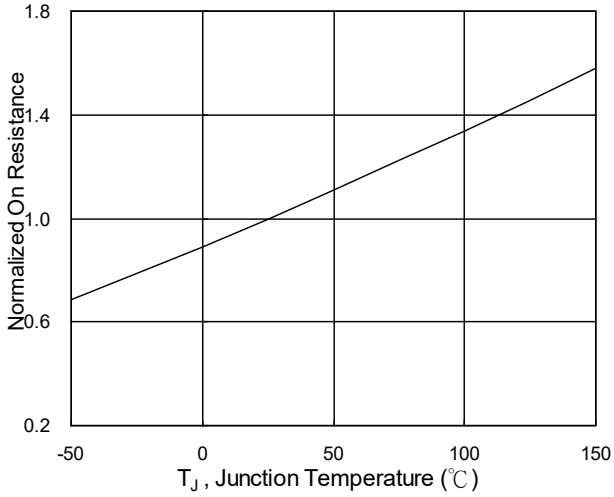



**Fig.6 Normalized $R_{DSON}$ vs. $T_J$**

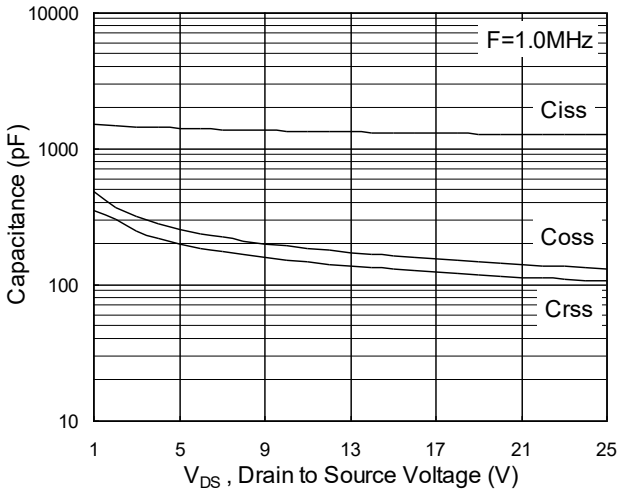



**Fig.7 Capacitance**

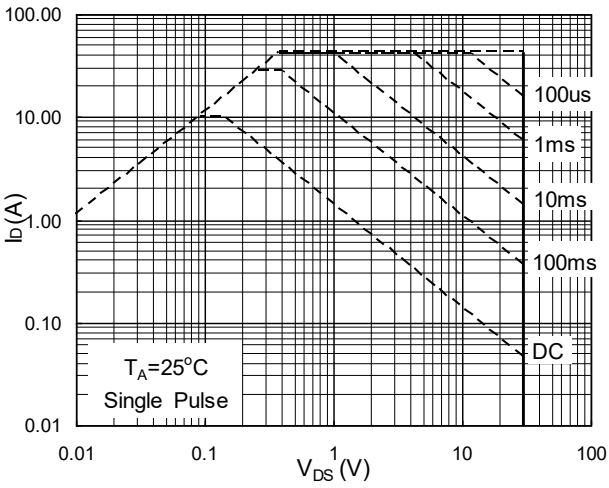



**Fig.8 Safe Operating Area**

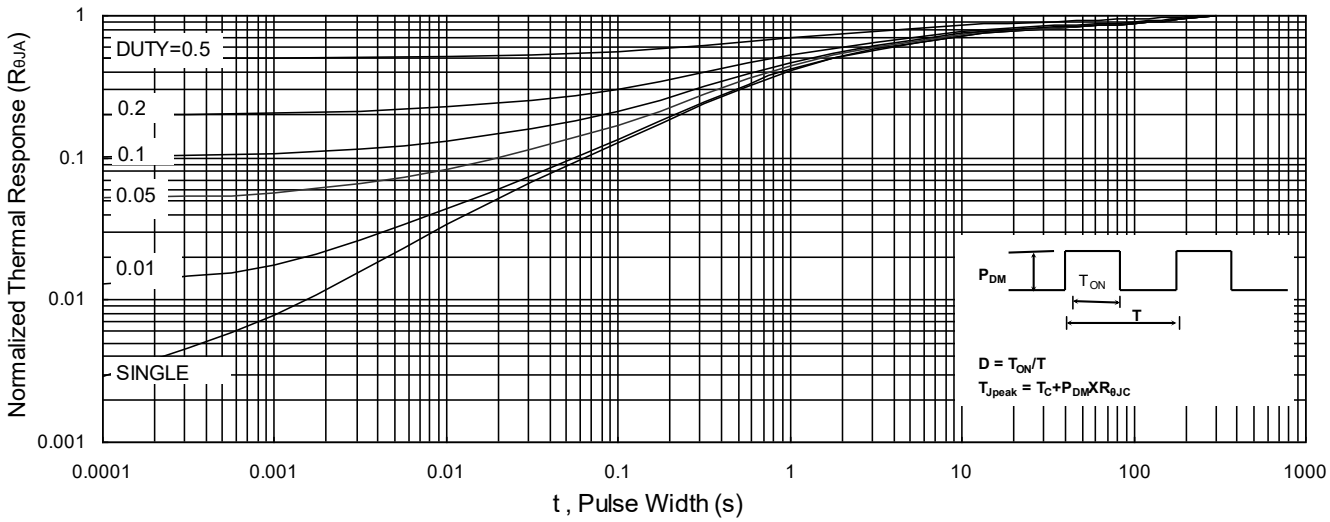



**Fig.9 Normalized Maximum Transient Thermal Impedance**

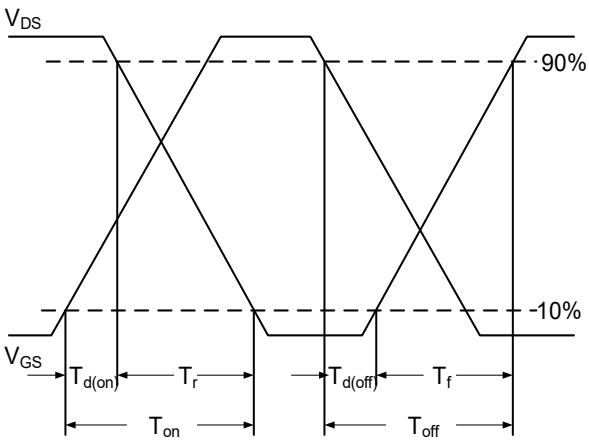



**Fig.10 Switching Time Waveform**

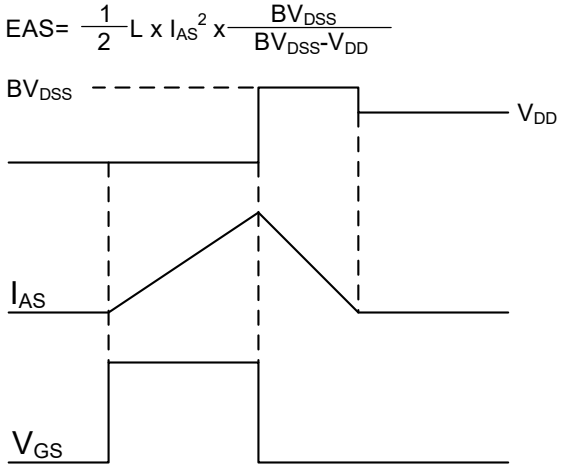
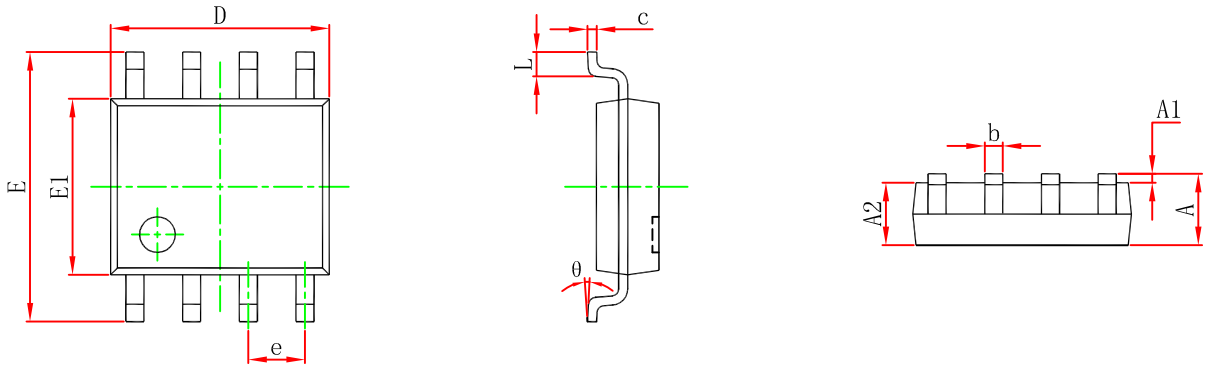
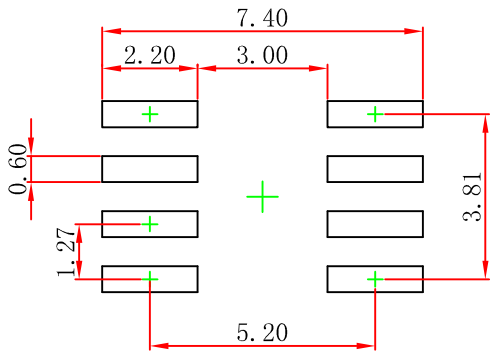



**Fig.11 Unclamped Inductive Switching Waveform**

## SOP-8 Package Outline Dimensions




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | **Min** | **Max** | **Min** | **Max** |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.007 | 0.010 |
| D | 4.800 | 5.000 | 0.189 | 0.197 |
| e | 1.270 (BSC) | | 0.050 (BSC) | |
| E | 5.800 | 6.200 | 0.228 | 0.244 |
| E1 | 3.800 | 4.000 | 0.150 | 0.157 |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |




Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

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