SIRS4301DP-T1-GE3-VB Datasheet

P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 30	0.0022 at V_{GS} = - 10 V	- 120	80 nC
	0.0035 at V_{GS} = - 4.5 V	- 100	

FEATURES

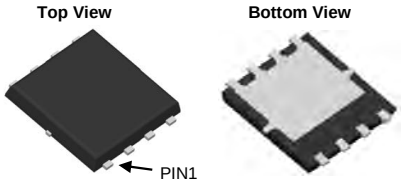
- **Halogen-free**
- Trench Power MOSFET
- 100 % R_g Tested

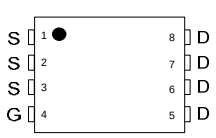
RoHS COMPLIANT

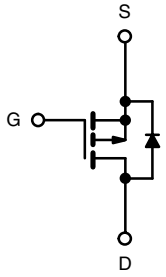
APPLICATIONS

- Notebook
  - Load Switch

DFN5X6







P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	- 120	A
	T_C = 70 °C		- 95	
	T_A = 25 °C		- 60.6[b, c]	
	T_A = 70 °C		- 30[b, c]	
Pulsed Drain Current		I_{DM}	- 360	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	- 60[a]	
	T_A = 25 °C		- 5.6[b, c]	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	- 40	
Single Pulse Avalanche Energy		E_{AS}	80	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	104	W
	T_C = 70 °C		66.6	
	T_A = 25 °C		6.25[b, c]	
	T_A = 70 °C		4.0[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)[d, e]			260	

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b, f]	t ≤ 10 s	R_{thJA}	15	20	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	0.9	1.2	

Notes:

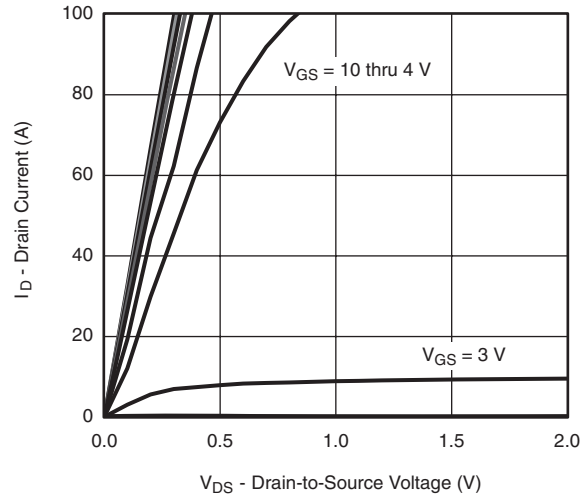
a. Package limited.
b. Surface Mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. The DFN5x6 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under Steady State conditions is 54 °C/W.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 31		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			6.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 1.0		- 2 .0	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 30 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 30 V, V_{GS} = 0 V, T_J = 55 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = - 5 V, V_{GS} = - 10 V	- 30			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 20 A		0.0022		Ω
		V_{GS} = - 4.5 V, I_D = - 15 A		0.0035		
Forward Transconductance[a]	g_{fs}	V_{DS} = - 15 V, I_D = - 20 A		95		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 15 V, V_{GS} = 0 V, f = 1 MHz		13700		pF
Output Capacitance	C_{oss}			1215		
Reverse Transfer Capacitance	C_{rss}			1125		
Total Gate Charge	Q_g	V_{DS} = - 15 V, V_{GS} = - 10 V, I_D = - 20 A		167	250	nC
		V_{DS} = - 15 V, V_{GS} = - 4.5 V, I_D = - 20 A		78	120	
Gate-Source Charge	Q_{gs}			27		
Gate-Drain Charge	Q_{gd}			35		
Gate Resistance	R_g	f = 1 MHz		1.7		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 15 V, R_L = 15 Ω $I_D \cong$ - 1.0 A, V_{GEN} = - 10 V, R_g = 1 Ω		25	40	ns
Rise Time	t_r			15	30	
Turn-Off Delay Time	$t_{d(off)}$			110	170	
Fall Time	t_f			30	50	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 15 V, R_L = 15 Ω $I_D \cong$ - 1.0 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		110	170	
Rise Time	t_r			100	150	
Turn-Off Delay Time	$t_{d(off)}$			100	150	
Fall Time	t_f			50	75	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			120	A
Pulse Diode Forward Current[a]	I_{SM}				360	
Body Diode Voltage	V_{SD}	I_S = - 5 A		- 0.74	- 1.1	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 3.5 A, dI/dt = 100 A/µs, T_J = 25 °C		50	100	ns
Body Diode Reverse Recovery Charge	Q_{rr}			65	130	nC
Reverse Recovery Fall Time	t_a			26		ns
Reverse Recovery Rise Time	t_b			24		

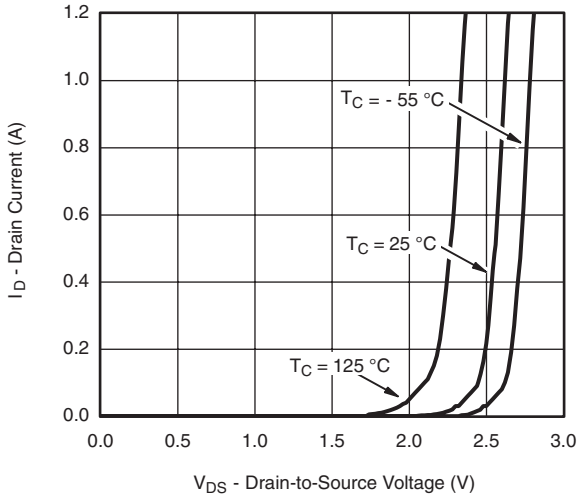
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

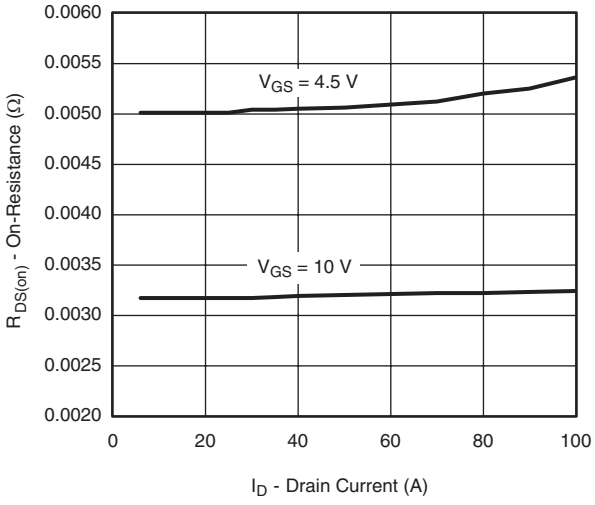
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



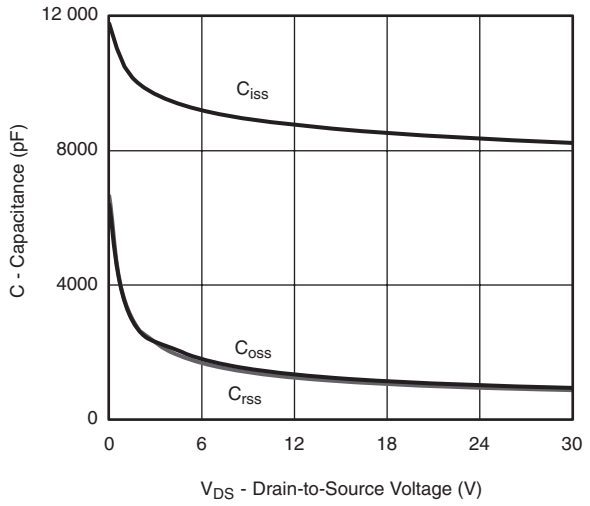
Output Characteristics



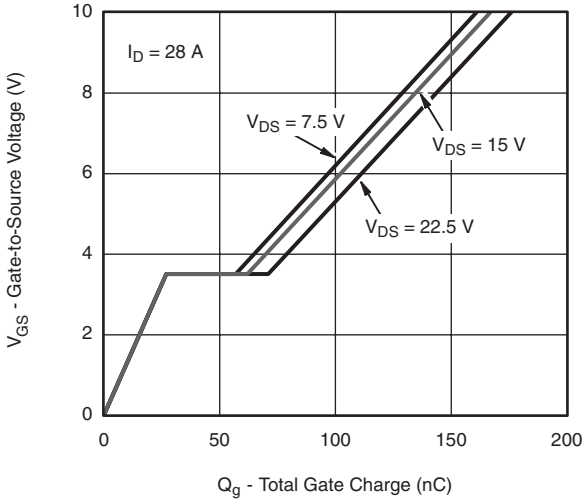
Transfer Characteristics



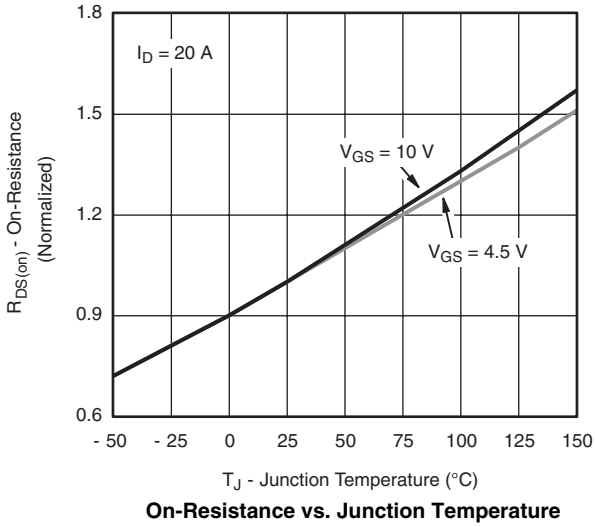
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

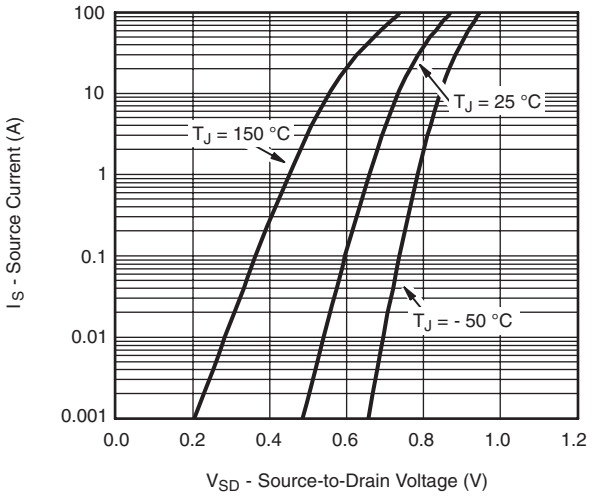


Gate Charge

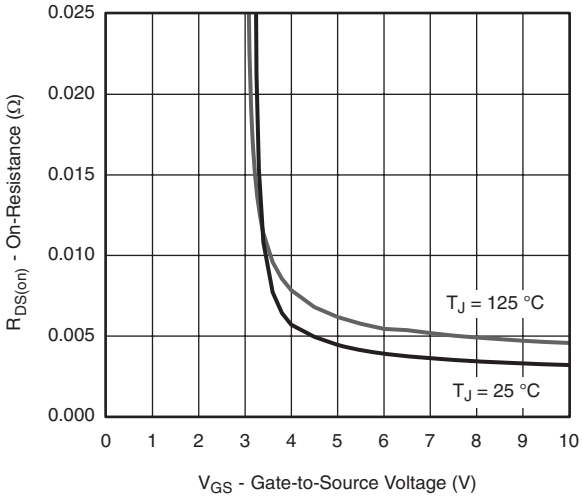


On-Resistance vs. Junction Temperature

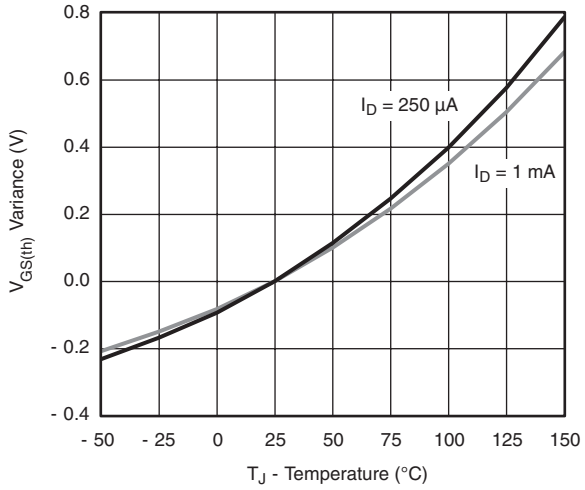
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



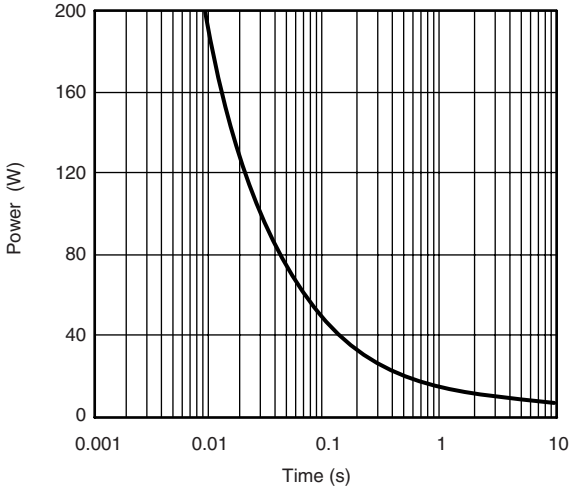
Source-Drain Diode Forward Voltage



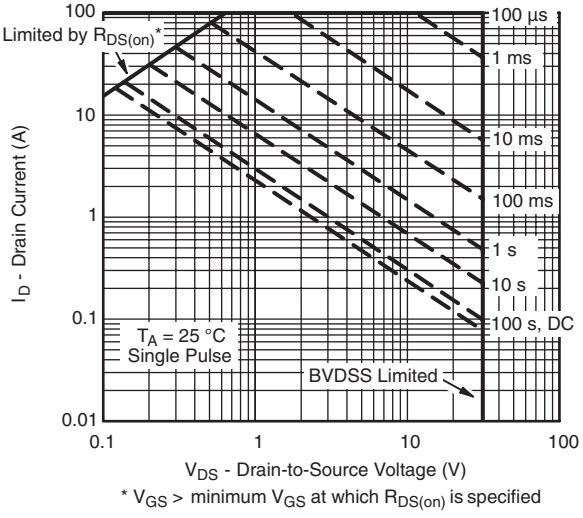
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



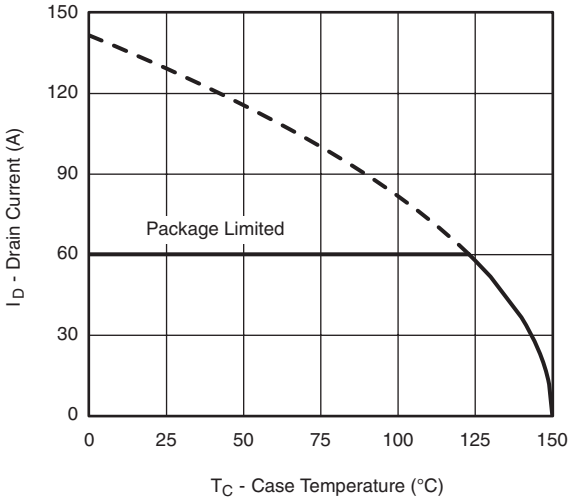
Single Pulse Power, Junction-to-Ambient



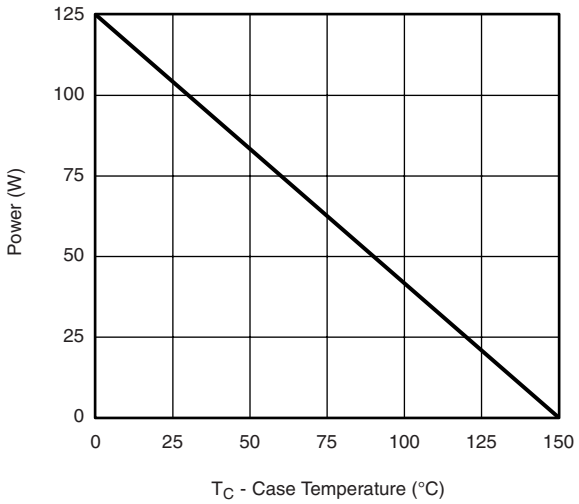
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

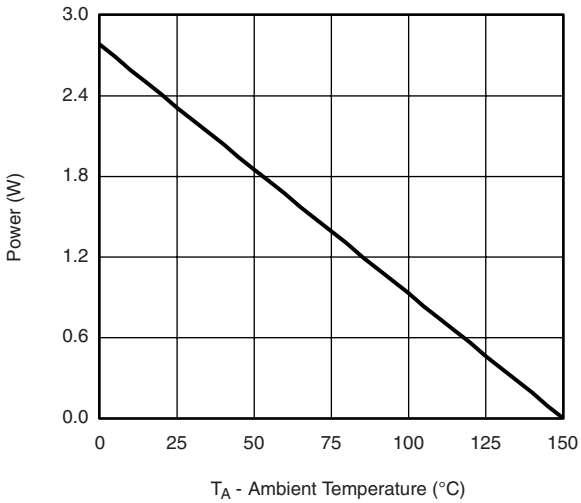
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



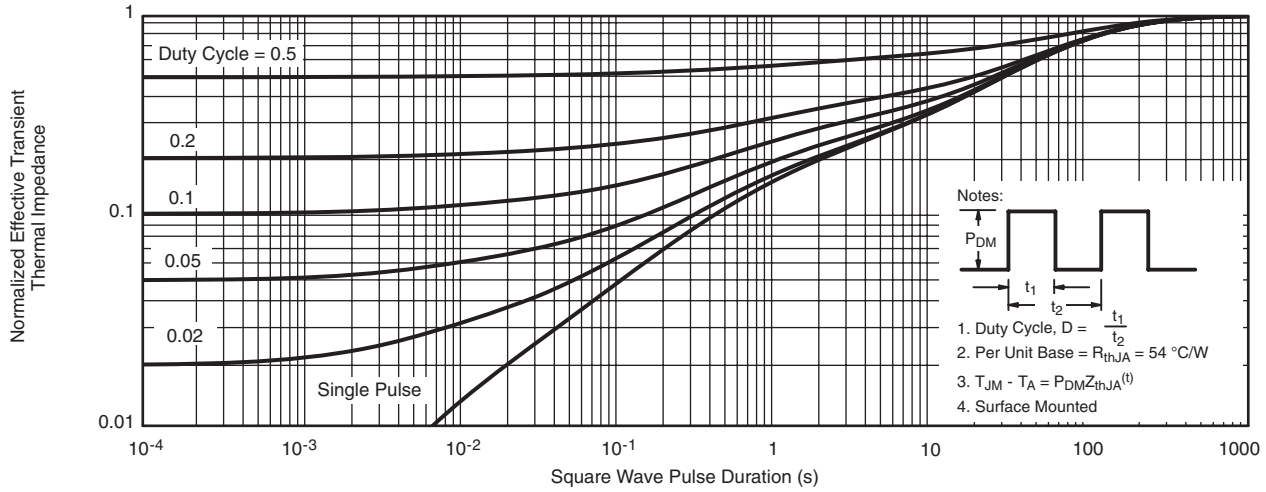
Power, Junction-to-Case



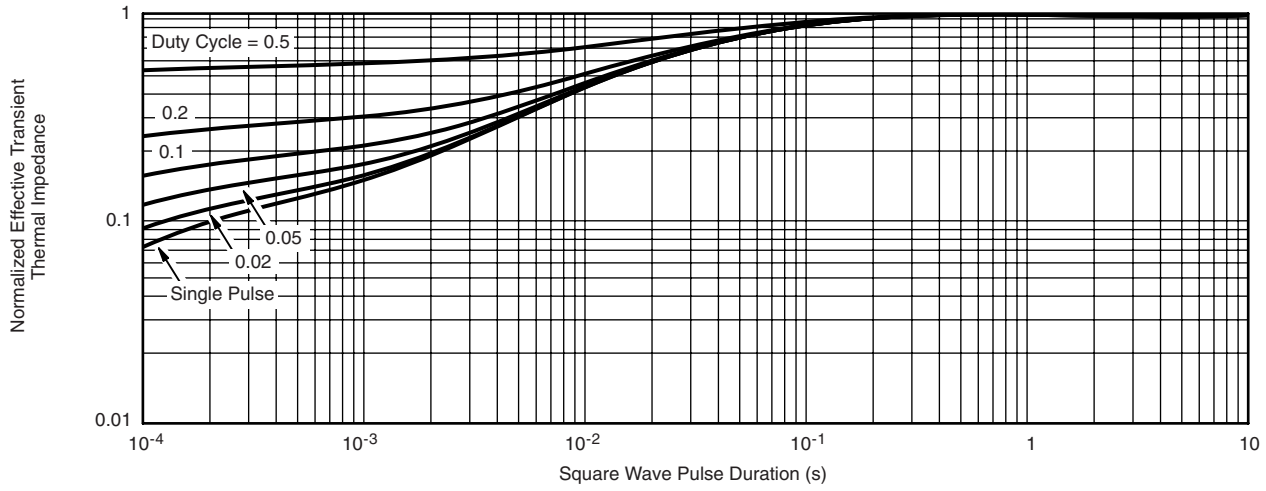
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

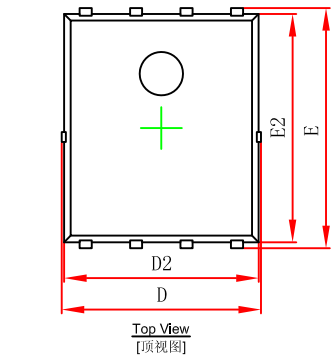


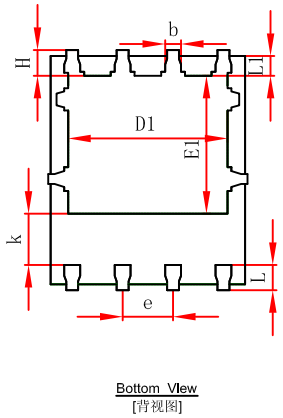
Normalized Thermal Transient Impedance, Junction-to-Ambient

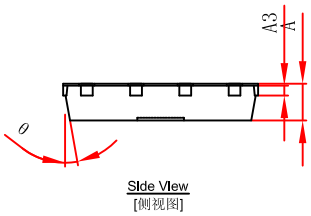


Normalized Thermal Transient Impedance, Junction-to-Case

PDFNWB5x6-8L Package Outline Dimensions

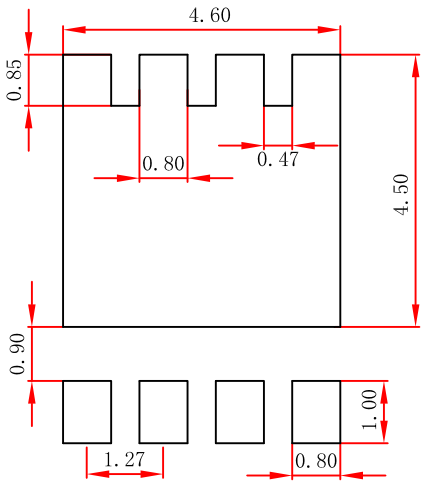






Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

PDFNWB5x6-8L Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

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