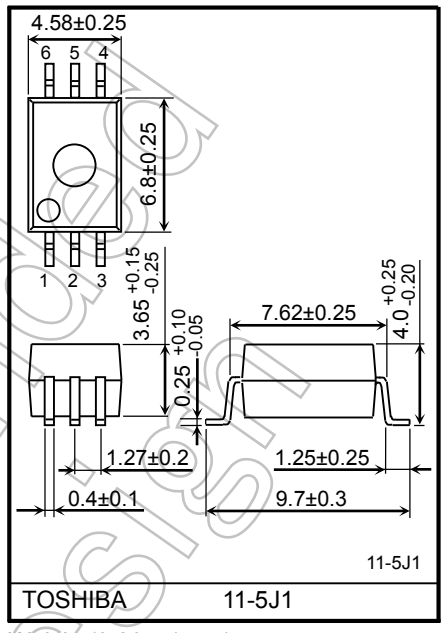
TOSHIBA Photocoupler GaAℓAs IRED & Photo-IC

TLP716

Unit: mm



Weight: 0.26 g (typ.)

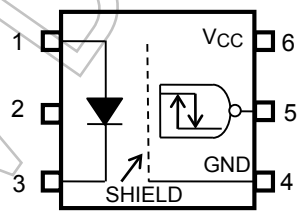
Plasma display panel
High Speed Interface
Factory Automation

The TOSHIBA TLP716 consists of a GaAℓAs light emitting diode and a high speed photodetector. This unit is 6-lead SDIP. TLP716 is 50% smaller than 8PIN DIP and has suited the safety standard reinforced insulation class. So, mounting area in safety standard required equipment can be reduced.

- Inverter Logic (totempole output)
- Package Type : SDIP6
- Guaranteed Performance Over Temperature : -40 to 100°C
- Power Supply Voltage: 4.5 to 5.5 V
- Input Thresholds Current: I_{FHL} = 6.5 mA (max)
- Propagation delay Time (t_{pHL}/t_{pLH}): 75 ns (max)
- Switching speed: 15 MBd (typ.)
- Common mode transient immunity: ±10 kV/μs (min)
- Isolation voltage: 5000 Vrms (min)
- UL approved : UL1577, File No.E67349
- c-UL approved : CSA Component Acceptance Service No. 5A, File No.E67349
- Option (D4) VDE approved : EN60747-5-5 EN60065 EN60950-1(Note 1) EN62368-1(Pending)

Note 1: When a EN60747-5-5 approved type is needed, please designate "Option(D4)"

Pin Configuration (Top View)

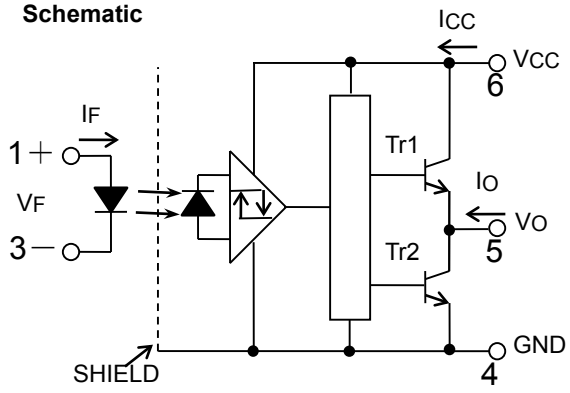


1: ANODE
2: N.C.
3: CATHODE
4: GND
5: V_O
6: V_{CC}

- Construction Mechanical Rating

Creepage Distance	7.0 mm (min)
Clearance	7.0 mm (min)
Insulation Thickness	0.4 mm (min)

Schematic



Note: 0.1 μF bypass capacitor must be connected between pins 6 and 4.

Truth Table

Input	LED	Tr1	Tr2	Output
H	ON	OFF	ON	L
L	OFF	ON	OFF	H

Start of commercial production
2006-06

Not Recommended for New Design

Absolute Maximum Ratings (Ta=25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current (Ta ≤ 85°C)	I_F	20	mA
	Forward Current Derating (Ta > 85°C)	$\Delta I_F/\Delta Ta$	-0.5	mA/°C
	Peak Transient Forward Current (Note1)	I_{FPT}	1	A
	Reverse Voltage	V_R	5	V
	Diode power dissipation	P_D	40	mW
	Diode power dissipation derating (Ta >85°C)	$\Delta P_D/\Delta Ta$	-1.0	mW/°C
	Junction Temperature	T_j	125	°C
DETECTOR	Output Current (Ta ≤ 85°C)	I_O	10	mA
	Output Current Derating (Ta > 85°C)	$\Delta I_O/\Delta Ta$	-0.25	mA/°C
	Output Voltage ($V_O \leq V_{CC}$)	V_O	-0.5 to 6	V
	Supply Voltage	V_{CC}	-0.5 to 6	V
	Power Dissipation (Ta ≤ 85°C)	P_C	40	mW
	Power Dissipation Derating (Ta > 85°C)	$\Delta P_C/\Delta Ta$	-1.0	mW/°C
	Junction Temperature	T_j	125	°C
Operating Temperature Range		T_{opr}	-40 to 100	°C
Storage Temperature Range		T_{stg}	-55 to 125	°C
Lead Solder Temperature(10 s)		T_{sol}	260	°C
Isolation Voltage (AC, 60 s, R.H. ≤ 60%) (Note2)		BV_S	5000	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Pulse width PW ≤ 1 μs, 300 pps.

Note 2: Device Considered a two terminal device: pins 1, 2 and 3 shorted together and pins 4, 5 and 6 shorted together.

Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT
Input Current, ON	$I_{F(ON)}$	8	12	18	mA
Input Voltage, OFF	$V_{F(OFF)}$	0	—	0.8	V
Supply Voltage (Note1)(Note2)(Note 3)	V_{CC}	4.5	5	5.5	V

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 1: This item denotes operating ranges, not meaning of recommended operating conditions.

Note 2: The detector of this product requires a power supply voltage (V_{CC}) of 4.5 V or higher for stable operation. If the V_{CC} is lower than this value, an I_{CC} may increase, or an output may be unstable. Be sure to use the product after checking the supply current, and the operation of a power-on/-off.

Note 3: A ceramic capacitor (0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

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The correlation between input current and switching speed and drive circuit (reference information)

Input Current (I_F)	TEST CIRCUIT (Psge 4)	Typical Switching Speed
12mA	1	14 – 16 MBd
8mA	1	11 – 13 MBd
8mA	2 (with Speed up capacitor)	16 – 20 MBd

Electrical Characteristics

(Unless otherwise specified, Ta = -40 to 100°C, V_{CC} = 4.5 to 5.5 V)

CHARACTERISTIC	SYMBOL	CONDITION	MIN	TYP.	MAX	UNIT
Input Forward Voltage	V_F	I_F = 10 mA, Ta = 25°C	—	1.65	1.8	V
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta Ta$	I_F = 10 mA	—	-2.0	—	mV/°C
Input Reverse Current	I_R	V_R = 5 V, Ta = 25°C	—	—	10	μA
Input Capacitance	C_T	V = 0 V, f = 1 MHz, Ta = 25°C	—	45	—	pF
Logic Low Output Voltage	V_{OL}	I_{OL} = 1.6 mA, I_F = 12 mA V_{CC} = 5 V	—	—	0.4	V
Logic High Output Voltage	V_{OH}	I_{OH} = -0.02 mA, V_F = 1.05 V V_{CC} = 5 V	4.0	—	—	V
Logic Low Supply Current	I_{CCL}	I_F = 12 mA	—	—	5.0	mA
Logic High Supply Current	I_{CCH}	V_F = 0 V	—	—	5.0	mA
Input Current Logic Low Output	I_{FHL}	I_O = 1.6 mA, V_O < 0.4 V	—	—	6.5	mA
Input Voltage Logic High Output	V_{FLH}	I_O = -0.02 mA, V_O > 4.0 V	0.8	—	—	V

Note: All typical values are at Ta = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 12 mA unless otherwise specified

Isolation Characteristics (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Capacitance input to output	C_S	V_S = 0 V , f = 1 MHz (Note 1)	—	0.8	—	pF
Isolation resistance	R_S	R.H. ≤ 60%, V_S = 500 V (Note 1)	1×10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S	AC, 60 s	5000	—	—	Vrms
		AC, 1 s, in oil	—	10000	—	
		DC, 60 s, in oil	—	10000	—	Vdc

Note 1: Device Considered a two terminal device: pins 1, 2 and 3 shorted together and pins 4, 5 and 6 shorted together.

Not Recommended for New Design

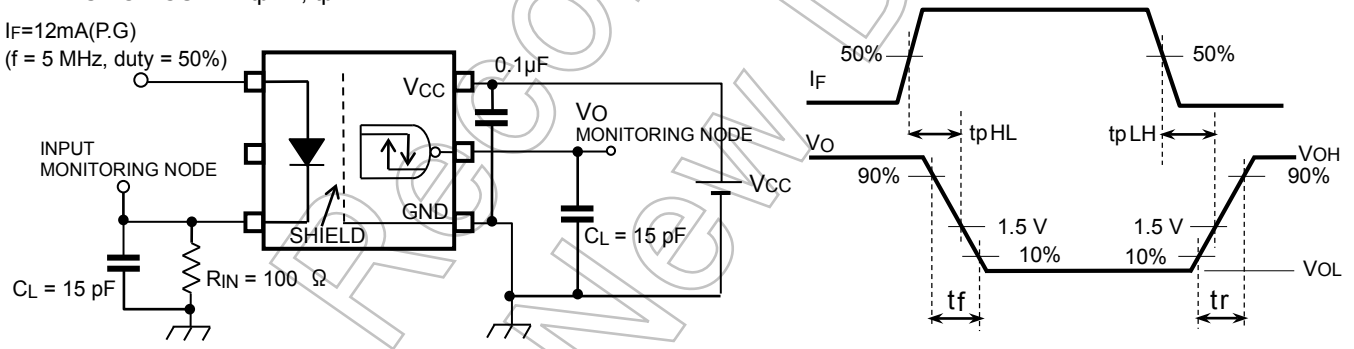
Switching Characteristics
(Unless otherwise specified, Ta = -40 to 100°C, V_{CC} = 4.5 to 5.5 V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION		MIN	TYP.	MAX	UNIT
propagation Delay Time to Logic Low output	tpHL	1	I_F=0→12mA	RIN=100Ω C_L=15pF (Note 1)	—	—	75	ns
propagation Delay Time to Logic High output	tpLH		I_F=12→0mA		—	—	75	ns
propagation Delay Time to Logic Low output	tpHL	2	V_{IN}=0→5V (I_F=0→8mA)	R_{IN}=430Ω C_{IN}=33pF C_L=15pF (Note 1)	—	—	65	ns
propagation Delay Time to Logic High output	tpLH		V_{IN}=5→0V (I_F=8→0mA)		—	—	65	ns
Switching Time Dispersion between ON and OFF	| tpLH - tpHL |	1	I_F=12mA, R_{IN}=100Ω, C_L=15pF (Note 1)		—	—	45	ns
Output Fall Time (90 to 10%)	t_f		I_F=0→12mA	R_{IN}=100Ω C_L=15pF (Note 1)	—	15	—	ns
Output Rise Time (10 to 90%)	t_r		I_F=12→0mA		—	15	—	ns
Common Mode transient Immunity at High Level Output	CM_H	3	V_{CM}=1000Vp-p, I_F=0mA, $V_{O(Min)}$=4V, Ta=25°C		10000	—	—	V/μs
Common Mode transient Immunity at Low Level Output	CM_L		V_{CM}=1000Vp-p, I_F=12mA, $V_{O(Max)}$=0.4V, Ta=25°C		-10000	—	—	V/μs

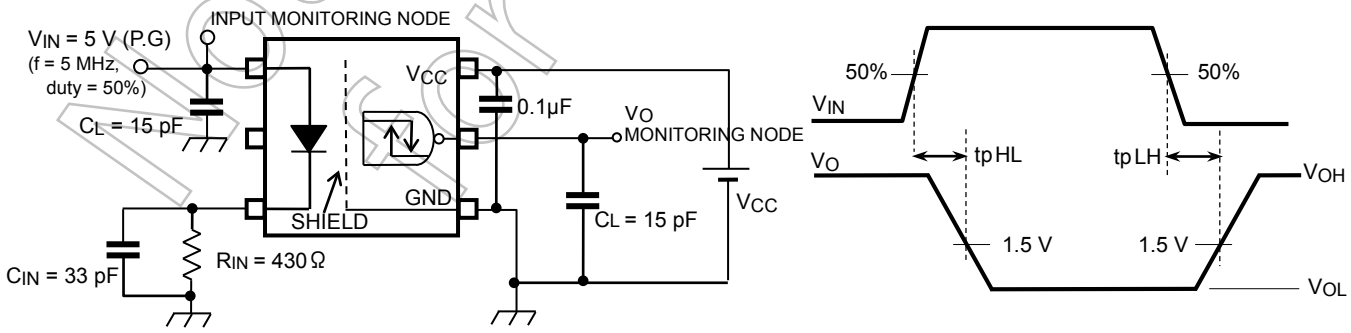
Note: All typical values are at Ta = 25°C

Note 1: C_L is approximately 15pF which includes probe and Jig/stray wiring capacitance.

TEST CIRCUIT 1: tpLH, tpHL



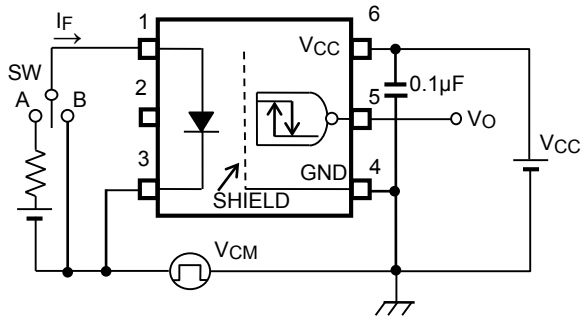
TEST CIRCUIT 2: tpLH, tpHL

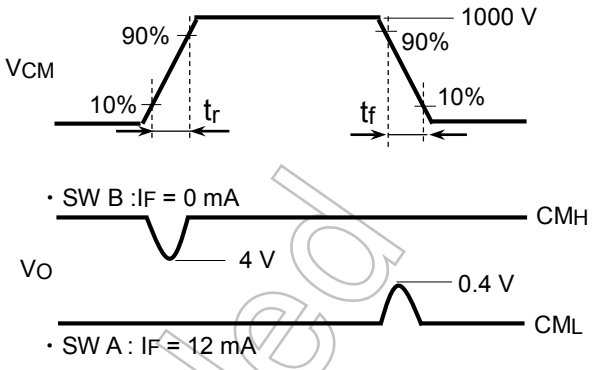


The PROBE and JIG capacitances are included in C_L.
(P.G) : Pulse Generatior

Not Recommended for New Design

TEST CIRCUIT 3: Common-Mode Transient Immunity Test Circuit





$$CM_H = \frac{800(V)}{t_r(\mu s)} \qquad CM_L = -\frac{800(V)}{t_f(\mu s)}$$

Note: CM_L (CM_H) is the maximum rate of fall (rise) of the common mode voltage that can be sustained with the output voltage in the low (high) state.

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