Data sheet acquired from Cypress Semiconductor Corporation.
Data sheet modified to remove devices not offered.

TEXAS INSTRUMENTS

CY74FCT163543

SCCS063A - June 1997 - Revised April 2000

16-Bit Latched Transceiver

Features

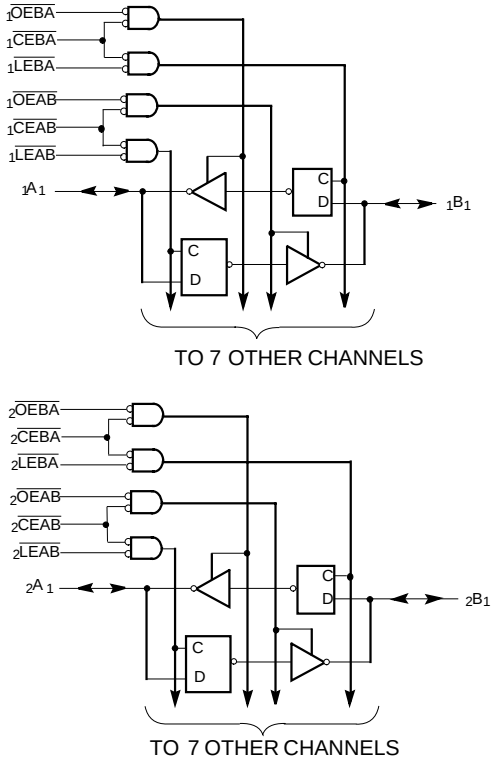
- **Low power, pin-compatible replacement for LCX and LPT families**
- **5V tolerant inputs and outputs**
- **24 mA balanced drive outputs**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for reduced noise**
- **FCT-C speed at 5.1 ns**
- **Latch-up performance exceeds JEDEC standard no. 17**
- **ESD > 2000V per MIL-STD-883D, Method 3015**
- **Typical output skew < 250 ps**
- **Industrial temperature range of –40˚C to +85˚C**
- **TSSOP (19.6-mil pitch) or SSOP (25-mil pitch)**
- **Typical V_{olp} (ground bounce) performance exceeds Mil Std 883D**
- **V_{CC} = 2.7V to 3.6V**

Functional Description

The CY74FCT163543 is a 16-bit, high-speed, low power latched transceiver that is organized as two independent 8-bit D-type latched transceivers, containing two sets of eight D-type latches with separate Latch Enable ($\overline{LEAB}$, $\overline{LEAB}$) and Output Enable ($\overline{OEAB}$, $\overline{OEAB}$) controls for each set to permit independent control of inputting and outputting in either direction of data flow. For data flow from A to B, for example, the A-to-B input Enable ($\overline{CEAB}$) must be LOW in order to enter data from A or to take data from B, as indicated in the truth table. With $\overline{CAEB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer follow the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the three-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses $\overline{CEAB}$, $\overline{LEAB}$, and $\overline{OEAB}$ inputs.

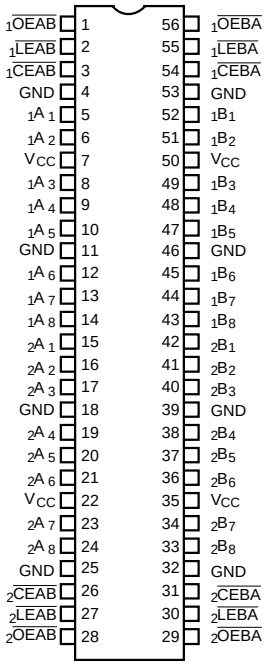
The CY74FCT163543 has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The inputs and outputs are capable of being driven by 5.0V buses, allowing them to be used in mixed voltage systems as translators. The outputs are also designed with a power off disable feature enabling them to be used in applications requiring live insertion. Flow-through pinout and small shrink packaging simplify board design.

Logic Block Diagrams



Pin Configuration

Top View
SSOP/TSSOP



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Pin Description

Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A	A-to-B Data Inputs or B-to-A Three-State Outputs
B	B-to-A Data Inputs or A-to-B Three-State Outputs

Function Table[1]

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A to B	B
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs[2]

Maximum Ratings[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –55°C to +125°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage Range ..... 0.5V to +4.6V

DC Input Voltage .....–0.5V to +7.0V

DC Output Voltage .....–0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .....–60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	2.7V to 3.6V

Electrical Characteristics Over the Operating Range V_{CC}=2.7V to 3.6V

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{IH}	Input HIGH Voltage			2.0		5.5	V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Input Hysteresis[6]				100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min.,	I_{IN}=–18 mA		–0.7	–1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max.,	V_{CC}=5.5V			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max.,	V_{CC}=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State pins)	V_{CC}=Max.,	V_{OUT}=5.5V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State pins)	V_{CC}=Max.,	V_{OUT}=GND			±1	µA
I_{ODL}	Output LOW Current[7]	V_{CC}=3.3V, V_{OUT}=1.5V	V_{IN}=V_{IH} or V_{IL},	50	90	200	mA
I_{ODH}	Output HIGH Current[7]	V_{CC}=3.3V, V_{OUT}=1.5V	V_{IN}=V_{IH} or V_{IL},	–36	–60	–110	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min.,	I_{OH}=–0.1 mA	V_{CC}–0.2			V
		V_{CC}=3.0V,	I_{OH}=–8 mA	2.4	3.0		
		V_{CC}=3.0V,	I_{OH}=–24 mA	2.0	3.0		
V_{OL}	Output LOW Voltage	V_{CC}=Min.,	I_{OL}=0.1mA			0.2	V
		V_{CC}=Min.,	I_{OL}=24mA		3.0	0.5	
I_{OS}	Short Circuit Current[7]	V_{CC}=Max.,	V_{OUT}=GND	–60	–135	–240	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V,	V_{OUT}≤4.5V			±100	µA

Notes:

1. A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, LEBA, and $\overline{OEBA}$.
2. Data prior to $\overline{LEAB}$ LOW-to-HIGH Transition H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = High Impedance.
3. Operation beyond the limits set forth may impair the useful life of the device. Unless noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
5. Typical values are at V_{CC}= 3.3V, T_A= +25˚C ambient.
6. This parameter is specified but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[6] (T_A = +25˚C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN}\leq$0.2V, $V_{IN}\geq V_{CC}$–0.2V	0.1	10	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	$V_{IN}=V_{CC}$-0.6V[8]	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	50	75	µA/MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	0.5	0.8	mA
			$V_{IN}=V_{CC}$-0.6V or V_{IN}=GND	0.5	0.8	mA
		V_{CC}=Max., f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE}$=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	2.0	3.0[11]	mA
			$V_{IN}=V_{CC}$-0.6V or V_{IN}=GND	2.0	3.3[11]	mA

Switching Characteristics Over the Operating Range V_{CC} = 3.0V to 3.6V[12,15]

Parameter	Description	CY74FCT163543A		CY74FCT163543C		Unit	Fig. No.[13]
		Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, Transparent Mode A to B or B to A	1.5	6.5	1.5	5.1	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A, $\overline{LEAB}$ to B	1.5	8.0	1.5	5.6	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B	1.5	9.0	1.5	7.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B	1.5	7.5	1.5	6.5	ns	1, 7, 8
t_{SU}	Set-up Time HIGH or LOW A or B to $\overline{LEAB}$ or $\overline{LEBA}$	2.0	—	2.0	—	ns	4
t_H	Hold Time HIGH or LOW A or B to $\overline{LEAB}$ or $\overline{LEBA}$	2.0	—	2.0	—	ns	4
t_W	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW	4.0	—	4.0	—	ns	5
$t_{SK(O)}$	Output Skew[14]	—	0.5	—	0.5	ns	—

Notes:

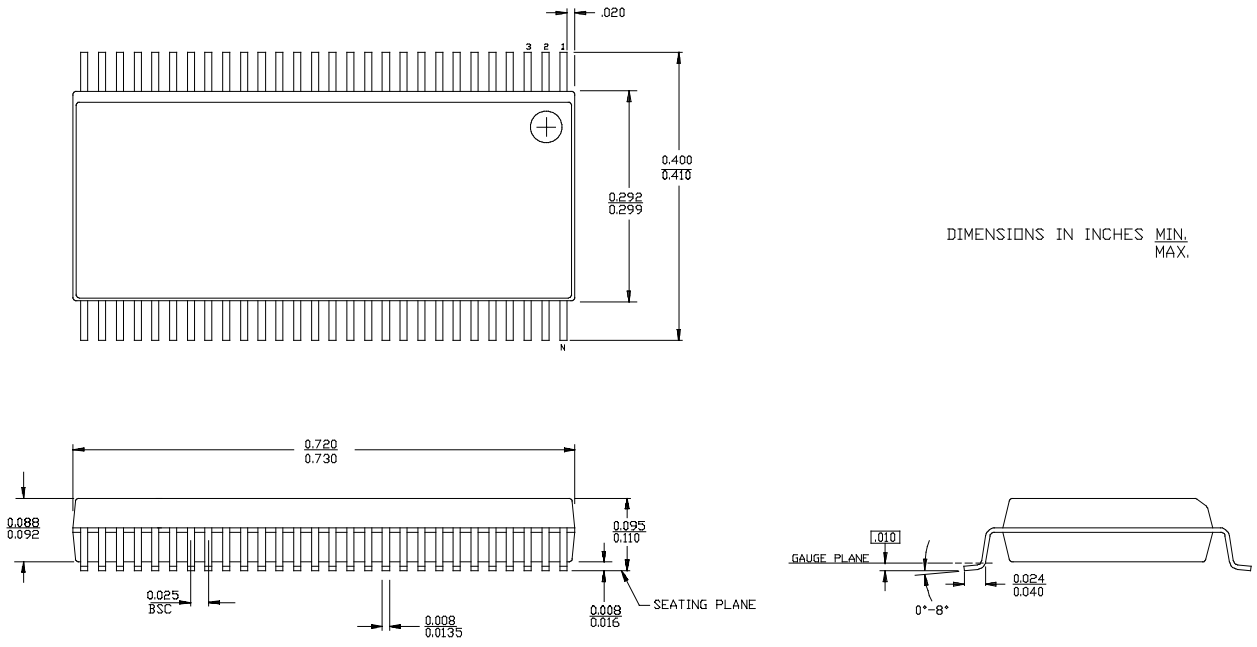
8. Per TTL driven input; all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0N_C/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    N_C = Number of clock inputs changing at f_1
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.
12. Minimum limits are specified but not tested on Propagation Delays.
13. See “Parameter Measurement Information” in the General Information section.
14. Skew between any two outputs of the same package switching in the same directional. This parameter is ensured by design.
15. For V_{CC} =2.7, propagation delay, output enable and output disable times should be degraded by 20%.

Ordering Information CY74FCT163543

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.1	CY74FCT163543CPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163543CPVC/PVCT	O56	56-Lead (300-Mil) SSOP	
6.5	CY74FCT163543APVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial

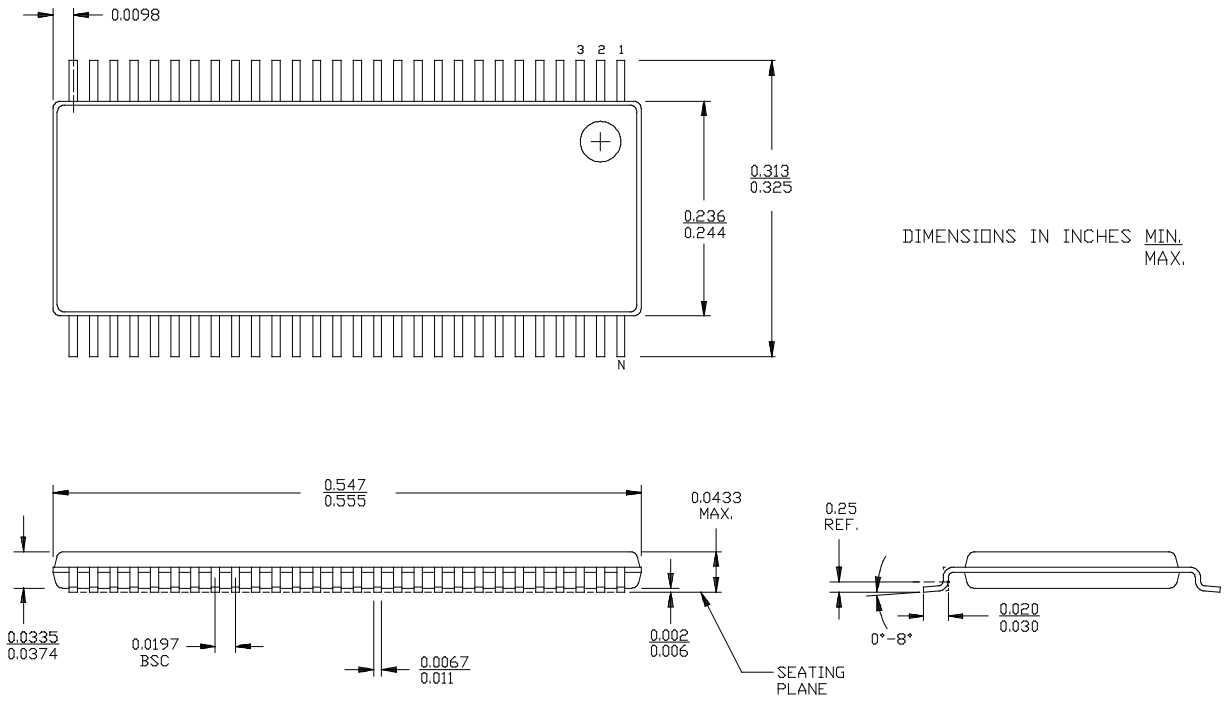
Package Diagrams

56-Lead Shrunk Small Outline Package O56



Package Diagrams (continued)

56-Lead Thin Shrunk Small Outline Package Z56



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CY74FCT163543APVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
CY74FCT163543APVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
CY74FCT163543CPAC	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
CY74FCT163543CPACT	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
CY74FCT163543CPVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
CY74FCT163543CPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

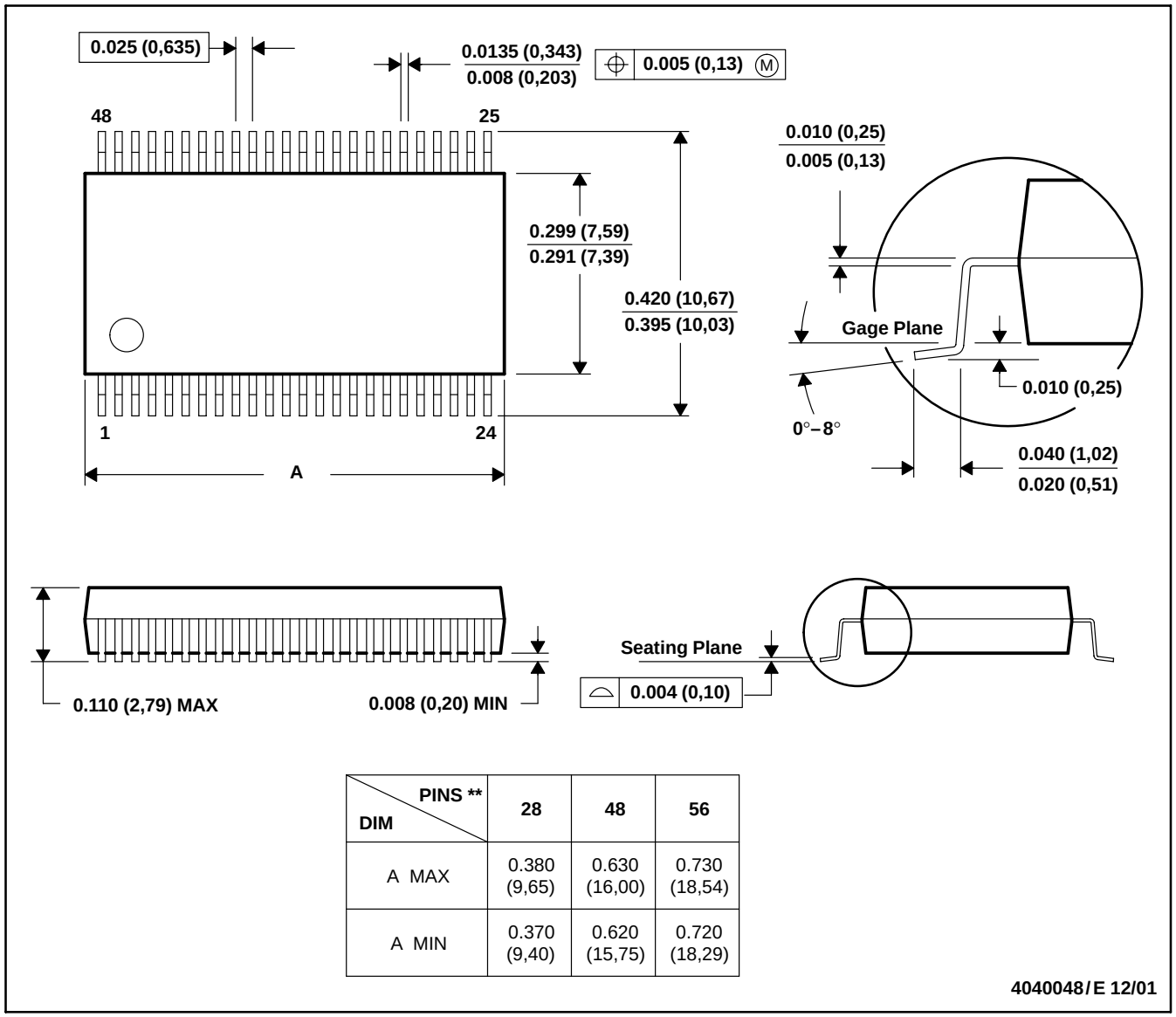
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



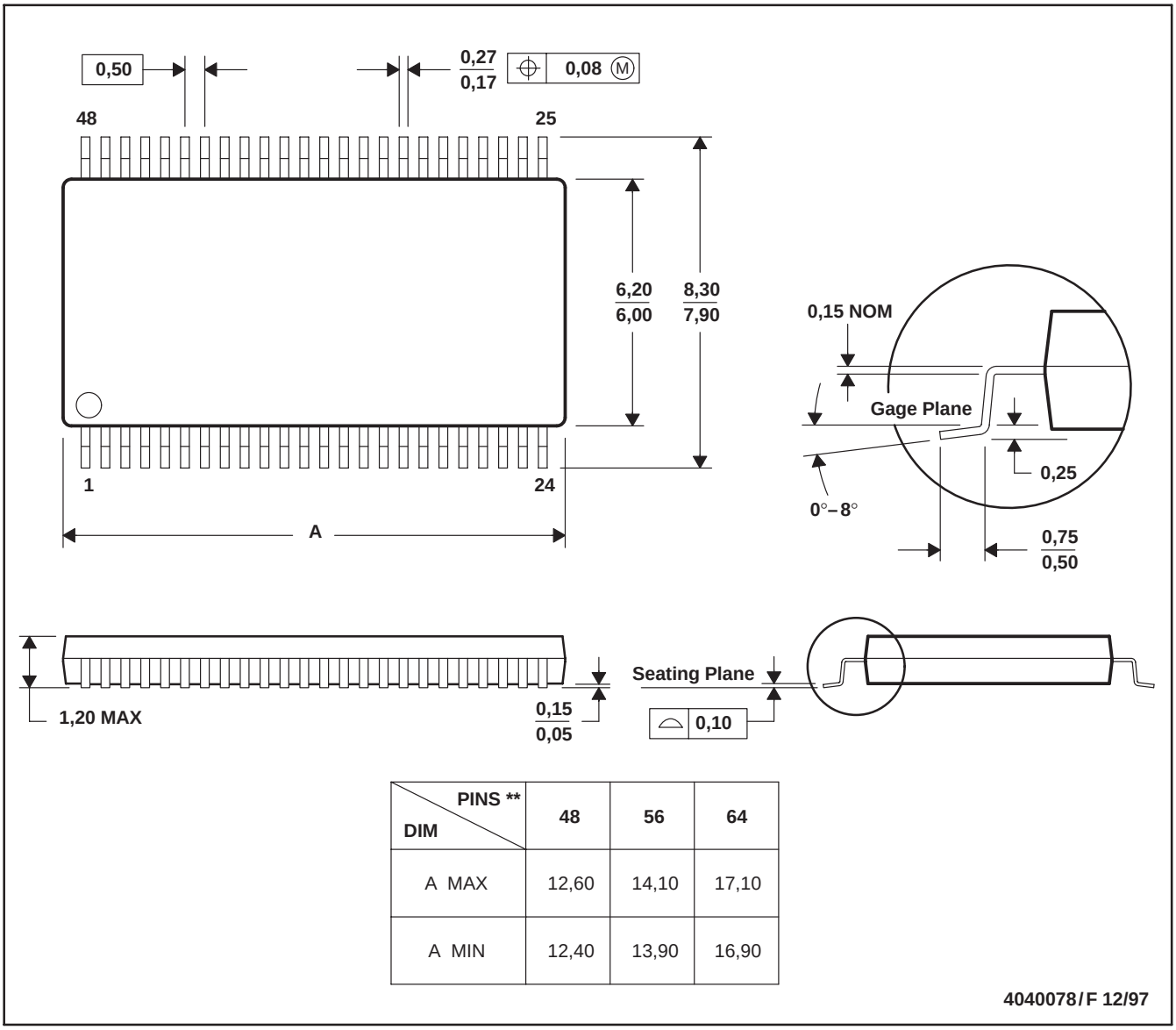
DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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SN74LVCZ240APW TPS71710DCKR OPA643P TPS51125ARGER TPS92200D2DDCR ISO124U/1K
MSP430F2112TRHBT MSP430F5131IDA MSP430G2332IN20 TLC085CDR TLV990-28PFB
TPA6203A1DRBR BQ24314DSGR DS90C383MTDX/NOPB MSP430F2001TRSAT MSP430F47127IPZ
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