3P3T Antenna Cross Switch with MIPI 2.1

Features

- Broadband frequency range: 0.1 to 5.0 GHz
- Low insertion loss: 0.83dB typical @ 3.80 GHz
- High $P_{0.1}$ dB of 39 dBm
- High isolation: 40 dB typical @ 3.80 GHz
- MIPI RFFE V2.1 interface
- Single VIO supply
- No DC blocking capacitors if no DC applied on RF lines
- Small WBQFN 2.0mm x 2.0mm x 0.55 mm -16L package

Applications

- Antenna routing switch for cellular devices
- Cellular Modems , Tablets and USB Devices
- GSM/CDMA/WCDMA/LTE and NR including n41, n77, n78, n79 bands

General Description

The AW12033TQNR is a three-pole, three-throw(3P3T) CMOS SOI switch with low insertion loss, high Isolation and high power handling capability. It is suitable for multi-mode LTE and 5G NR triple antenna applications.

The AW12033TQNR is perfectly compatible with MIPI RFFE V2.1 control interface operating in 1.65 to 1.95V voltage range. It is provided in a compact 2.0mm x 2.0mm x 0.55mm size, 16-pin WBQFN package.

Typical Application Circuit

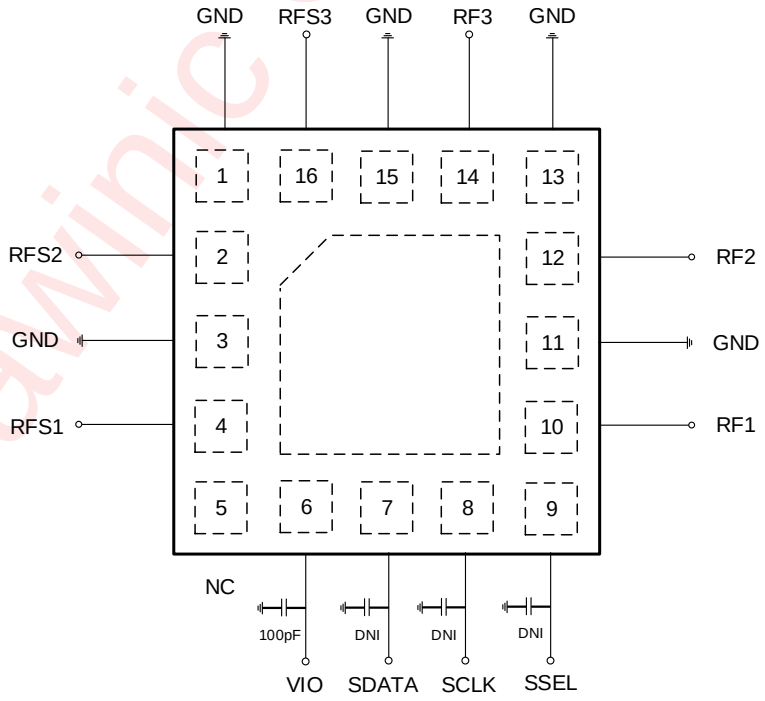


Figure 1 Typical Application Circuit of AW12033TQNR

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Pin Configuration And Top Mark

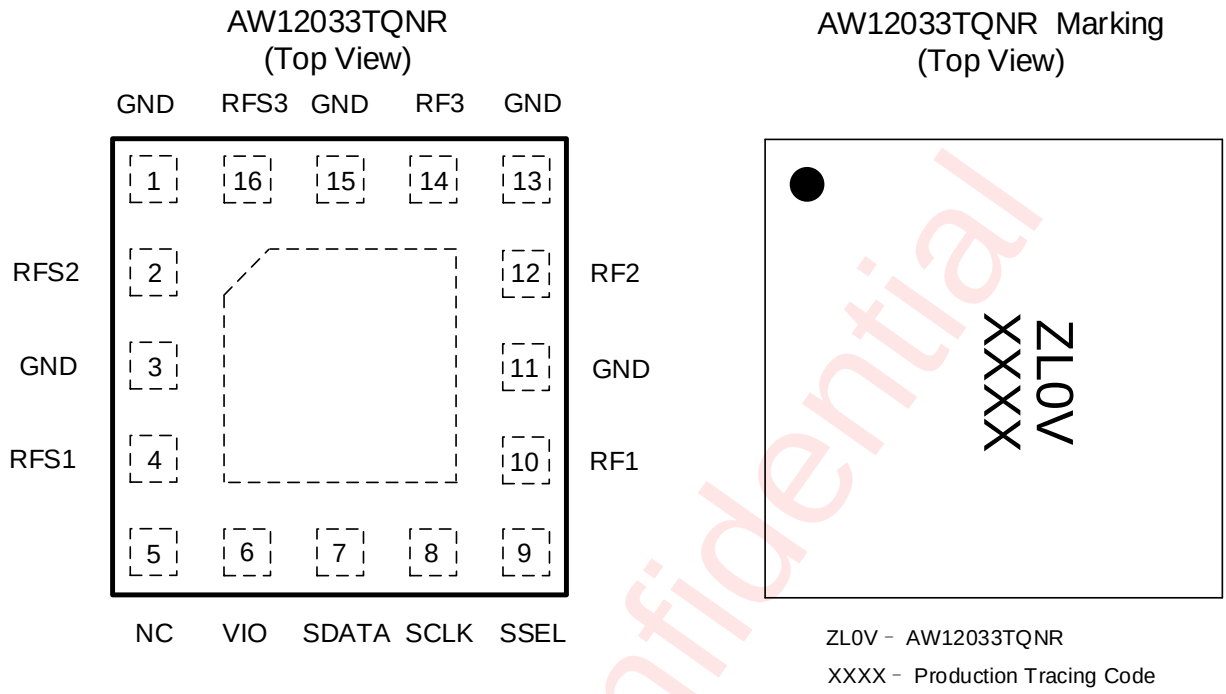


Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	GND	Ground
2	RFS2	RFS port2 - with internal shunt switch to GND
3	GND	Ground
4	RFS1	RFS port1 - with internal shunt switch to GND
5	NC	Not Connected
6	VIO	MIPI RFFE power supply
7	SDATA	MIPI RFFE data
8	SCLK	MIPI RFFE clock
9	SSEL	MIPI USID select port
10	RF1	RF port1
11	GND	Ground
12	RF2	RF port2
13	GND	Ground
14	RF3	RF port3
15	GND	Ground
16	RFS3	RFS port3 - with internal shunt switch to GND

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Functional Block Diagram

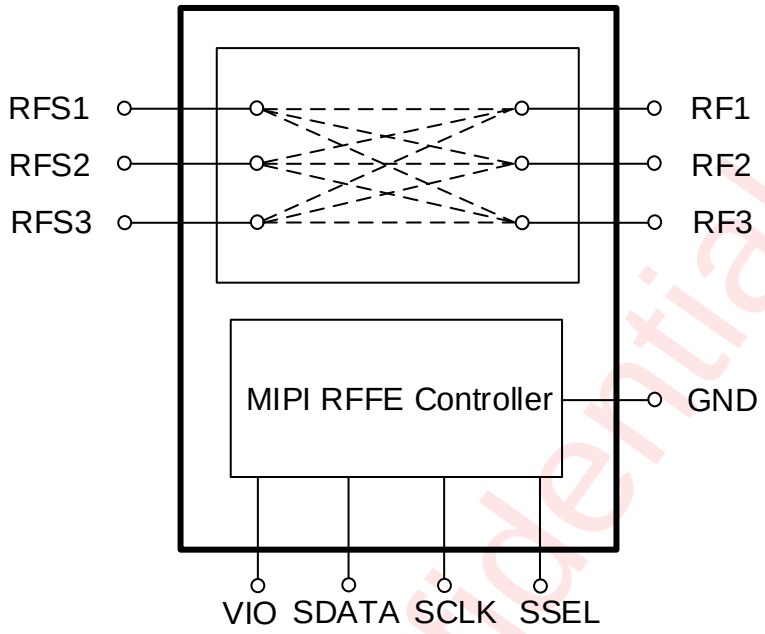


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW12033TQNR	-40°C～85°C	WBQFN 2.0mm x 2.0mm x 0.55 mm -16L	ZL0V	MSL1	ROHS+HF	4500 units/ Tape and Reel

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Absolute Maximum Ratings(NOTE1)

PARAMETERS	RANGE
Supply Voltage VIO for MIPI	-0.3V to 2.5V
Interface Control Voltage Range SDATA, SCLK	-0.3V to 2.5V
RF input power	40 dBm
Operating Free-air Temperature Range	-40°C to 85°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD	
HBM(Human Body Model)(NOTE 2)	±1000V
CDM (Charged Device Model) (NOTE 3)	±500V

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-002-2018.

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Electrical Characteristics

VIO=1.8V, PIN=0dBm, VSWR=1:1,Temp=+25°C. (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC Specifications						
V_{IO}	Supply voltage for MIPI		1.65	1.8	1.95	V
I_{IO}	V_{IO} Supply Current	Active Mode		60	120	μA
		Low Power Mode		2	15	μA
V_{CTL_H}	SDATA,SCLK Control Voltage High	Must not exceed V_{IO} voltage	0.8*V_{IO}	V_{IO}	1.95	V
V_{CTL_L}	SDATA,SCLK Control Voltage Low	Must not exceed V_{IO} voltage	0	0	0.2*V_{IO}	V
T_{SW}	Time to switch between RF states	50% last SCLK falling edge to 90% RF signal		2	3	μs
Tpup	Time from Power Up plus Switch command	50% last SCLK falling edge to 90% RF signal		10	20	μs
RF Specifications						
IL	Insertion Loss (RFS1/2/3 to RF1/2/3)	617-960MHz		0.45	0.65	dB
		1425-2200MHz		0.59	0.80	dB
		2300-2690MHz		0.70	0.90	dB
		3300-3800MHz		0.83	1.20	dB
		3800-5000MHz		1.0	1.50	dB
RL	Return Loss(RFS1/2/3 to RF1/2/3)	617-960MHz	18	23		dB
		1425-2200MHz	13	19		dB
		2300-2690MHz	12	18		dB
		3300-3800MHz	10	13		dB
		3800-5000MHz	8	12		dB
ISO	Isolaiton(RFS1/2/3 to RF1/2/3)	617-960MHz	32	50		dB
		1425-2200MHz	26	44		dB
		2300-2690MHz	25	42		dB
		3300-3800MHz	22	40		dB
		3800-5000MHz	20	37		dB
H2	Second Harmonics	Freq=900MHz, P_{IN}=+35dBm,CW		-60	-45	dBm
H3	Third Harmonics	Freq=900MHz, P_{IN}=+35dBm,CW		-55	-45	dBm
H2	Second Harmonics	Freq=1900MHz, P_{IN}=+33dBm,CW		-58	-45	dBm

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PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
H3	Third Harmonics	Freq=1900MHz, P_{IN}=+33dBm,CW		-60	-45	dBm
$P_{0.1dB}$	0.1dB Compression Point	All RFS/RF Ports		39.0		dBm

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Power ON and OFF Sequence

1. Once V_{IO} is powered down to 0 V, wait at least 10 μs to reapply power to V_{IO}.

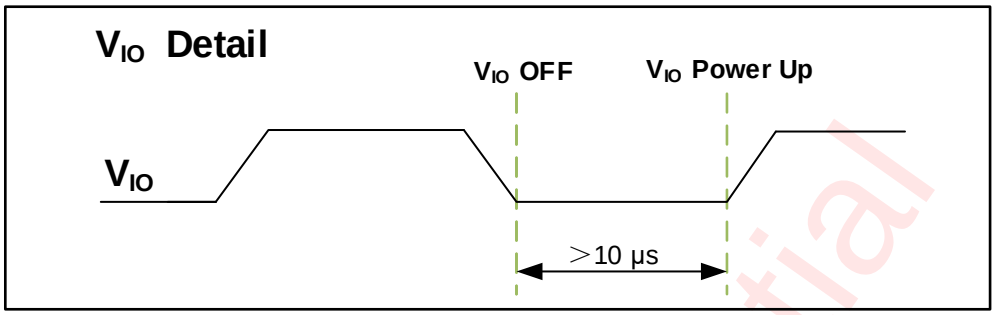


Figure 4 Digital Supply Detail

2. Before applying RF power , V_{IO} must be turned on for at least 10 μs.

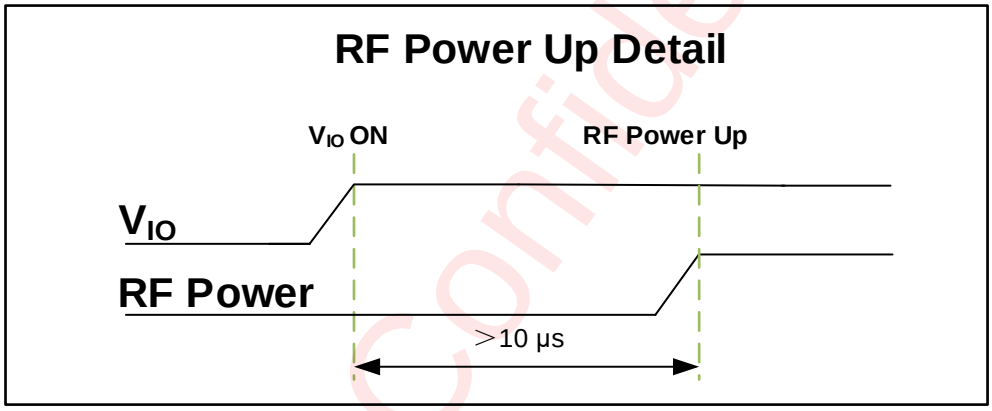


Figure 5 RF Power-Up Detail

3. Before sending SDATA/SCLK , V_{IO} must be applied for at least 800 ns to ensure correct data transmission. And after the RFFE bus is idle, wait at least 3 μs to apply the RF signal.

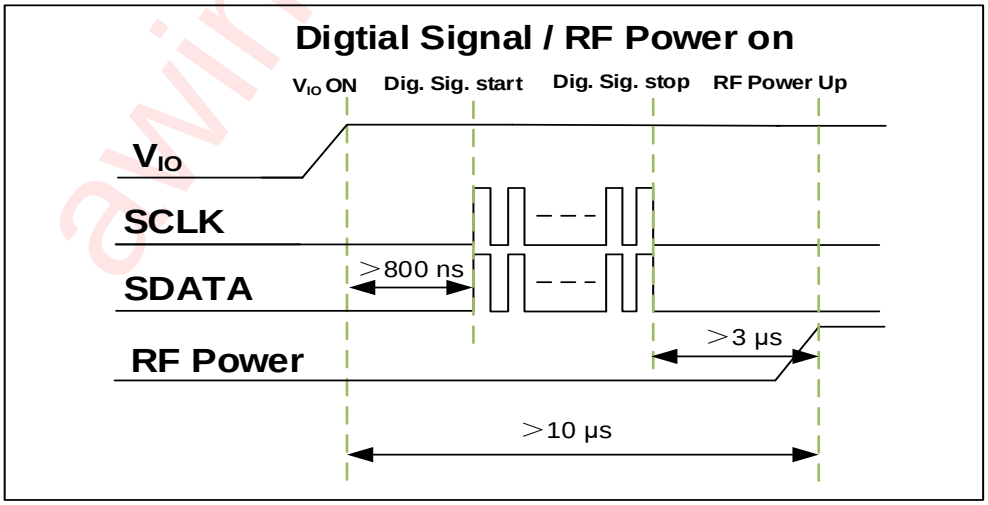


Figure 6 Digital Signal / RF Power-On Detail

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4. There shall be no RFFE bus operations during RF Signal active to protect the device. So RF input signal shall be applied after RFFE bus operations being finished and be removed before RFFE bus operations being started.

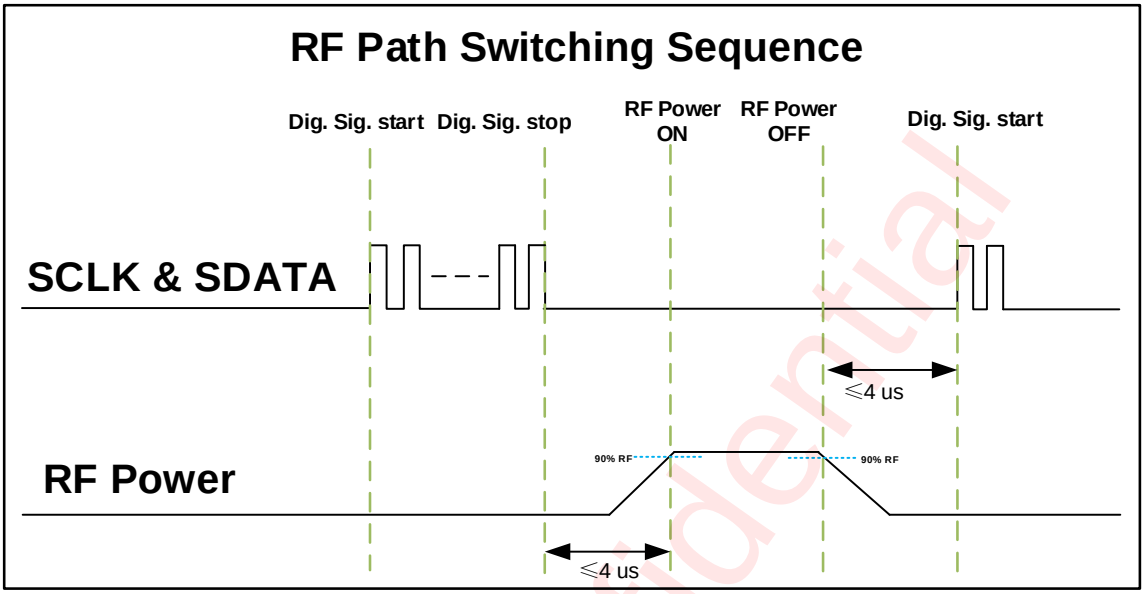


Figure 7 RF Path Switching Sequence

5. If “Lower Power Mode” is used, there must be a 10 μs delay before exiting “Lower Power Mode”.

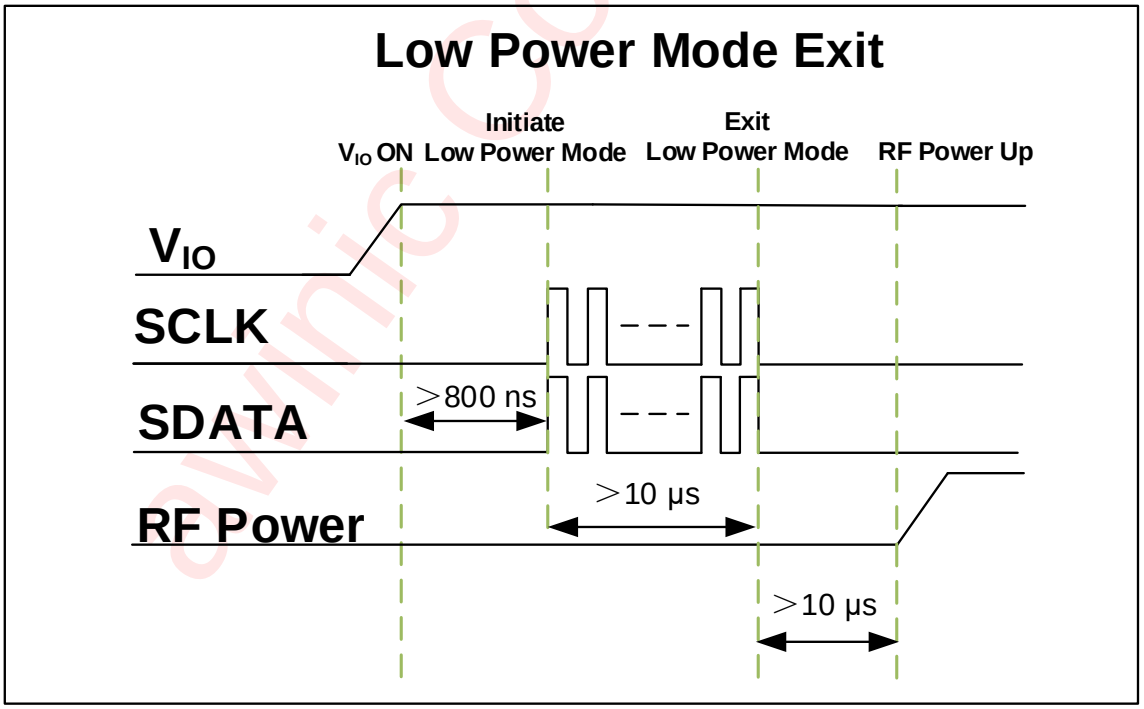


Figure 8 Lower Power Mode Exit Timing

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MIPI RFFE Specification

The MIPI RFFE interface is working in systems following the MIPI Alliance Specification for RF Front-End Control Interface version 2.1.

TABLE1: MIPI FEATURES

Feature	Supported	Comment
MIPI RFFE 2.1 standard	Yes	
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Masked write command sequence	Yes	Indicated as MW in below register mapping tables
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz for read and write
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz for write
Half speed read	Yes	
Full speed read Full speed write	Yes	
Longer Reach RFFE Bus Length Feature	Yes	
Programmable driver strength	Yes	
Programmable Group SID	Yes	
Programmable USID	Yes	Support for three registers write and extended write sequences
Trigger functionality	Yes	
Extended Triggers and Trigger Masks	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID select pin	Yes	External pin for changing USID: USID select pin = 0→0x0B USID select pin = 1→0x0A

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TABLE2: Start-up Behavior

Feature	State	Comment
Power status	Low power mode	Low power mode after start-up
Trigger function	Enable	Enable after start-up. Programmable via register

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MIPI Read and Write Timing

Register 0 write:

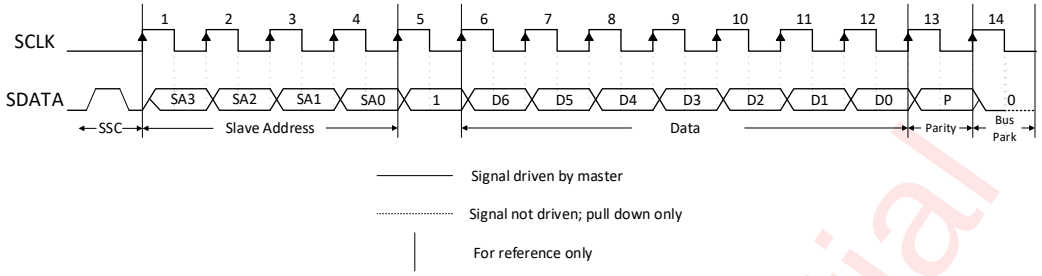


Figure 9 Register 0 write command sequence

Register write:

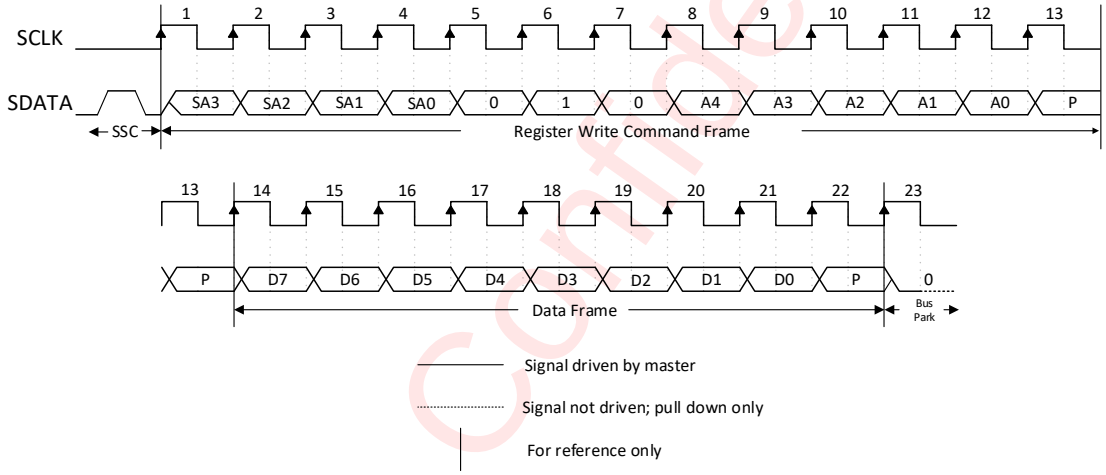


Figure 10 Register write command sequence

Register read:

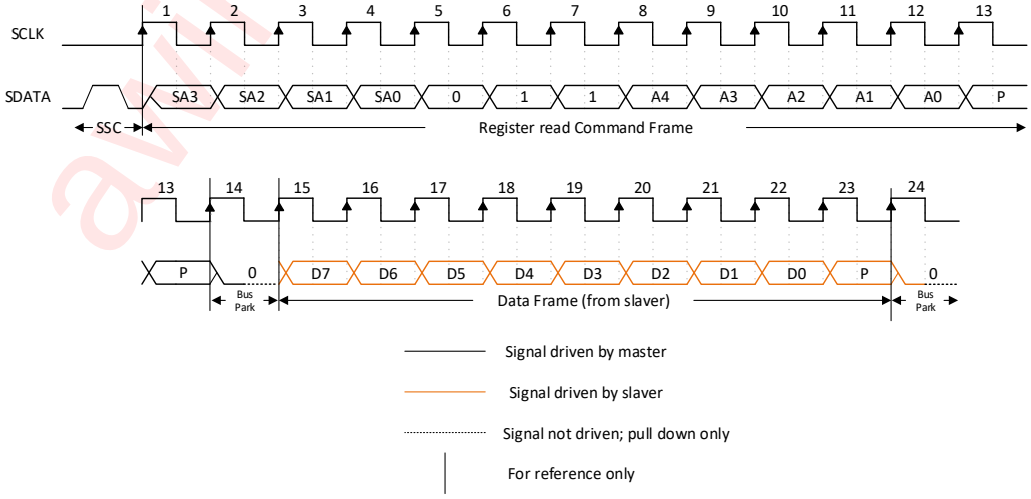


Figure 11 Register read command sequence

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Extended Register write:

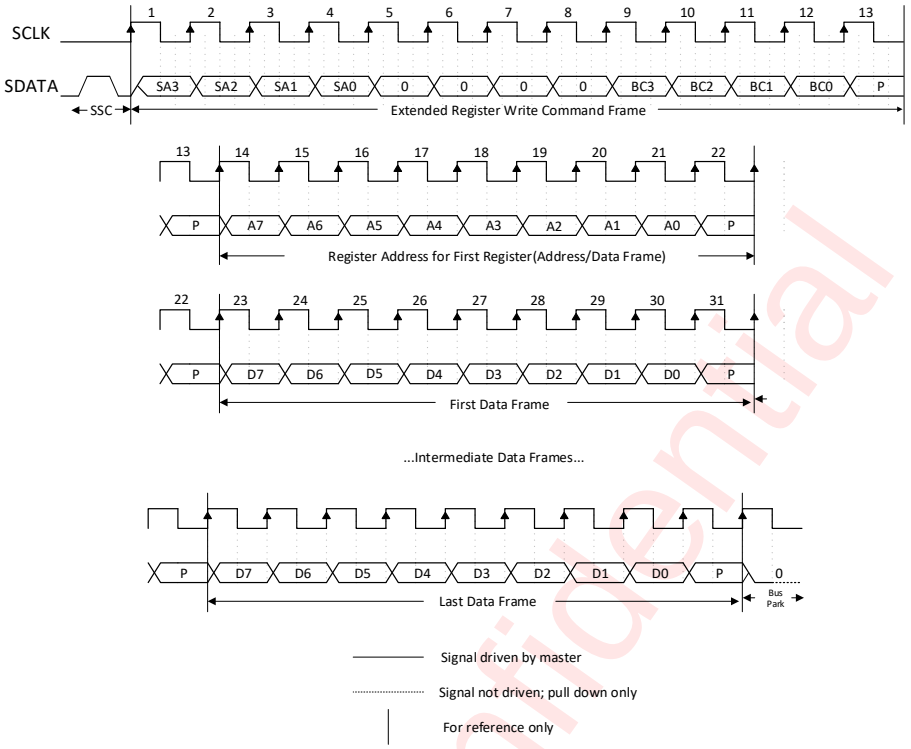


Figure 12 Extended Register write command sequence

Extended Register read:

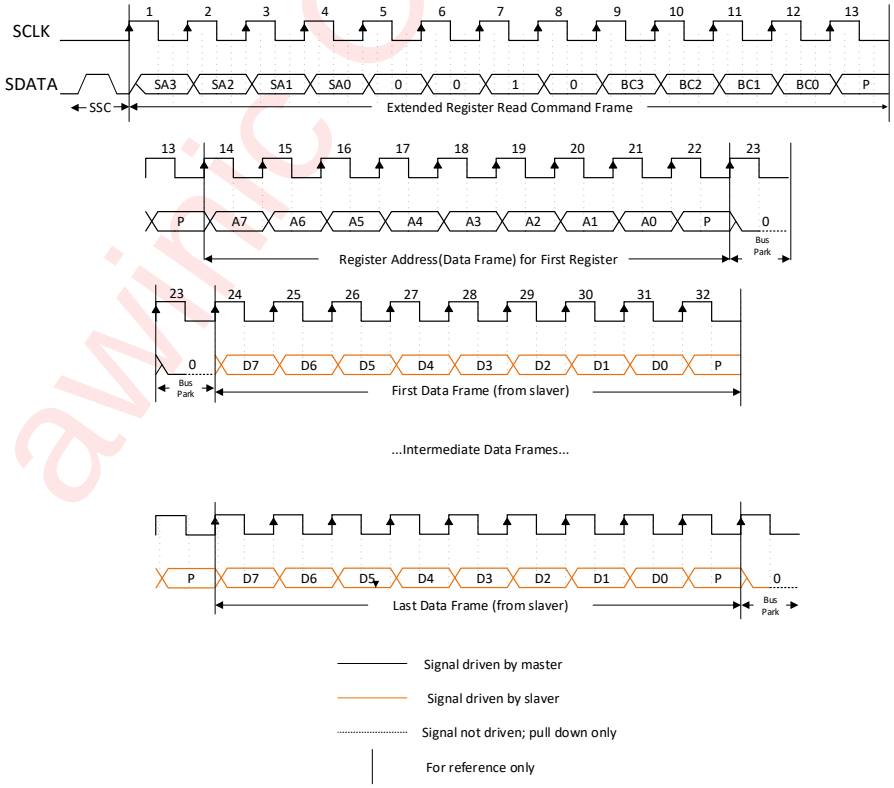


Figure 13 Extended Register read command sequence

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Masked write:

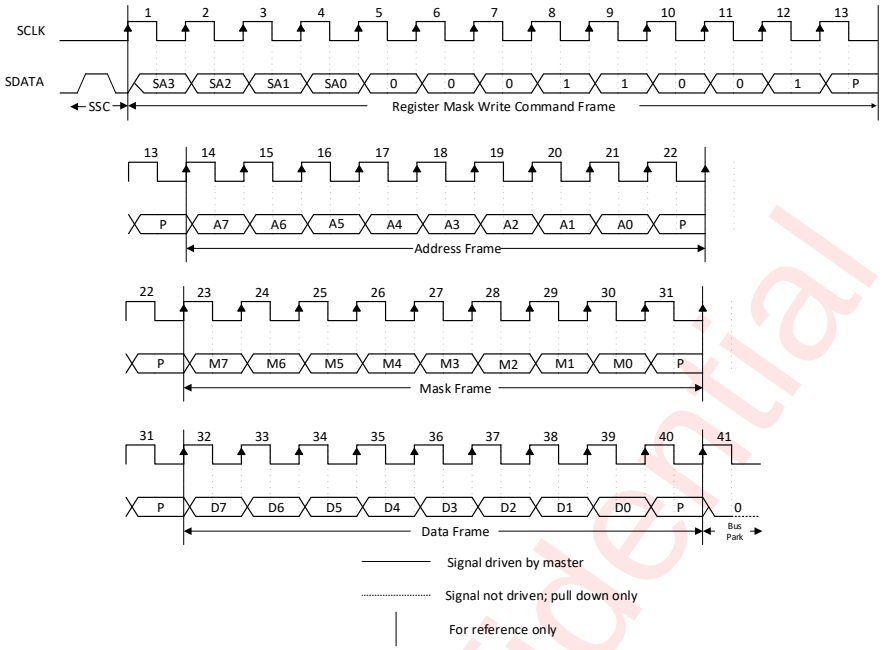


Figure 14 Masked Write Command Sequence

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Register Configuration

Register Detailed Description

REGISTER 0x00：REGISTER_0

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	RF Control 0	Register_0 Truth Table	0x00	No	Trig 0-10	RW MW

REGISTER 0x01：REGISTER_1

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	RF Control 1	Register_1 Truth Table	0x00	No	Trig 0-10	RW MW

REGISTER 0x1A：RFFE_STATUS

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Reset all configurable non-RFFE reserved register to default values 0: normal operation 1: software reset	0x0	No	No	W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0x0	No	No	RW
5	CMD_LEN ERR	Command Sequence received with an incorrect length	0x0	No	No	RW
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0x0	No	No	RW
3	DATA_FR_P_ERR	Data Frame received with a parity error	0x0	No	No	RW
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0x0	No	No	RW
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0x0	No	No	RW
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0x0	No	No	RW

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REGISTER 0x1B：GSID0-1

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

REGISTER 0x1C：PM_TRIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	PWR_MODE[1]	0: Normal Operation 1: Low Power - Antenna in isolation	1	B/G	No	R/W
6	PWR_MODE[0]	0: ACTIVE 1: STARTUP - Reset all registers to default settings *Note: Setting PWR_MODE to STARTUP is identical to a hardware reset initiated by the VIO signal.*	0	B/G	No	R/W
5:3	TriggerMask[2:0]	Setting bit TriggerMask[N] disables Trigger[N] TriggerMask[N] updates before Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register. If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.*	000	No	No	R/W
2:0	Trigger[2:0]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[0], [1], and [2] will always read as 0.*	000	B/G	No	W

REGISTER 0x1D：PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[7:0]	Lower eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x0C	No	No	R

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REGISTER 0x1E：MANUFACTURER_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	MFG_ID[7:0]	Lower eight bits of MIPI Manufacturer ID *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x49	No	No	R

REGISTER 0x1F：MAN_USID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	MFG_ID[11:8]	Upper four bits of MIPI Manufacturer ID *Note: This is a read-only register. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this register, but does not update it. See MIPI 6.6.2 for details.*	0x00	No	No	R
3:0	USID[3:0]	Programmable Unique Slave ID The default value at reset is selected via pin SSEL		No	No	R/W
		USID pin connected to GND	0x0B			
		USID pin connected to VIO	0x0A			

REGISTER 0x20：EXT_PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	EXT_PROD_ID[7:0]	Upper eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x00	No	No	R

REGISTER 0x21：REVISION_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	REVISION_ID[7:0]	This is a read-only register.	0x04	No	No	R

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REGISTER 0x22：GSID2-3

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID2[3:0]	Group Slave ID2	0x0	No	No	R/W
3:0	GSID3[3:0]	Group Slave ID3	0x0	No	No	R/W

REGISTER 0x23：UDR_RST

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.*	0	B/G	No	W
6:0	RESERVED		0x00	No	No	R

REGISTER 0x24：ERR_SUM

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	SPARE	Reserved for future use	0	No	No	R/W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W

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REGISTER 0x2D：EXT_TRIG_MASK

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	TriggerMask[10:3]	Setting bit TriggerMask[N] disables Trigger[N] If using an Extended Write to update both TriggerMask and Trigger, than TriggerMask[N] updates before Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register. If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.*	0xFF	No	No	R/W

REGISTER 0x2E：EXT_TRIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	Trigger[10:3]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[10 - 3] will always read as 0.*	0x00	B/G	No	W

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Truth Table

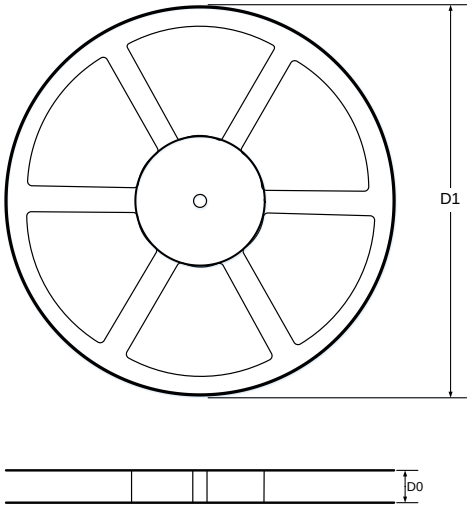
REGISTER_0									
state	Mode	D7	D6	D5	D4	D3	D2	D1	D0
1	RFS1-OPEN	×	×	×	×	×	0	0	0
2	RFS1-RF1	×	×	×	×	×	0	0	1
3	RFS1-RF2	×	×	×	×	×	0	1	0
4	RFS1-RF3	×	×	×	×	×	0	1	1
5	RFS2-OPEN	×	×	0	0	0	×	×	×
6	RFS2-RF1	×	×	0	0	1	×	×	×
7	RFS2-RF2	×	×	0	1	0	×	×	×
8	RFS2-RF3	×	×	0	1	1	×	×	×
REGISTER_1									
9	RFS3-OPEN	×	×	×	×	×	0	0	0
10	RFS3-RF1	×	×	×	×	×	0	0	1
11	RFS3-RF2	×	×	×	×	×	0	1	0
12	RFS3-RF3	×	×	×	×	×	0	1	1

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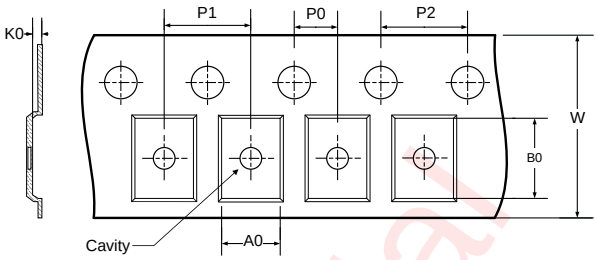
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Tape And Reel Information

REEL DIMENSIONS

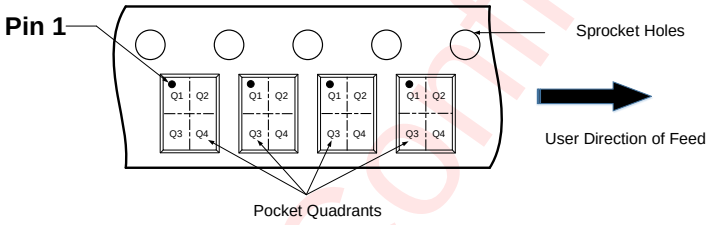


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2.25	2.25	0.75	2	4	4	8	Q1

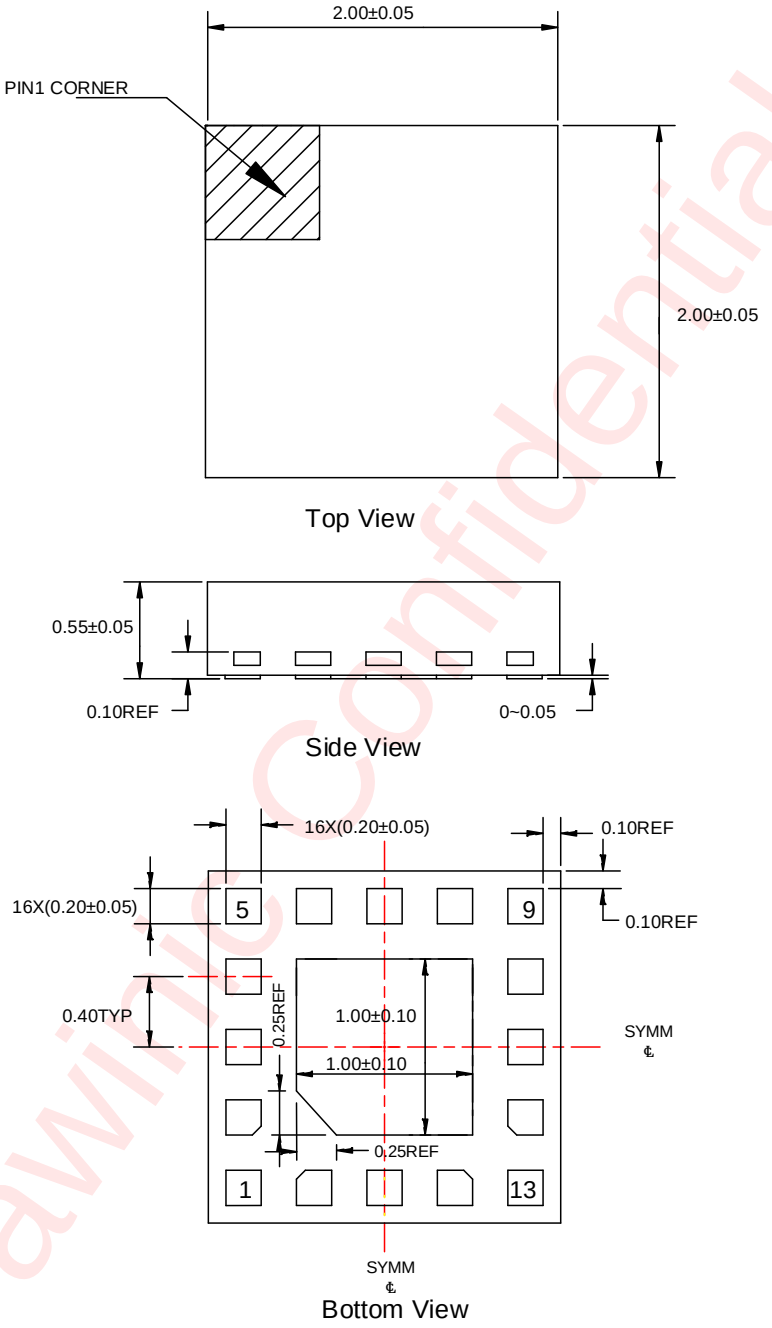
All dimensions are nominal

Figure 15 Tape and Reel

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Package Outline Dimensions



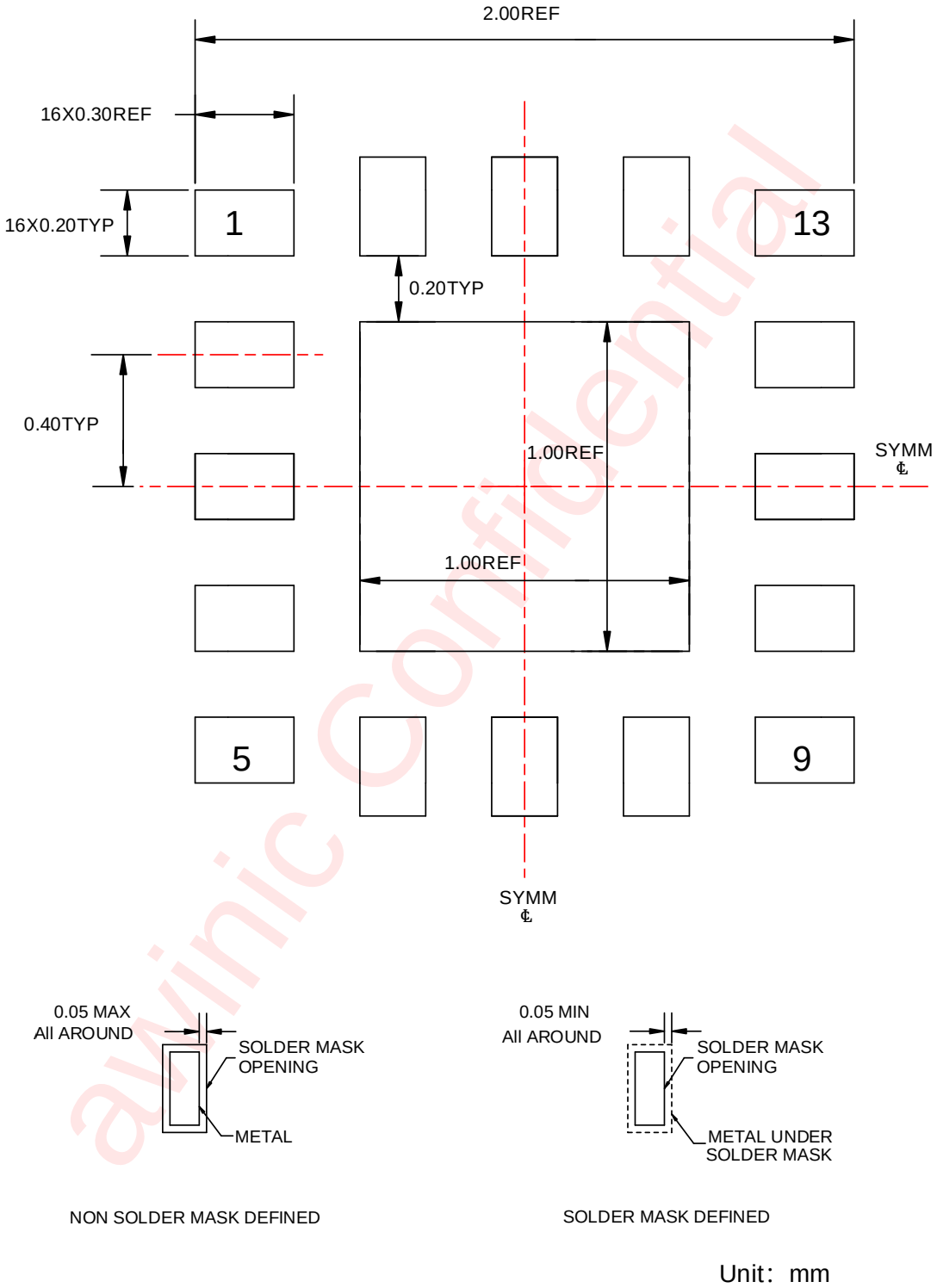
Unit: mm

Figure 16 Package Outline

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Land Pattern Data



Unit: mm

Figure 17 Land Pattern

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Revision History

Vision	Date	Change Record
V1.0	Dec. 2021	Officially Released
V1.1	May. 2022	Update the upper four bits of MIPI Manufacturer ID; Update the reset nubmer of 2D register Update the truth table
V1.2	Aug. 2022	Update Supply Voltage VIO for MIPI
V1.3	Dec. 2022	Update IL and RL
V1.4	Apr. 2023	Update Electrical Characteristics
V1.5	Dec. 2023	Update REGISTER 0x1A

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