# DMN4010LFG-7-VB Datasheet

## N-Channel 40V (D-S) MOSFET

| PRODUCT SUMMARY | | | |
|---|---|---|---|
| $V_{DS}$ (V) | $R_{DS(on)}$ (Ω) | $I_D$ (A) [f] | $Q_g$ (TYP.) |
| 40 | 0.013 at $V_{GS}$ = 10 V | 28 | 6.8 nC |
| | 0.015 at $V_{GS}$ = 4.5 V | 25 | |

### FEATURES

- Trench Gen IV power MOSFET
- Tuned for the lowest $R_{DS}$ - $Q_{oss}$ FOM
- 100 % $R_g$ and UIS tested
- $Q_{gd}$ / $Q_{gs}$ ratio < 1 optimizes switching characteristics

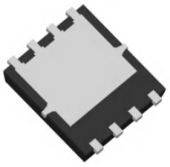
RoHS COMPLIANT
HALOGEN FREE

DFN 3x3

Top View

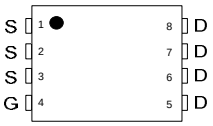


Bottom View



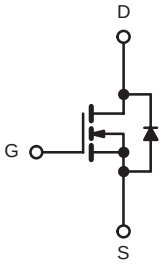
Pin 1

Top View




### APPLICATIONS

- Synchronous rectification
- DC/DC converters
- Motor drive switch
- Battery and load switch




N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C, unless otherwise noted) | | | | |
|---|---|---|---|---|
| PARAMETER | | SYMBOL | LIMIT | UNIT |
| Drain-Source Voltage | | $V_{DS}$ | 40 | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 20 | |
| Continuous Drain Current ($T_J$ = 150 °C) | $T_C$ = 25 °C | $I_D$ | 30 | A |
| | $T_C$ = 70 °C | | 25.3 | |
| | $T_A$ = 25 °C | | 11.4 [a, b] | |
| | $T_A$ = 70 °C | | 9.2 [a, b] | |
| Pulsed Drain Current (t = 100 µs) | | $I_{DM}$ | 70 | |
| Continuous Source-Drain Diode Current | $T_C$ = 25 °C | $I_S$ | 19 | |
| | $T_A$ = 25 °C | | 2.2 [a, b] | |
| Single Pulse Avalanche Current | L = 0.1 mH | $I_{AS}$ | 11 | |
| Single Pulse Avalanche Energy | | $E_{AS}$ | 6 | mJ |
| Maximum Power Dissipation | $T_C$ = 25 °C | $P_D$ | 23 | W |
| | $T_C$ = 70 °C | | 14.8 | |
| | $T_A$ = 25 °C | | 2.6 [a, b] | |
| | $T_A$ = 70 °C | | 1.7 [a, b] | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | -55 to +150 | °C |
| Soldering Recommendations (Peak temperature) [c, d] | | | 260 | |

| THERMAL RESISTANCE RATINGS | | | | | |
|---|---|---|---|---|---|
| PARAMETER | | SYMBOL | TYPICAL | MAXIMUM | UNIT |
| Maximum Junction-to-Ambient [a, e] | t ≤ 10 s | $R_{thJA}$ | 38 | 48 | °C/W |
| Maximum Junction-to-Case (Drain) | Steady state | $R_{thJC}$ | 4.3 | 5.4 | |

**Notes**

a. Surface mounted on 1" x 1" FR4 board.
b. t = 10 s.
e. The DFN 3 x 3 EP is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
e. Maximum under steady state conditions is 94 °C/W.
f. Based on $T_C$ = 25 °C.

| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 40 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | $I_D$ = 250 µA | - | 22.1 | - | mV/°C |
| $V_{GS(th)}$ Temperature Coefficient | $\Delta V_{GS(th)}/T_J$ | | - | -5.1 | - | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1.0 | - | 2.5 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = +20 V / -16 V | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 40 V, $V_{GS}$ = 0 V | - | - | 1 | µA |
| | | $V_{DS}$ = 40 V, $V_{GS}$ = 0 V, $T_J$ = 55 °C | - | - | 10 | |
| On-State Drain Current [a] | $I_{D(on)}$ | $V_{DS} \geq$ 5 V, $V_{GS}$ = 10 V | 10 | - | - | A |
| Drain-Source On-State Resistance [a] | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 5 A | - | 0.013 | - | Ω |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 5 A | - | 0.015 | - | |
| Forward Transconductance [a] | $g_{fs}$ | $V_{DS}$ = 10 V, $I_D$ = 5 A | - | 52 | - | S |
| **Dynamic [b]** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V, f = 1 MHz | - | 1800 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 155 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 20 | - | |
| $C_{rss}/C_{iss}$ Ratio | | | - | 0.018 | 0.036 | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 20 V, $V_{GS}$ = 10 V, $I_D$ = 5 A | - | 14.2 | 22 | nC |
| | | $V_{DS}$ = 20 V, $V_{GS}$ = 4.5 V, $I_D$ = 5 A | - | 6.8 | 11 | |
| Gate-Source Charge | $Q_{gs}$ | | - | 3 | - | |
| Gate-Drain Charge | $Q_{gd}$ | | - | 1.5 | - | |
| Output Charge | $Q_{oss}$ | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V | - | 6.5 | - | |
| Gate Resistance | $R_g$ | f = 1 MHz | 0.4 | 2 | 4 | Ω |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 20 V, $R_L$ = 4 Ω<br>$I_D \cong$ 5 A, $V_{GEN}$ = 4.5 V, $R_g$ = 1 Ω | - | 16 | 30 | ns |
| Rise Time | $t_r$ | | - | 56 | 110 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 13 | 25 | |
| Fall Time | $t_f$ | | - | 27 | 55 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 20 V, $R_L$ = 4 Ω<br>$I_D \cong$ 5 A, $V_{GEN}$ = 10 V, $R_g$ = 1 Ω | - | 7 | 15 | |
| Rise Time | $t_r$ | | - | 22 | 45 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 13 | 25 | |
| Fall Time | $t_f$ | | - | 8 | 15 | |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | $T_C$ = 25 °C | - | - | 19 | A |
| Pulse Diode Forward Current | $I_{SM}$ | | - | - | 3 0 | |
| Body Diode Voltage | $V_{SD}$ | $I_S$ = 5 A, $V_{GS}$ = 0 V | - | 0.8 | 1.2 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $I_F$ = 5 A, dI/dt = 100 A/µs, $T_J$ = 25 °C | - | 20 | 40 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | - | 10 | 20 | nC |
| Reverse Recovery Fall Time | $t_a$ | | - | 10.5 | - | ns |
| Reverse Recovery Rise Time | $t_b$ | | - | 9.5 | - | |

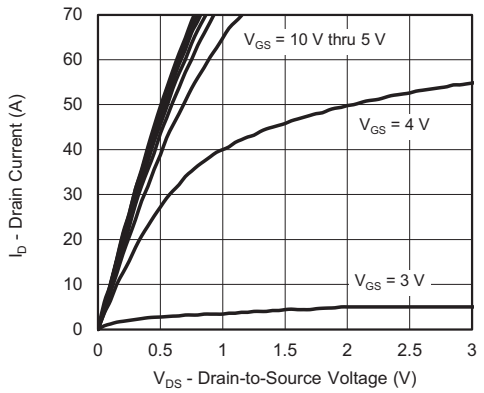
**Notes**

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

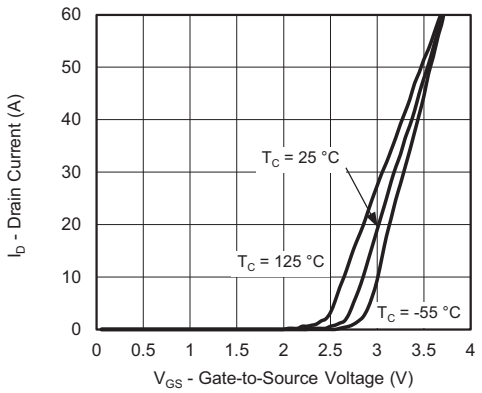
b. Guaranteed by design, not subject to production testing.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

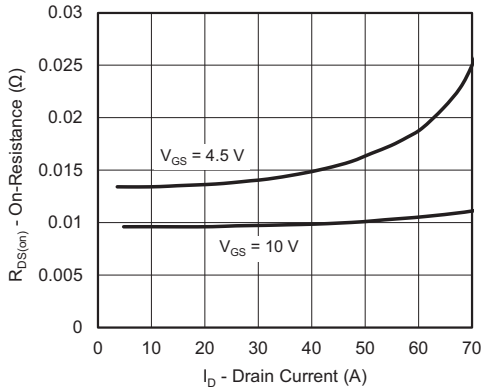
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



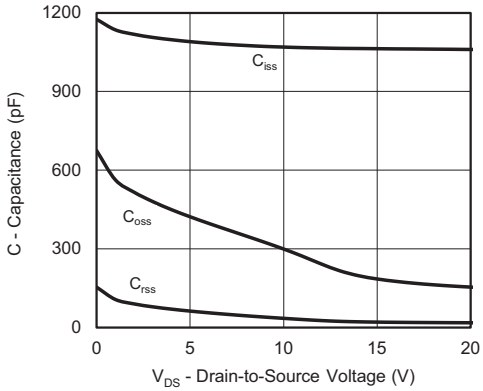

**Output Characteristics**



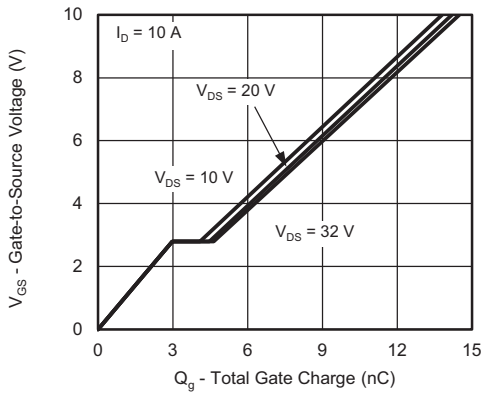

**Transfer Characteristics**



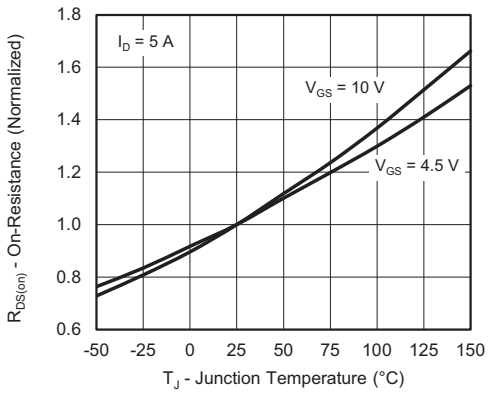

**On-Resistance vs. Drain Current and Gate Voltage**




**Capacitance**

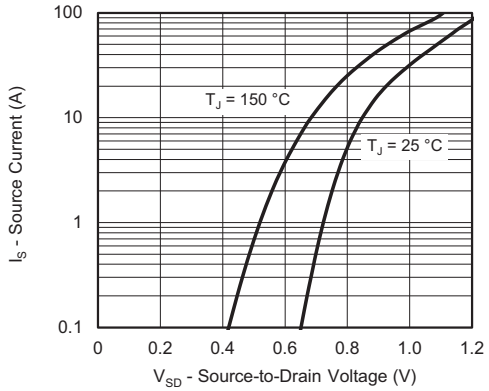



**Gate Charge**

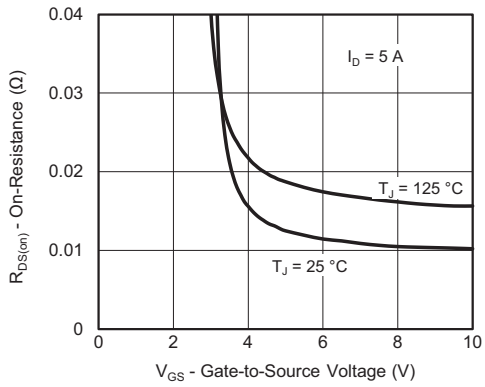



**On-Resistance vs. Junction Temperature**

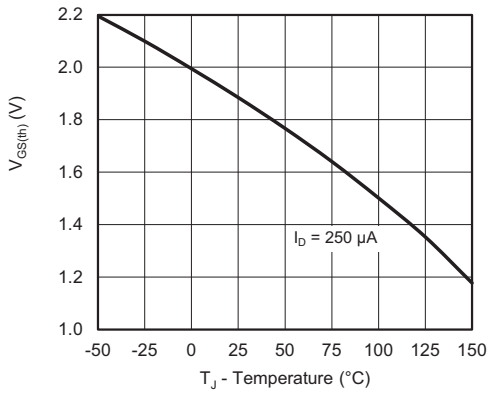
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



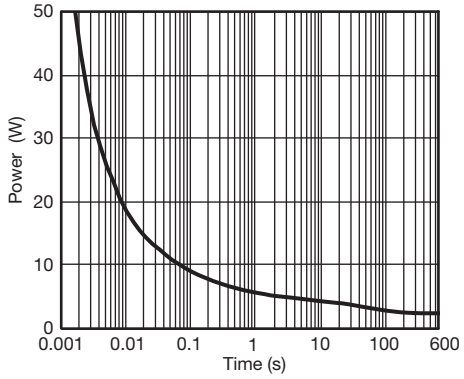

**Source-Drain Diode Forward Voltage**



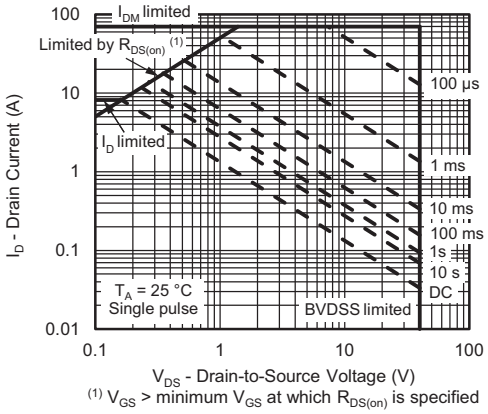

**On-Resistance vs. Gate-to-Source Voltage**




**Threshold Voltage**

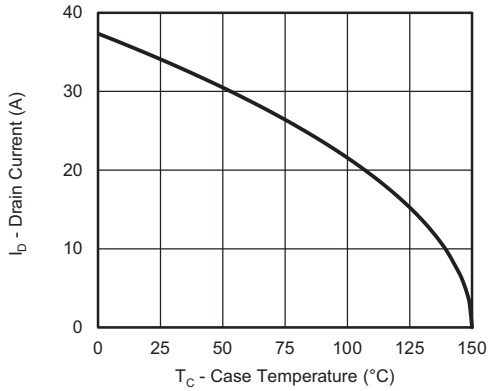



**Single Pulse Power, Junction-to-Ambient**

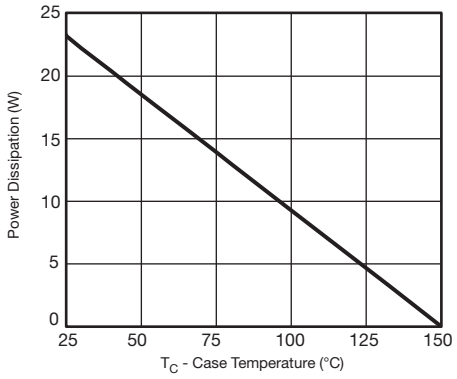



**Safe Operating Area, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)




**Current Derating** [a]

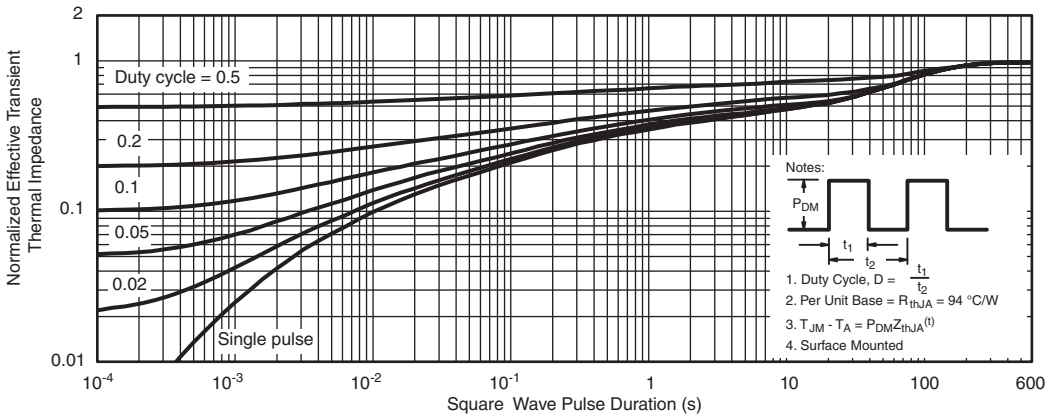



**Power Derating**

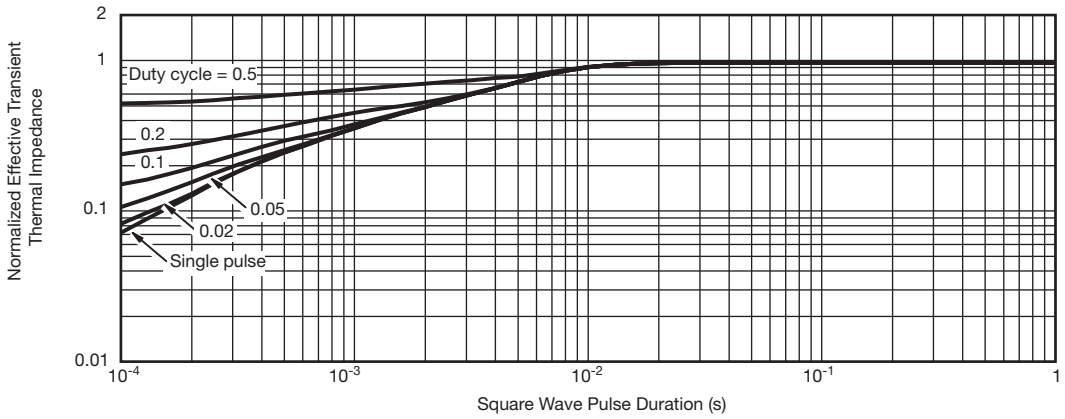
**Note**

a. The power dissipation $P_D$ is based on $T_J$ (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

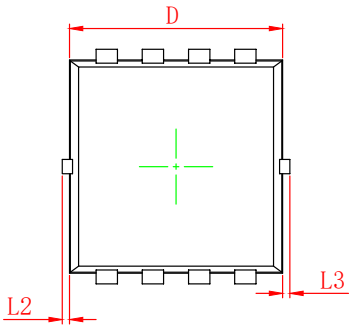



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

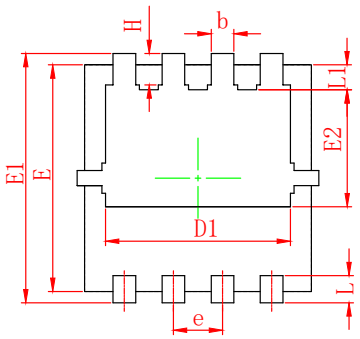



**Normalized Thermal Transient Impedance, Junction-to-Case**

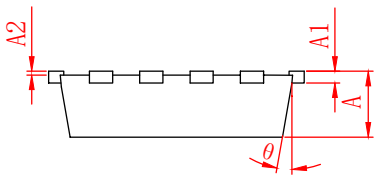
## **PDFNWB3×3-8L** Package Outline Dimensions




Top
[顶视图]




Bottom View
[背视图]

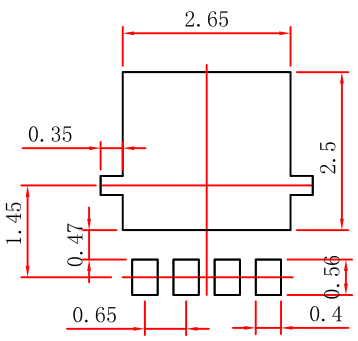



ViewSide
[侧视图]

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.650 | 0.850 | 0.026 | 0.033 |
| A1 | 0.203REF. | | 0.008REF. | |
| A2 | 0~0.05 | | 0~0.002 | |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| D1 | 2.050 | 2.550 | 0.081 | 0.100 |
| E | 2.900 | 3.100 | 0.114 | 0.122 |
| E1 | 3.150 | 3.450 | 0.124 | 0.136 |
| E2 | 1.450 | 1.650 | 0.057 | 0.065 |
| b | 0.200 | 0.400 | 0.008 | 0.016 |
| e | 0.550 | 0.750 | 0.022 | 0.030 |
| L | 0.300 | 0.500 | 0.012 | 0.020 |
| L1 | 0.180 | 0.480 | 0.007 | 0.019 |
| L2 | 0~0.100 | | 0~0.004 | |
| L3 | 0~0.100 | | 0~0.004 | |
| H | 0.315 | 0.515 | 0.012 | 0.020 |
| Φ | 9° | 13° | 9° | 13° |

## Suggested Pad Layout

View




Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

# Disclaimer

All products due to improve reliability, function or design or for other reasons, product specifications and data are subject to change without notice.

Taiwan VBsemi Electronics Co., Ltd., branches, agents, employees, and all persons acting on its or their representatives (collectively, the "Taiwan VBsemi"), assumes no responsibility for any errors, inaccuracies or incomplete data contained in the table or any other any disclosure of any information related to the product.(www.VBsemi.com)

Taiwan VBsemi makes no guarantee, representation or warranty on the product for any particular purpose of any goods or continuous production. To the maximum extent permitted by applicable law on Taiwan VBsemi relinquished: (1) any application and all liability arising out of or use of any products; (2) any and all liability, including but not limited to special, consequential damages or incidental ; (3) any and all implied warranties, including a particular purpose, non-infringement and merchantability guarantee.

Statement on certain types of applications are based on knowledge of the product is often used in a typical application of the general product VBsemi Taiwan demand that the Taiwan VBsemi of. Statement on whether the product is suitable for a particular application is non-binding. It is the customer's responsibility to verify specific product features in the products described in the specification is appropriate for use in a particular application. Parameter data sheets and technical specifications can be provided may vary depending on the application and performance over time. All operating parameters, including typical parameters must be made by customer's technical experts validated for each customer application. Product specifications do not expand or modify Taiwan VBsemi purchasing terms and conditions, including but not limited to warranty herein.

Unless expressly stated in writing, Taiwan VBsemi products are not intended for use in medical, life saving, or life sustaining applications or any other application. Wherein VBsemi product failure could lead to personal injury or death, use or sale of products used in Taiwan VBsemi such applications using client did not express their own risk. Contact your authorized Taiwan VBsemi people who are related to product design applications and other terms and conditions in writing.

The information provided in this document and the company's products without a license, express or implied, by estoppel or otherwise, to any intellectual property rights granted to the VBsemi act or document. Product names and trademarks referred to herein are trademarks of their respective representatives will be all.

# Material Category Policy

**Taiwan VBsemi Electronics Co., Ltd., hereby certify that all of the products are determined to be oHS compliant and meets the definition of restrictions under Directive of the European Parliament 2011/65 / EU, 2011 Nian. 6. 8 Ri Yue restrict the use of certain hazardous substances in electrical and electronic equipment (EEE) - modification, unless otherwise specified as inconsistent.(www.VBsemi.com)**

**Please note that some documents may still refer to Taiwan VBsemi RoHS Directive 2002/95 / EC. We confirm that all products identified as consistent with the Directive 2002/95 / EC European Directive 2011/65 /.**

**Taiwan VBsemi Electronics Co., Ltd. hereby certify that all of its products comply identified as halogen-free halogen-free standards required by the JEDEC JS709A. Please note that some Taiwanese VBsemi documents still refer to the definition of IEC 61249-2-21, and we are sure that all products conform to confirm compliance with IEC 61249-2-21 standard level JS709A.**