Description

The MP1471GJ-Z is a high efficiency 600kHz, Constant on-Time (COT) control mode synchronous step-down DC-DC converter capable of delivering up to 3A current. MP1471GJ-Z integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. Low output voltage ripple and small external inductor and capacitor size are achieved with 600KHz switching frequency . It adopts the COT architecture to achieve fast transie-nt responses for high voltage step down applications. The MP1471GJ-Z requires a minimum number of readily available standard extermal components and is available in a 6-pin SOT23-6 ROHS compliant pa -ckage

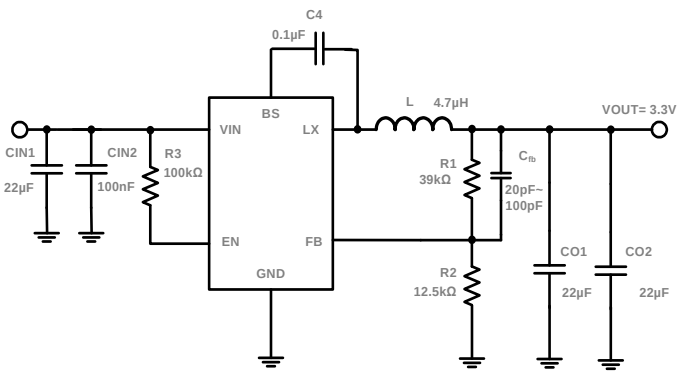
Application

- Digital Set Top Boxes
- Flat Panel Television and Monitors
- Notebook computer
- Wireless and DSL Modems

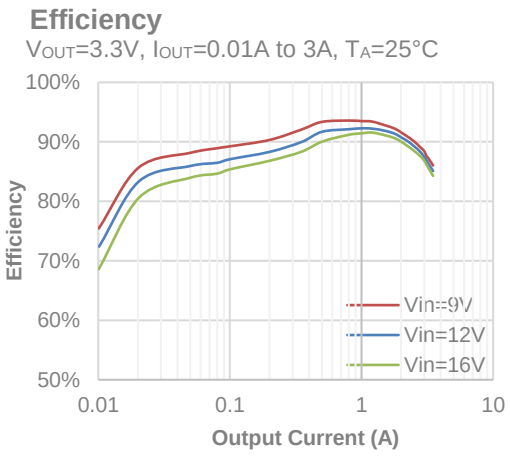
Features

- 70mΩ/35mΩ Low $R_{DS(ON)}$ internal FETs
- High Efficiency Synchronous-Mode Operation
- Wide Input Range:4.5V to 18V
- Output Voltage from 0.8V
- 600kHz Switch Frequency
- Up to 3A, 3.5A@1.2V Output Current
- COT control to achieve fast transient responses
- Power Save Mode at Light Load
- Integrated internal compensation
- Stable with Low ESR Ceramic Output Capacitors
- Over Current Protection with Hiccup Mode
- Thermal Shutdown
- Inrush Current Limit and Soft Start
- Build in Input Over Voltage Protection
- Available in SOT23-6 Package

Typical Application



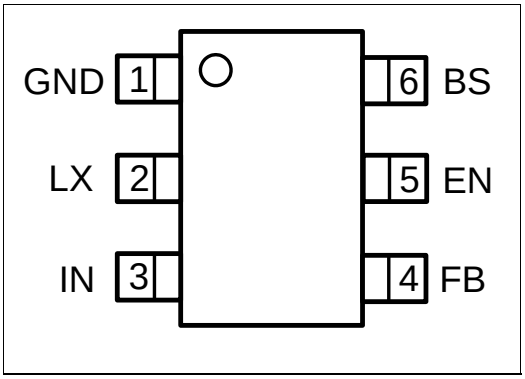
Typical Application Circuits (V_{REF}=0.8V)



Absolute Maximum Ratings (Note 1)

Parameter	Min	Max	Unit
Input Supply Voltage, EN	-0.3	20	V
LX Voltages	-0.3	20	V
LX Voltages (<10ns transient)	-4.5	22	V
FB Voltage	-0.3	6	V
BS Voltage	-0.3	26	V
BS to LX Voltage	-0.3	6	V
Storage Temperature Range	-65	150	°C
Junction Temperature (Note2)	160		°C
Power Dissipation	1000		mW
Lead Temperature (Soldering, 10s)	260		°C

Package



SOT23-6

Order Information

Part Number	Package	Top Marking	Quantity/Reel
MP1471GJ-Z	SOT23-6	TM3xxx	3000

xxx: Inside Code

MP1471GJ-Z devices are Pb-free and RoHS compliant.

Pin Functions

Pin AP1471GJ-Z	Name	Function
1	GND	Ground Pin
2	LX	Switching Pin
3	IN	Power supply Pin
4	FB	Output Voltage feedback input. Connect FB to the center point of the external resistor divider.
5	EN	Drive this pin to a logic-high to enable the IC. Drive to a logic-low to disable the IC and enter micro-power shutdown mode. Don't floating EN.
6	BS	Bootstrap. A capacitor connected between LX and BS pins is required to form a floating supply across the high-side switch driver.

ESD Rating

Items	Description	Value	Unit
V_{ESD_HBM}	Human Body Model for all pins	±2000	V
V_{ESD_CDM}	Charged Device Model for all pins	±1000	V

JEDEC specification JS-001

Recommended Operating Conditions

Items	Description	Min	Max	Unit
Voltage Range	IN	4.5	18	V
T_J	Operating Junction Temperature	-40	125	°C

Thermal Resistance (Note3)

Items	Description	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	100	°C/W
θ_{JC}	Junction-to-case(top) thermal resistance	56	°C/W
θ_{JB}	Junction-to-board thermal resistance	16.2	°C/W
ψ_{JC}	Junction-to-case(top) characterization parameter	2.0	°C/W

Electrical Characteristics

V_{IN}=12V, V_{OUT}=3.3V, T_A = 25°C, unless otherwise noted.

Parameter	Conditions	Min	Typ.	Max	Units
Input Voltage Range		4.5		18	V
OVP Threshold		18.7	19.3	19.8	V
UVLO Rising Threshold			4.3		V
UVLO Hysteresis			0.35		V
Quiescent Current	V_{EN}=2V, V_{FB}=V_{REF} x 105%		300		μA
Shutdown Current	V_{IN}=12V, EN=0V		5	10	μA
Regulated Feedback Voltage	T_A=25°C,4.5V≤V_{IN}≤18V	0.784	0.8	0.816	V
High-Side Switch On-Resistance			70		mΩ
Low-Side Switch On-Resistance			35		mΩ
High-Side Switch Leakage Current	V_{EN}=0V, V_{LX}=0V	1		10	μA
Switch Valley Current Limit	Minimum Duty Cycle	3.7	4	4.5	A
On Time	V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=1A	132	166	200	ns
Oscillation Frequency	Maximum Duty Cycle	450	600	750	kHz
Maximum Duty Cycle			90		%
Minimum On-Time(Note 4)			80		ns
Soft Start Time		0.5	0.8	1.2	ms
Hiccup on Time(Note 4)			1.2		ms
Hiccup Time Before Restart(Note 4)			3.6		ms
EN Rising Threshold		0.85	0.95	1.05	V
EN Hysteresis			180		mV
Thermal Shutdown Threshold (Note 4)			165		°C
Thermal Shutdown Hysteresis (Note 4)			30		°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.
Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + P_D \times \theta_{JA}$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D\,(MAX)} = (T_{J(MAX)}-T_A)/\theta_{JA}$.
Note 3: Measured on JESD51-7, 4-layer PCB.
Note 4: Guaranteed by design.

Block Diagram

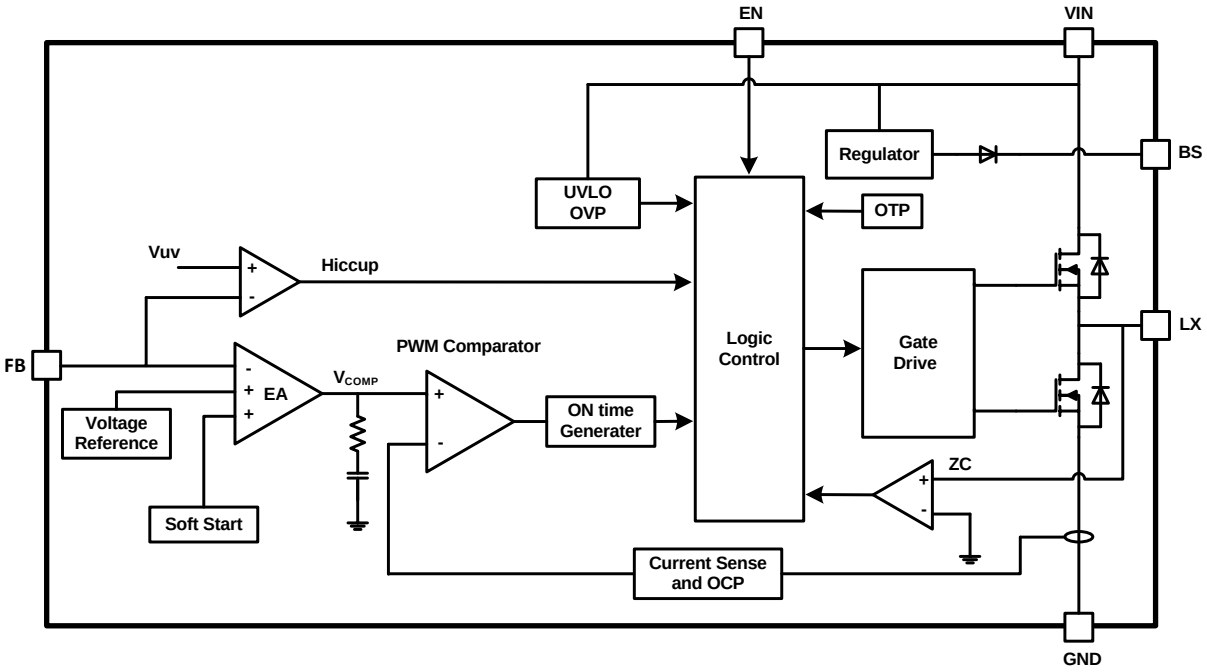


Figure 1. MP1471GJ-Z Block Diagram

Operation Description

Internal Regulator

The MP1471GJ-Z is a constant on-time (COT) step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains low resistance, high voltage high side and low side power MOSFETs, and operates at 600kHz operating frequency to ensure a compact, high efficiency design with excellent AC and DC performance.

Error Amplifier

MP1471GJ-Z adopts operational transconductance amplifier (OTA) as error amplifier. The error amplifier compares the FB pin voltage with the internal FB reference (V_{REF}) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the V_{COMP} voltage, which is used to compare with the low side power MOSFET current sensing signal and trigger on time pulse. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to V_{REF}. When it is lower than the internal FB reference (V_{REF}), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than V_{REF}, V_{REF} regains control. The SS time is internally fixed to 0.8ms typically.

Over-Current-Protection and Short Circuits Protection

The MP1471GJ-Z has cycle-by-cycle valley current limit function. When the inductor current valley value is larger than the valley current limit during low side MOSFET on state, the device enters into valley over current protection mode and low side MOSFET keeps on state until inductor current drops down to the value equal or lower than the valley current limit, and then on time pulse could be generated and high side MOSFET could turn on again.

If the output is short to GND and the output voltage drop until feedback voltage V_{FB} is below the output under-voltage V_{UV} threshold which is typically 46% of V_{REF}, MP1471GJ-Z enters into hiccup mode to periodically disable and restart switching operation. The hiccup mode helps to reduce power dissipation and thermal rise during output short condition. The period of MP1471GJ-Z hiccup mode is typically 4.8ms.

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts switching operation. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The V_{COMP} voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Application Information

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). Choose R1 to be around 39kΩ for optimal transient response. R2 is then given by:

Table 1: Selection for Common Output Voltages (V_{FB}=0.8V)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{FB}(pF)	L (μH)
5	39	7.43	33	4.7
3.3	39	12.5	33	4.7
2.5	39	18.3	33	3.3
1.8	39	31.2	33	2.2
1.5	39	44.6	33	2.2
1.2	39	78	33	1.5
1	18	72	33	1.0

$$R_2 = \frac{R_1}{V_{out}/V_{FB} - 1}$$

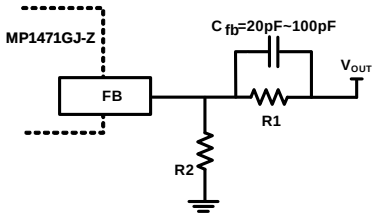


Figure 2. Feedback Network

Selecting the Inductor

A 1.0μH to 4.7μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be as small as possible. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{out} \times (V_{in} - V_{out})}{V_{in} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current. Choose inductor ripple current to be approximately 30% if the maximum load current 3A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Selecting the Output Capacitor

The output capacitor (Co1 and Co2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times \left[R_{ESR} + \frac{1}{8 \times f_S \times C_2}\right]$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^{\,2} \times L \times C_2} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

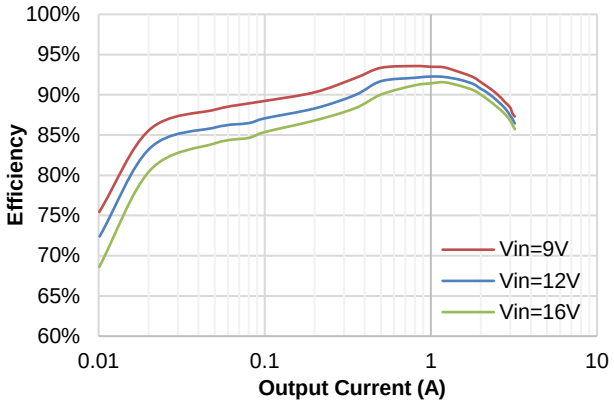
$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP1471GJ-Z can be optimized for a wide range of capacitance and ESR values.

Typical Performance Characteristics

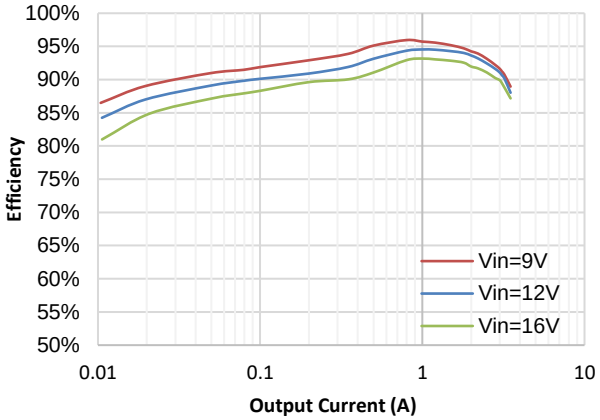
Efficiency

V_{OUT} =3.3V, L=4.7µH, DCR=30mΩ



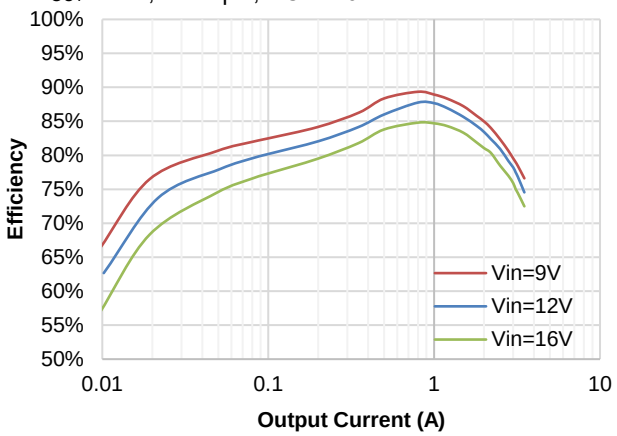
Efficiency

V_{OUT} =5V, L=4.7µH, DCR=30mΩ



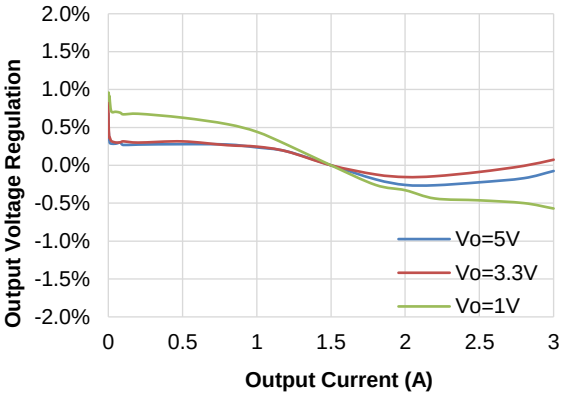
Efficiency

V_{OUT}=1.2V, L=2.2µH, DCR=20mΩ



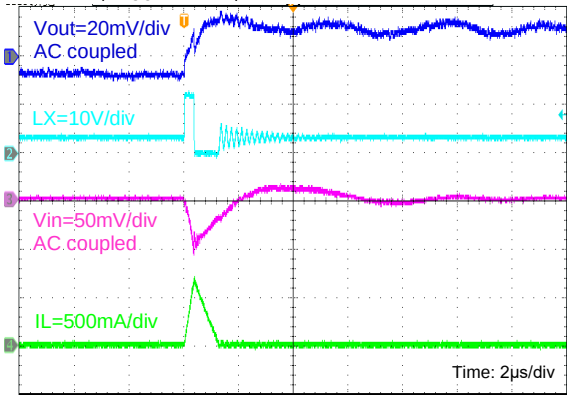
Load Regulation

V_{IN}=12V, T_A=25°C



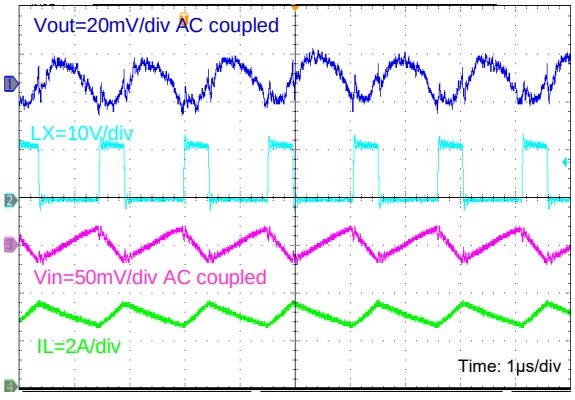
Steady State Operation

V_{IN} =12V, V_{OUT} =3.3V, No Load



Steady State Operation

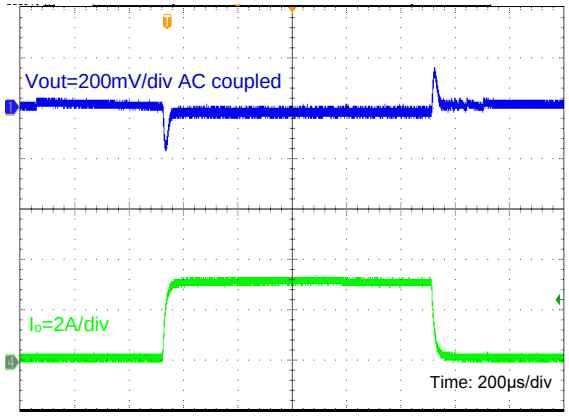
V_{IN} =12V, V_{OUT} =3.3V, I_o=Full Load



Typical Performance Characteristics(continued)

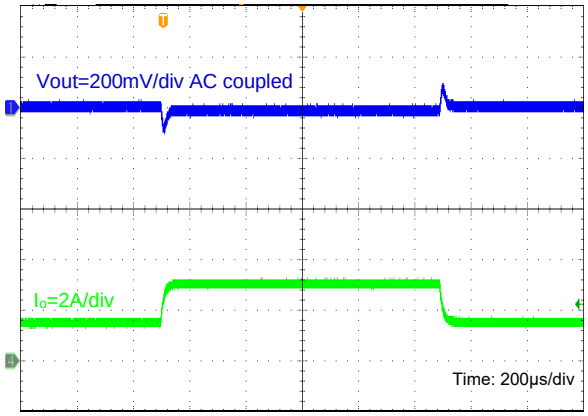
Load Transient

V_{IN} =12V, V_{OUT} =3.3V, I_o =0A to 3A



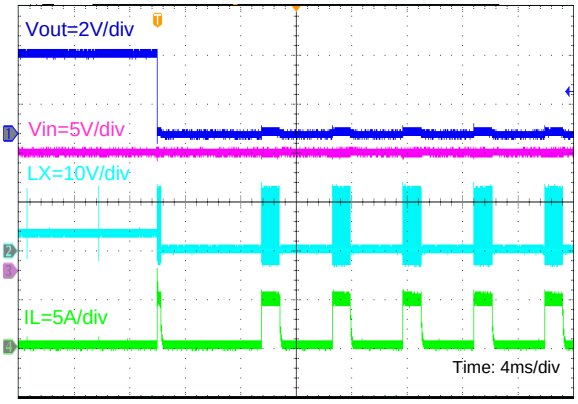
Load Transient

V_{IN} =12V, V_{OUT} =3.3V, I_o =1.5A to 3A



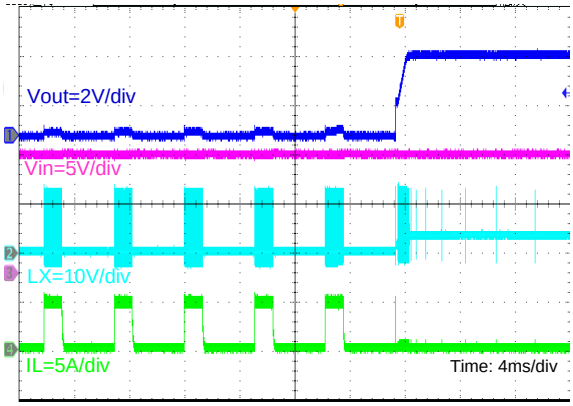
Output Short Entry

V_{IN} =12V, V_{OUT} =3.3V, No Load



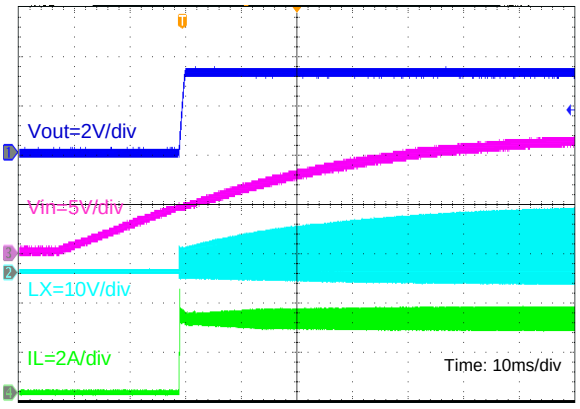
Output Short Recovery

V_{IN}=12V, V_{OUT} =3.3V, No Load



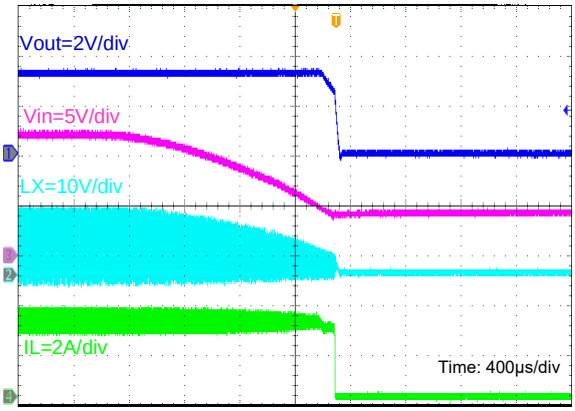
Input Power On

V_{IN} =12V, V_{OUT} =3.3V, I_o =Full Load



Input Power Down

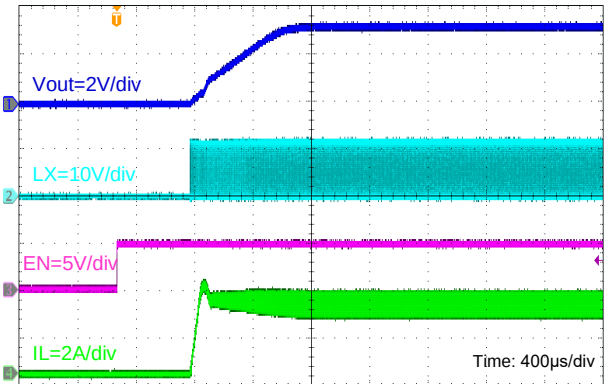
V_{IN} =12V, V_{OUT} =3.3V, I_o =Full Load



Typical Performance Characteristics(continued)

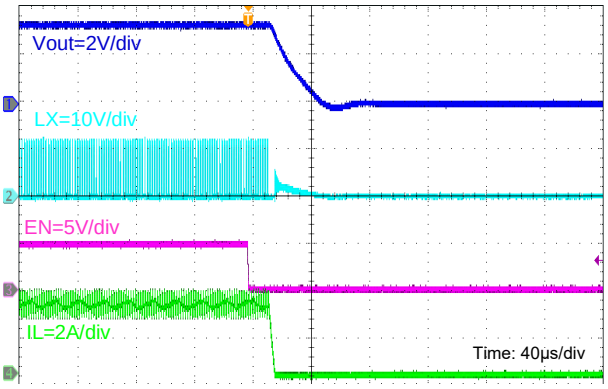
EN Enable

V_{IN} =12V, V_{OUT} =3.3V, I_o =Full Load



EN Disable

V_{IN} =12V, V_{OUT} =3.3V, I_o =Full Load



Typical Application Circuits

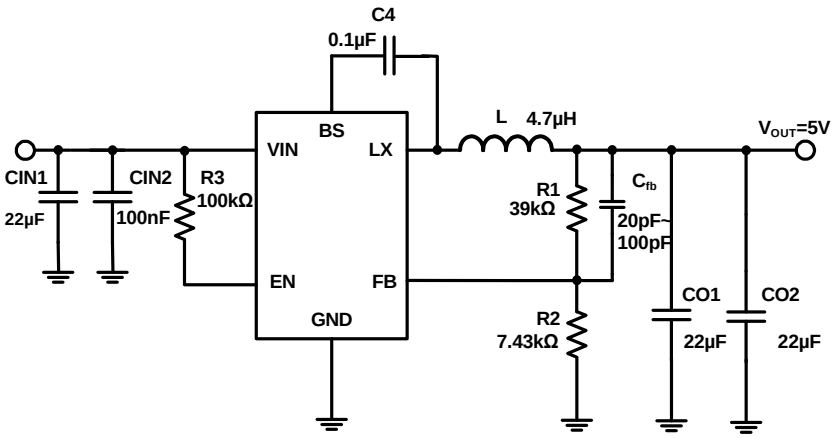


Figure 4. 12V_{IN}, 5V Output (V_{FB}=0.8V)

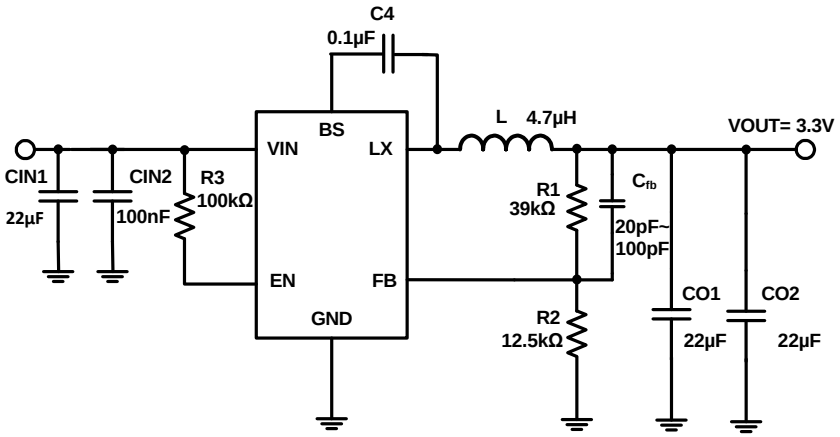


Figure 5. 12V_{IN}, 3.3V Output (V_{FB}=0.8V)

Typical Application Circuits(continued)

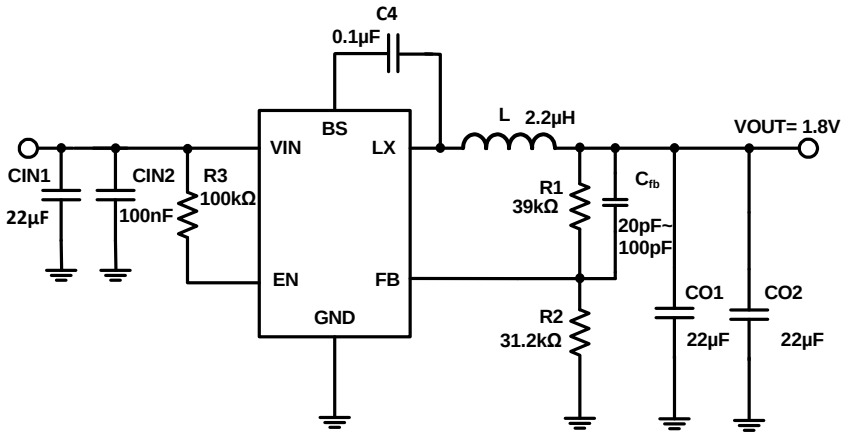


Figure 6. 12V_{IN}, 1.8V Output (V_{FB}=0.8V)

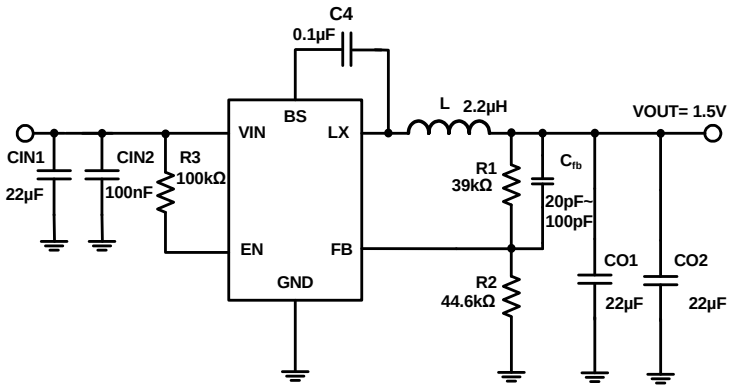


Figure 7. 12V_{IN}, 1.5V Output (V_{FB}=0.8V)

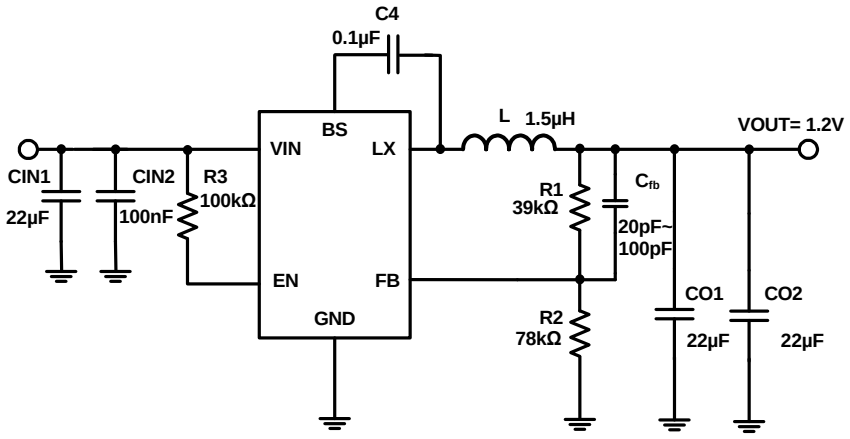


Figure 8. 12V_{IN}, 1.2V Output (V_{FB}=0.8V)

Typical Application Circuits(continued)

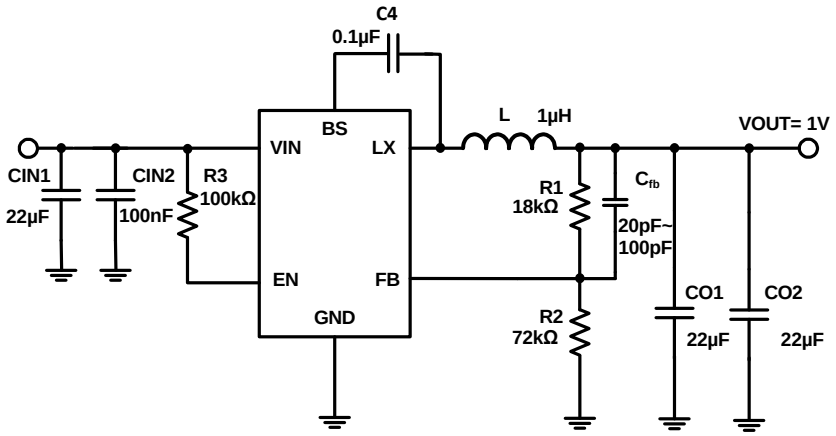


Figure 9. 12V_{IN}, 1V Output (V_{FB}=0.8V)

PCB Layout Guide

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines and take Figure 3 for reference.

1) Keep the path of switching current short and minimize the loop area formed by Input capacitor, IN pin and GND.

2) Bypass ceramic capacitors are suggested to be put close to the IN Pin.

3) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the chip as possible.

4) VOUT, LX away from sensitive analog areas such as FB.

5) Connect IN, LX, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

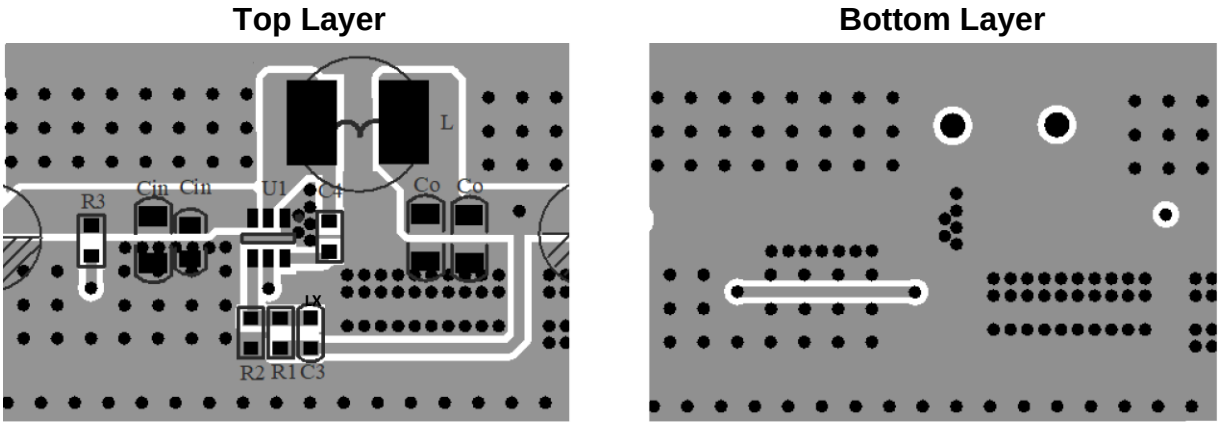
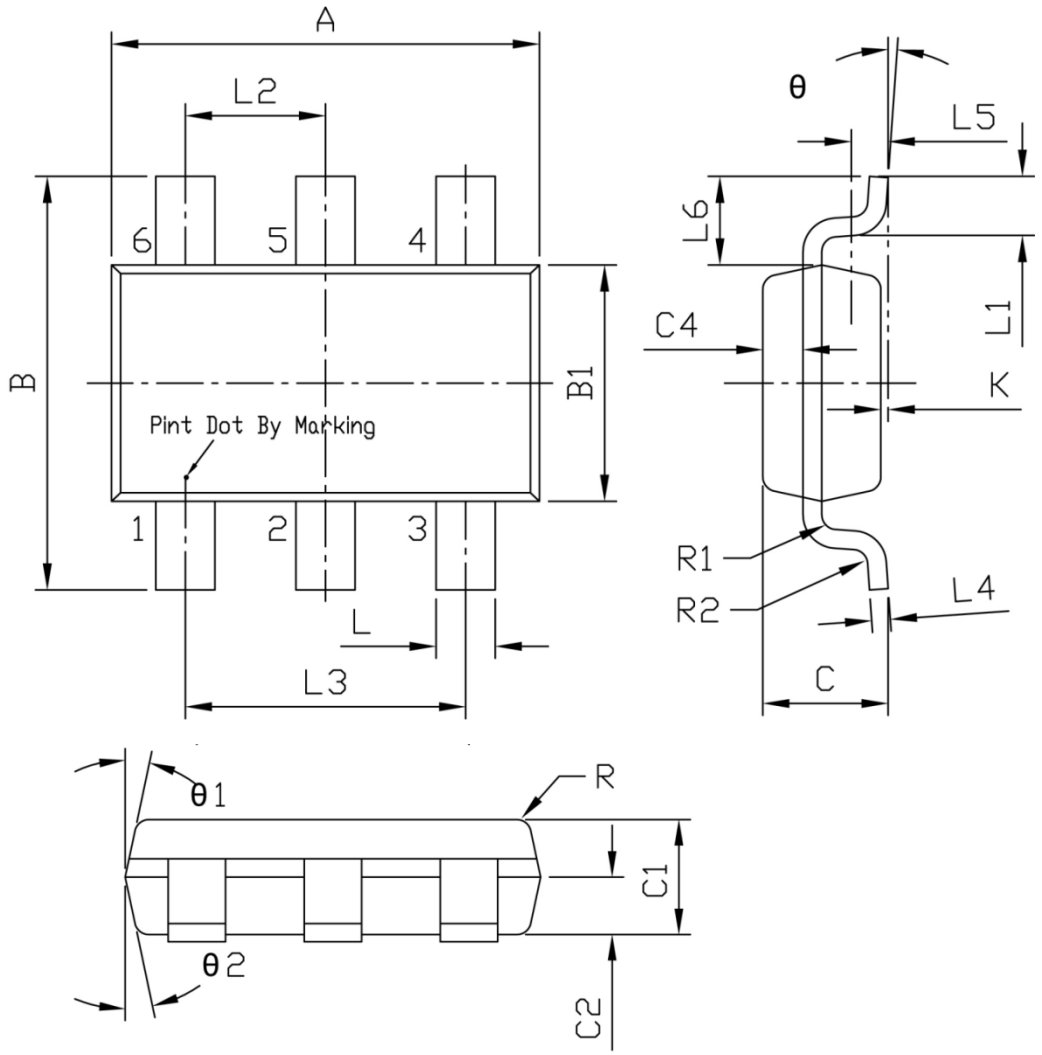


Figure 3. Sample of PCB Layout

Package Information

SOT23-6

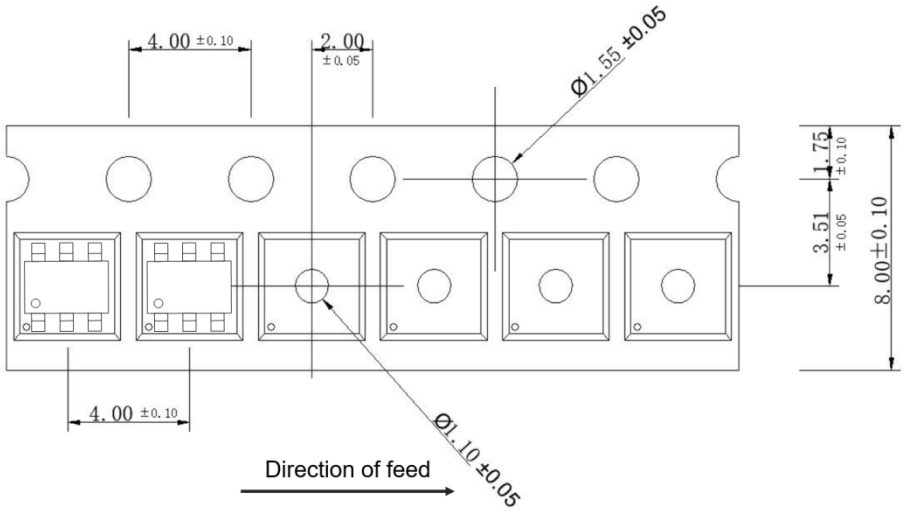


Unit: mm

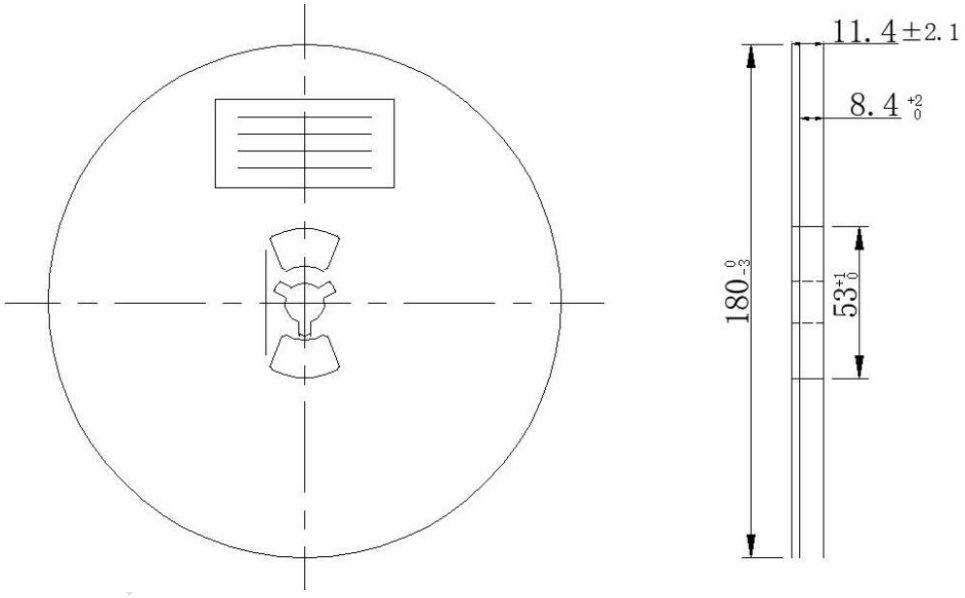
Symbol	Dimensions In Millimeters			Symbol	Dimensions In Millimeters		
	Min	Typ	Max		Min	Typ.	Max
A	2.80	2.90	3.00	L3	1.800	1.900	2.000
B	2.60	2.80	3.00	L4	0.077	0.127	0.177
B1	1.50	1.60	1.70	L5	-	0.250	-
C	-	-	1.05	L6	-	0.600	-
C1	0.60	0.80	1.00	θ	0°		0°
C2	0.35	0.40	0.45	Θ1	10°	12°	14°
C4	0.223	0.273	0.323	Θ2	10°	12°	14°
K	0.000	0.075	0.150	R	-	0.100	-
L	0.325	0.400	0.475	R1	-	0.100	-
L1	0.325	0.450	0.550	R2	-	0.100	-
L2	0.850	0.950	1.050				

Tape and Reel Information

Tape Dimensions:



Reel Dimensions:



Note:

1) All Dimensions are in Millimeter
2) Quantity of Units per Reel is 3000
3) MSL level is Level 3.