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ESD Protection Diodes

Micro−packaged Diodes for ESD Protection

ESDM2033

The ESDM2033 is designed to protect voltage sensitive components from ESD. Excellent clamping capability, low leakage, and fast response time provide best in class protection on designs that are exposed to ESD. Because of its small size, it is suited for use in smartphone, smart-watch, or many other portable / wearable applications where board space comes at a premium.

Features

- Low Capacitance (5.5 pF Max, I/O to GND)
- Small Body Outline Dimensions
  - 0.6 x 0.3 mm
- Protection for the Following IEC Standards:
  IEC 61000−4−2 (Level 4)
- Low ESD Clamping Voltage
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
IEC 61000−4−2 Contact (ESD) IEC 61000−4−2 Air (ESD)	ESD ESD	±15 ±15	kV kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

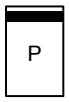
See Application Note AND8308/D for further description of survivability specs.

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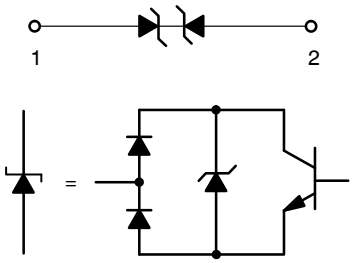
X4DFN2
(0201)
CASE 152AX

MARKING DIAGRAM



P = Specific Device Code

PIN CONFIGURATION AND SCHEMATIC



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			3.3	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	3.68	5.0	6.5	V
Reverse Leakage Current	I_R	V_{RWM} = 3.3 V, I/O Pin to GND			0.1	μA
Clamping Voltage TLP (Note 1)	V_C	I_{PP} = 8 A } IEC 61000−4−2 Level 2 equivalent (±4 kV Contact, ±4 kV Air)		5.5		V
		I_{PP} = 16 A } IEC 61000−4−2 Level 2 equivalent (±8 kV Contact, ±15 kV Air)		6.5		
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz			5.5	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.

ORDERING INFORMATION

Device	Package	Shipping†
ESDM2033MX4T5G	X4DFN2 (Pb−Free)	10,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

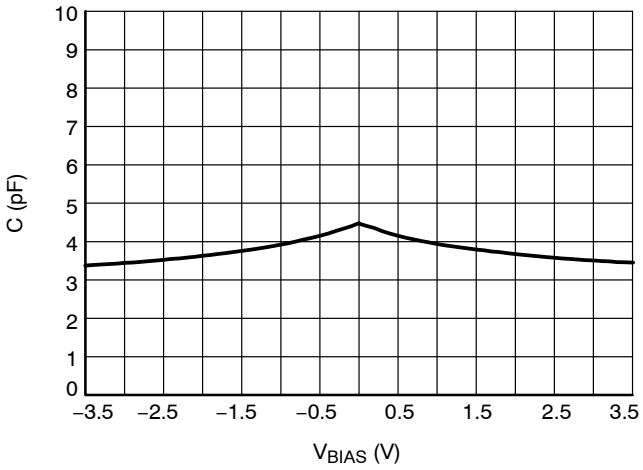


Figure 1. CV Characteristics

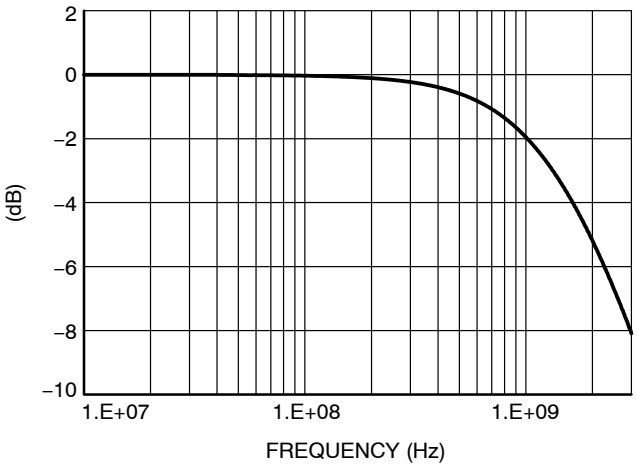


Figure 2. S21 Insertion Loss

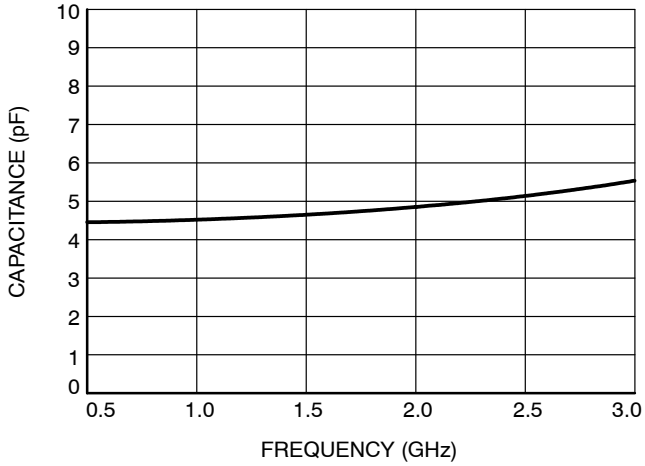


Figure 3. Capacitance over Frequency

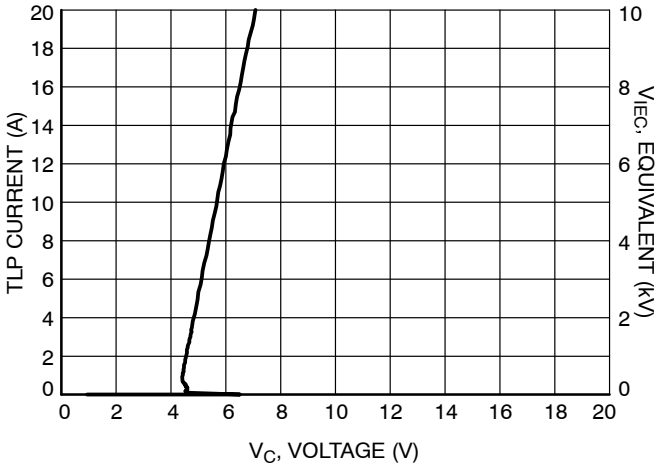


Figure 4. Positive TLP I−V Curve

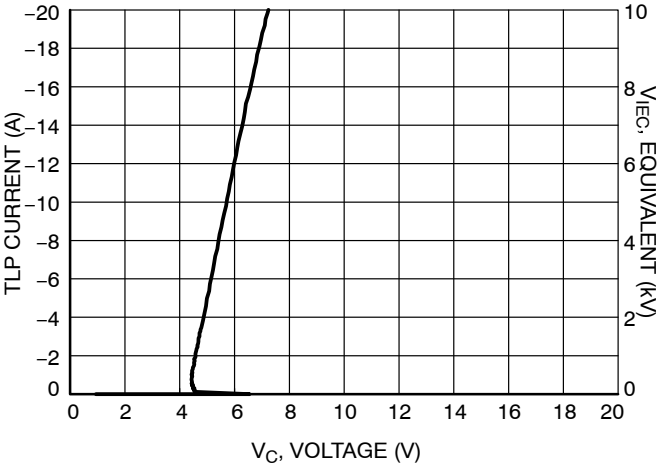


Figure 5. Negative TLP I−V Curve

TYPICAL CHARACTERISTICS

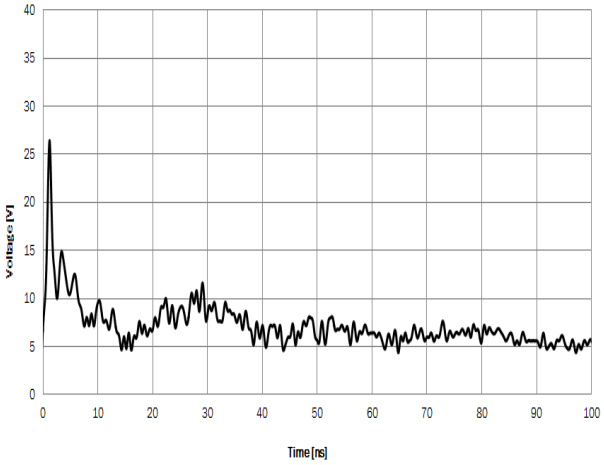


Figure 6. Positive 8 kV ESD Contact Discharge

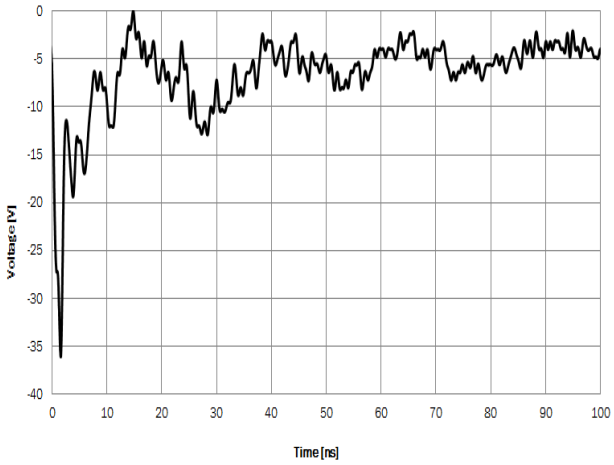


Figure 7. Negative 8 kV ESD Contact Discharge

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

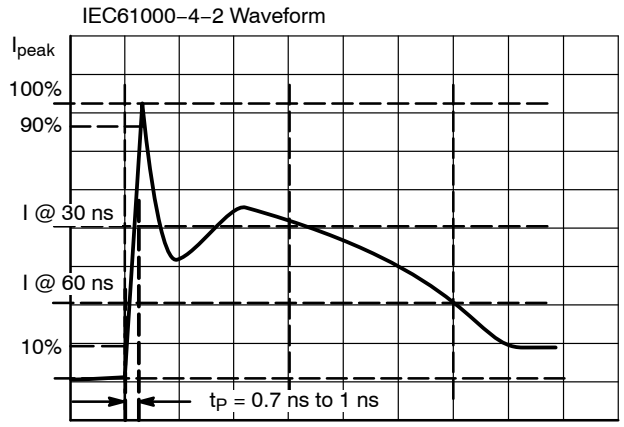


Figure 8. IEC61000−4−2 Spec

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 9. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 10 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

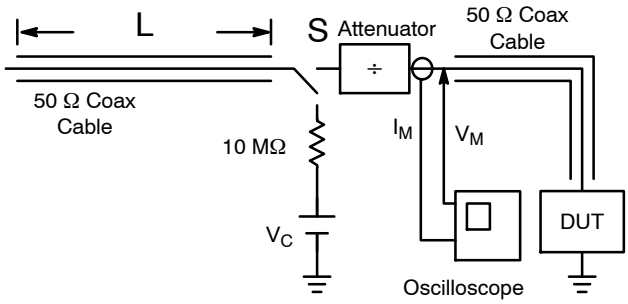


Figure 9. Simplified Schematic of a Typical TLP System

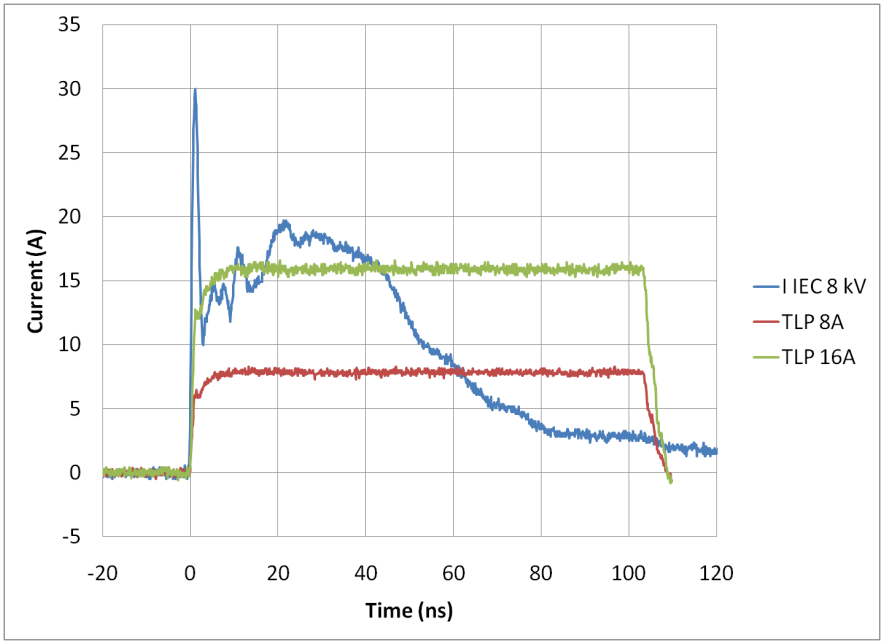
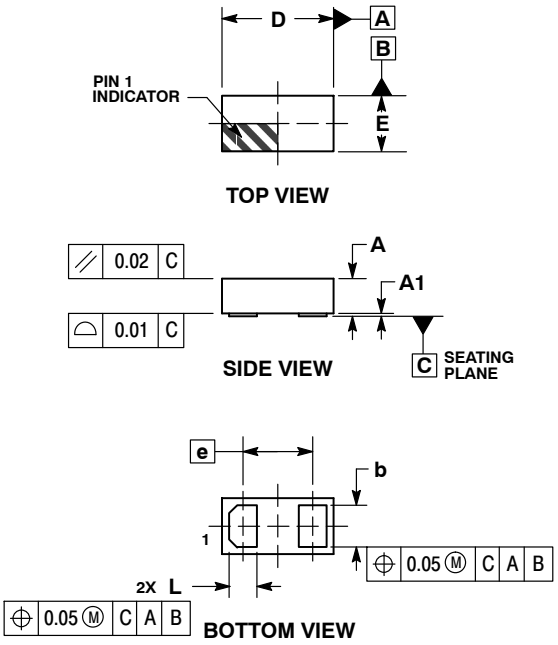


Figure 10. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

ESDM2033

PACKAGE DIMENSIONS

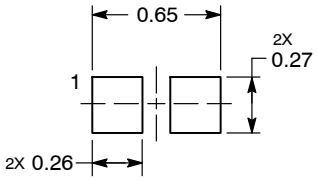
DFN2, 0.60x0.30, 0.36P
CASE 152AX
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.175	0.200	0.225
A1		0.018 REF	
b	0.205	0.215	0.225
D	0.575	0.600	0.625
E	0.275	0.300	0.325
e		0.36 BSC	
L	0.145	0.155	0.165

RECOMMENDED SOLDER FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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