

钍地半导体
Tudi Semiconductor

Product Specification

TUDI-25LC1024-E/P

1-Mbit SPI Bus Serial EEPROM

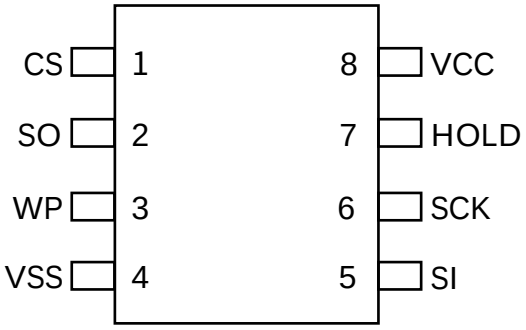
网址 www.sztdbdt.com

用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features



DIP8 Pin Configuration

- ●20 MHz Maximum Clock Speed
- ●Byte and Page-Level Write Operations:
  - 256-byte page
  - 6 ms maximum write cycle time
  - No page or sector erase required
- ●Low-Power CMOS Technology:
  - Maximum Write current: 5 mA at 5.5V, 20 MHz
  - Read current: 7 mA at 5.5V, 20 MHz
  - Standby current: 1 µA at 2.5V (Deep power-down)
- ●Electronic Signature for Device ID
- ●Self-Timed Erase and Write Cycles:
  - Page Erase (6 ms maximum)
  - Sector Erase (10 ms maximum)
  - Chip Erase (10 ms maximum)
- ●Sector Write Protection (32K byte/sector):
  - Protect none, 1/4, 1/2 or all of array
- ●Built-In Write Protection:
  - Power-on/off data protection circuitry
  - Write enable latch
  - Write-protect pin
- ● High Reliability:
  - Endurance: 1M erase/write cycles
  - Data Retention: >200 years
  - ESD Protection: >4000V
- ●Temperature Ranges Supported:
  - Industrial (I): -40C to +85C
  - Extended (E): -40 ° C to +125 ° C
- ●RoHS Compliant

Description

The 25LC1024 is a 1024-Kbit serial EEPROM memory with byte-level and page-level serial EEPROM functions. It also features Page, Sector and Chip erase instructions typically associated with Flash-based products. These instruc-tions are not required for byte or page write operations. The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled by a Chip Select (CS) input. Communication to the device can be paused via the hold pin (HOLD). While the device is paused, transi-tions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

Absolute Maximum Ratings

V_{CC}.....6.5V All inputs and outputs w.r.t.
V_{SS} .....-0.6V to V_{CC} +1.0V.
Storage temperature .....-65°C to +150°C
Ambient temperature under bias.....-40°C to +125°C ESD
protection on all pins.....4 kV

NOTICE: Stresses above those listed under “ Absolute Maximum Ratings ” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in theoperational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

Pin Function

Name	Function
CS	Chip Select Input
SO	Serial Data Output
WP	Write-Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
HOLD	Hold Input
V_{CC}	Supply Voltage

PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 1.

TABLE 1: PIN FUNCTION TABLE

Name	8-Lead PDIP	Function
CS	1	Chip Select Input
SO	2	Serial Data Output
WP	3	Write-Protect Pin
Vss	4	Ground
SI	5	Serial Data Input
SCK	6	Serial Clock Input
HOLD	7	Hold Input
Vcc	8	Supply Voltage

TABLE 2: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial(I):TA=-40℃ to +85℃,Vcc=2.5V to 5.5VExtended(E): TA=-40℃ to +125℃,Vcc=2.5V to 5.5V			
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Test Conditions
D001	V_{IH1}	High-Level Input Voltage	0.7 Vcc	Vcc+1	V	
D002	V_{IL1}	Low-Level Input Voltage	-0.3	0.3 Vcc	V	Vcc≥2.7V
D003	V_{IL2}		-0.3	0.2 Vcc	V	Vcc<2.7V
D004	V_{OL}	Low-level Output Voltage	—	0.4	V	I_{OL}=2.1 mA
D005	V_{OH}	High-Level Output Voltage	Vcc -0.2	—	V	I_{OH}=-400 μA
D006	I_{LI}	Input Leakage Current	—	± 1	μA	CS=Vcc,V_{IN}=Vss or Vcc
D007	I_{LO}	Output Leakage Current	—	±1	μA	CS =Vcc,V_{OUT}=Vss or Vcc
D008	C_{INT}	Internal Capacitance(all inputs and outputs)	—	7	pF	TA=+25℃,CLK=1.0 MHz, Vcc=5.0V(Note 1)
D009	Icc Read	Operating Current	—	10	mA	Vcc=5.5V;F_{CLK}=20.0 MHz; SO=Open
			—	5	mA	Vcc=2.5V;F_{CLK}=10.0 MHz; SO=Open
D010	Icc Write		—	7	mA	Vcc=5.5V
			—	5	mA	Vcc=2.5V
D011	Iccs	Standby Current	—	20	μA	CS=Vcc=5.5V,Inputs tied toVcc or Vss,+125℃
			—	12	μA	CS=Vcc=5.5V,Inputs tied toVcc or Vss,+85℃
D012	I_{CCSPD}	Deep Power-Down Current	—	1	μA	CS=Vcc=2.5V,Inputs tied toVcc or Vss,+85℃
			—	2	μA	CS=Vcc=2.5V,Inputs tied toVcc or Vss,+125℃

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 3: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I):TA=-40°℃ to+85℃,Vcc=2.5V to 5.5V Extended (E):TA=-40℃ to+125℃,Vcc=2.5V to 5.5V			
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Conditions
1	FCLK	Clock Frequency	—	20	MHz	4.5V≤Vcc≤5.5V(I)
			—	10	MHz	2.5V≤Vcc<5.5V(I,E)
2	Tcss	CS Setup Time	25	—	ns	4.5V≤Vcc≤5.5V(I)
			50	—	ns	2.5V≤Vcc<5.5V(I,E)
3	TCSH	CS Hold Time	50	—	ns	4.5V≤Vcc≤5.5V(I)
			100	—	ns	2.5V≤Vcc<5.5V(I,E)
4	TCSD	CS Disable Time	50	—	ns	
5	Tsu	Data Setup Time	5	—	ns	4.5V≤Vcc≤5.5V(I)
			10	—	ns	2.5V≤Vcc<5.5V(I,E)
6	THD	Data Hold Time	10	—	ns	4.5V≤Vcc≤5.5V(I)
			20	—	ns	2.5V≤Vcc<5.5V(I,E)
7	TR	CLK Rise Time	—	20	ns	Note 1
8	TF	CLK Fall Time	—	20	ns	Note 1
9	THI	Clock High Time	25	—	ns	4.5V≤Vcc≤5.5V(I)
			50	—	ns	2.5V≤Vcc<5.5V(I,E)
10	TLO	Clock Low Time	25	—	ns	4.5V≤Vcc≤5.5V(I)
			50	—	ns	2.5V≤Vcc<5.5V(I,E)
11	TCLD	Clock Delay Time	50	—	ns	
12	TCLE	Clock Enable Time	50	—	ns	
13	Tv	Output Valid from Clock Low	—	25	ns	4.5V≤Vcc≤5.5V(I)
			—	50	ns	2.5V≤Vcc<5.5V(I,E)
14	THO	Output Hold Time	0	—	ns	Note 1

TABLE 3: AC CHARACTERISTICS (continued)

AC CHARACTERISTICS			Industrial (I):TA=-40°℃ to+85℃,Vcc=2.5V to 5.5V Extended (E):TA=-40℃ to+125℃,Vcc=2.5V to 5.5V			
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Conditions
15	TDIS	Output Disable Time	—	25	ns	4.5V≤Vcc≤5.5V(I)
			—	50	ns	2.5V≤Vcc<5.5V(I,E)
16	THS	HOLD Setup Time	10	—	ns	4.5V≤Vcc≤5.5V(I)
			20	—	ns	2.5V≤Vcc<5.5V(I,E)
17	THH	HOLD Hold Time	10	—	ns	4.5V≤Vcc≤5.5V(I)
			20	—	ns	2.5V≤Vcc<5.5V(I,E)
18	THZ	HOLD Low to Output High-Z	—	15	ns	4.5V≤Vcc≤5.5V(I)
			—	30	ns	2.5V≤Vcc<5.5V(I,E)(Note 1)
19	THV	HOLD High to Output Valid	—	15	ns	4.5V≤Vcc≤5.5V(I)
			—	30	ns	2.5V≤Vcc<5.5V(I,E)
20	TREL	CS High to Standby Mode	—	100	μs	
21	TPD	CS High to Deep Power-Down	—	100	μS	
22	TCE	Chip Erase Cycle Time	—	10	ms	
23	TSE	Sector Erase Cycle Time	—	10	ms	
24	TWC	Internal Write Cycle Time	—	6	ms	Byte or Page mode and PageErase
25		Endurance	1M	—	E/W Cycles	Page mode,+25℃,5.5V(Note 2)

Note 1: This parameter is periodically sampled and not 100% tested.
2: This parameter is not tested but established by characterization and qualification.

TABLE 4: AC TEST CONDITIONS

AC Waveform	
V_{LO}=0.2V	—
V_{HI}=Vcc-0.2V	Note 1
V_{HI}=4.0V	Note 2
C_L=30 pF	—
Timing Measurement Reference Level	
Input	0.5 Vcc
Output	0.5 Vcc

Note 1: For VCC ≤ 4.0V
2: For VCC > 4.0V

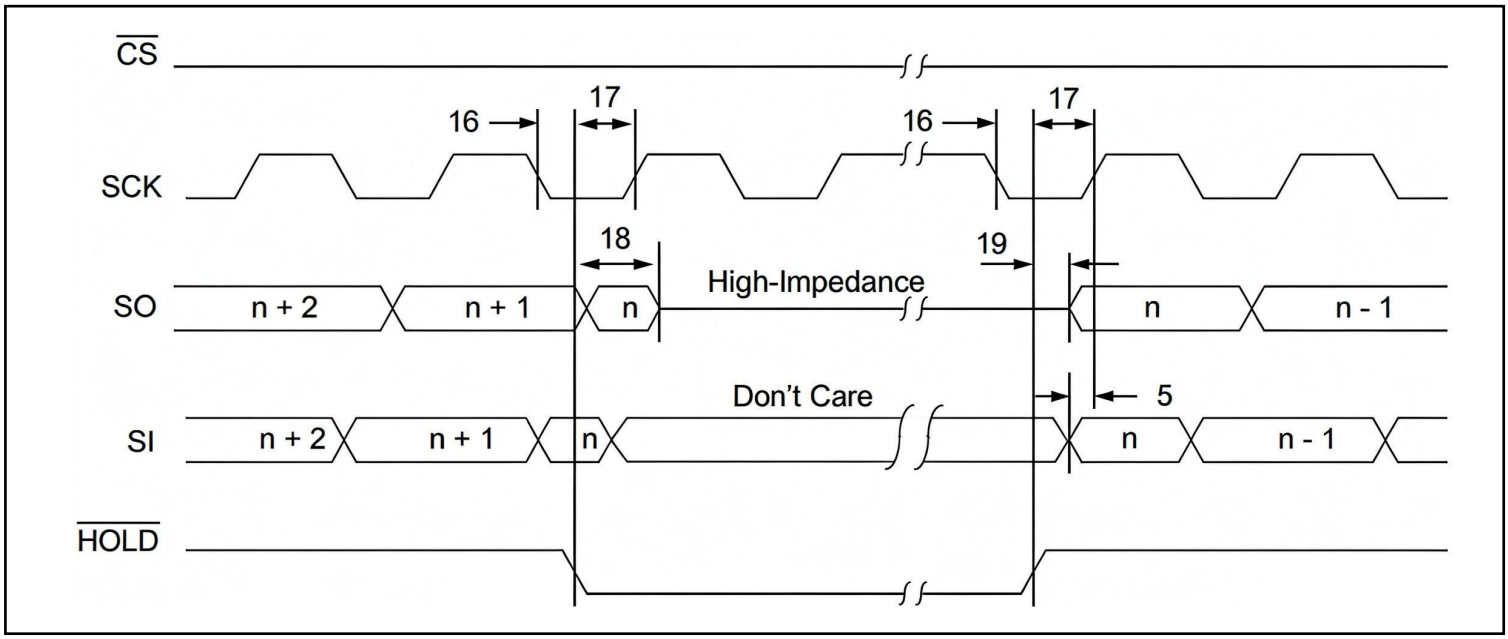


FIGURE 1: HOLD TIMING

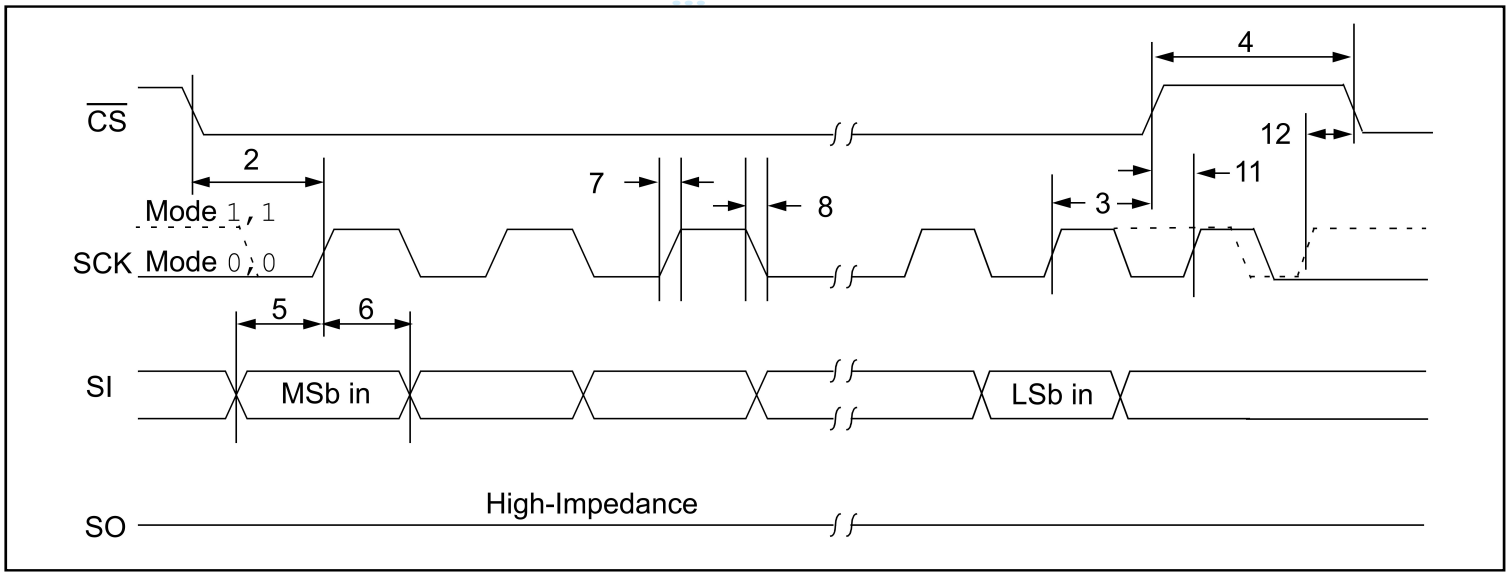


FIGURE 2: SERIAL INPUT TIMING

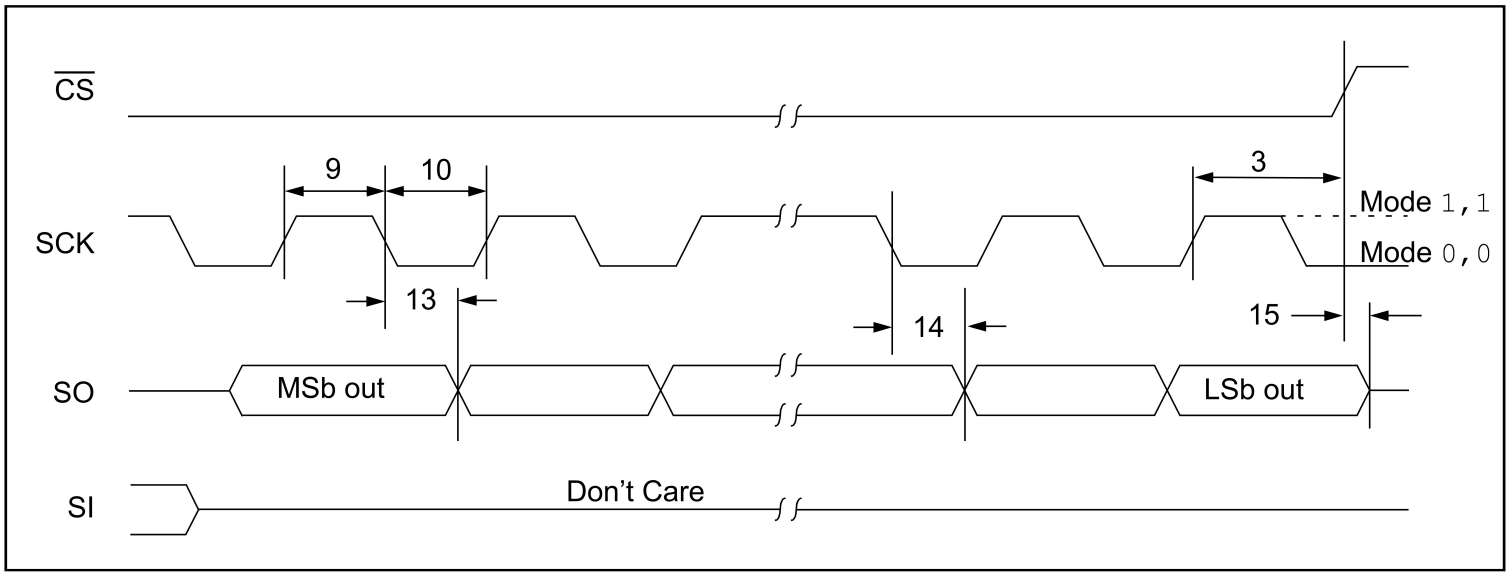


FIGURE 3: SERIAL OUTPUT TIMING

Chip Select (CS)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the CS input signal. If CS is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on CS after a valid write sequence initiates an internal write cycle. After power-up, a low level on CS is required prior to any sequence being initiated.

Serial Output (SO)

The SO pin is used to transfer data out of the 25LC1024. During a read cycle, data are shifted out on this pin after the falling edge of the serial clock.

Write-Protect (WP)

This pin is used in conjunction with the WPEN bit in the STATUS register to prohibit writes to the nonvolatile bits in the STATUS register. When WP is low and WPEN is high, writing to the nonvolatile bits in the STATUS register is disabled. All other operations function normally. When WP is high, all functions, including writes to the nonvolatile bits in the STATUS register, operate normally. If the WPEN bit is set, WP low during a STATUS register write sequence will disable writing to the STATUS register. If an internal write cycle has already begun, WP going low will have no effect on the write. The WP pin function is blocked when the WPEN bit in the STATUS register is low. This allows the user to install the 25LC1024 in a system with WP pin grounded and still be able to write to the STATUS register. The WP pin functions will be enabled when the WPEN bit is set high.

Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data are latched on the rising edge of the serial clock.

Serial Clock (SCK)

The SCK is used to synchronize the communication between a host and the 25LC1024. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin are updated after the falling edge of the clock input.

Hold (HOLD)

The HOLD pin is used to suspend transmission to the 25LC1024 while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the HOLD pin may be pulled low to pause further serial communication without resetting the serial sequence. The HOLD pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-to-low transition. The 25LC1024 must remain selected during this sequence. The SI and SCK levels are “don’t cares” during the time the device is paused and any transitions on these pins will be ignored. To resume serial communication, HOLD must be brought high while the SCK pin is low, otherwise serial communication will not be resumed until the next SCK high-to-low transition. The SO line will tri-state immediately upon a high-to-low transition of the HOLD pin and will begin outputting again immediately upon a subsequent low-to-high transition of the HOLD pin, independent of the state of SCK.

FUNCTIONAL DESCRIPTION

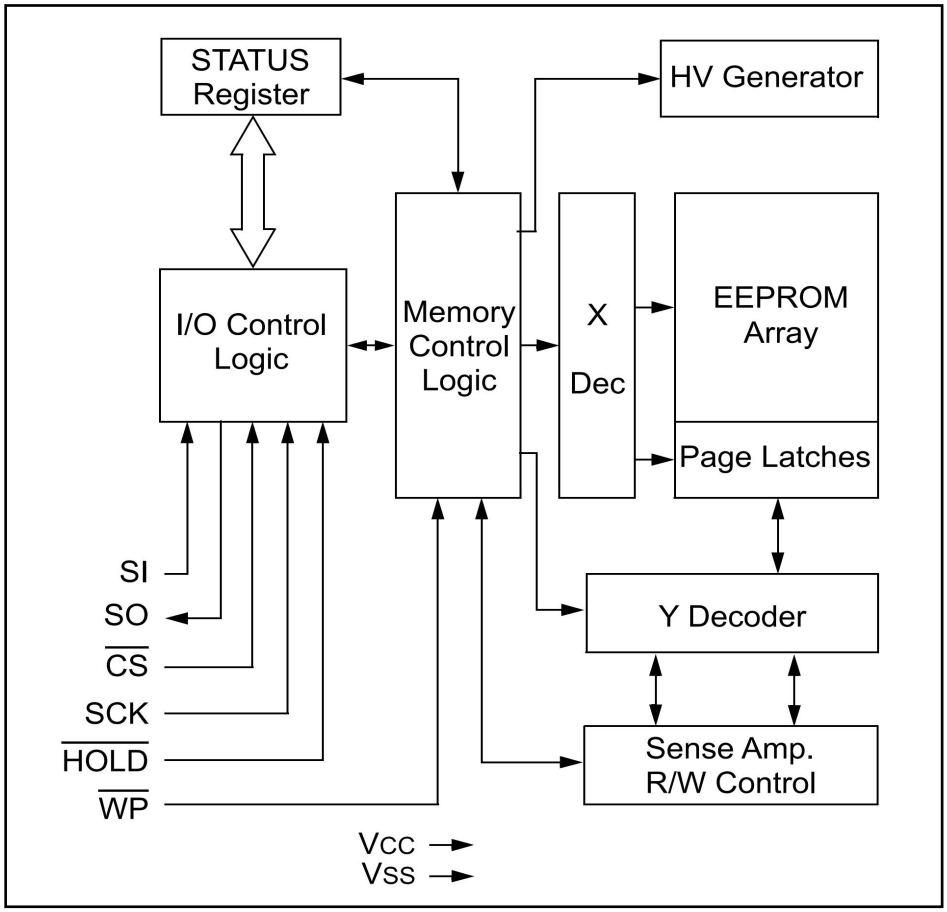
Principles of Operation

The 25LC1024 is a 131,072-byte Serial EEPROM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today’s popular microcontroller families. It may also interface with microcon-trollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in firmware to match the SPI protocol. The 25LC1024 contains an 8-bit instruction register. The device is accessed via the SI pin,with data being clocked in on the rising edge of SCK. The CS pin must be low and the HOLD pin must be high for the entire operation. Table 5 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses and data are transferred MSb first, LSb last. Data (SI) is sampled on the first rising edge of SCK after CS goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the HOLD input and place the 25LC1024 in ‘HOLD’ mode. After releasing the HOLD pin, operation will resume from the point when the HOLD was asserted.

TABLE 5: INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 0011	Read data from memory array beginning at selected address
WRITE	0000 0010	Write data to memory array beginning at selected address
WREN	0000 0110	Set the write enable latch (enable write operations)
WRDI	0000 0100	Reset the write enable latch (disable write operations)
RDSR	0000 0101	Read STATUS register
WRSR	0000 0001	Write STATUS register
PE	0100 0010	Page Erase-erase one page in memory array
SE	1101 1000	Sector Erase-erase one sector in memory array
CE	1100 0111	Chip Erase-erase all sectors in memory array
RDID	1010 1011	Release from Deep power-down and read electronic signature
DPD	1011 1001	Deep Power-Down mode

BLOCK DIAGRAM



Read Sequence

The device is selected by pulling CS low. The 8-bit READ instruction is transmitted to the 25LC1024 followed by the 24-bit address, with seven MSBs of the address being “don’t care” bits. After the correct READ instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal Address Pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (1FFFFh), the address counter rolls over to address, 00000h, allowing the read cycle to be contin-ued indefinitely. The read operation is terminated by raising the CS pin (Figure 4).

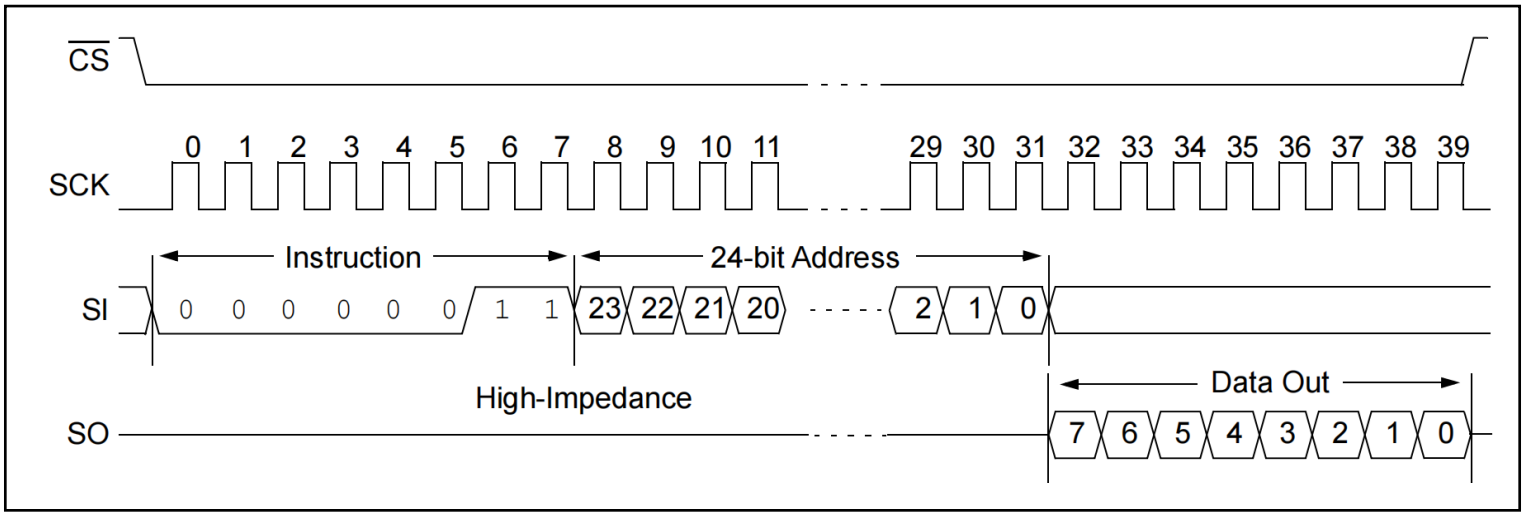


FIGURE 4: READ SEQUENCE

Write Sequence

Prior to any attempt to write data to the 25LC1024, the write enable latch must be set by issuing the WREN instruction (Figure 7). This is done by setting CS low and then clocking out the proper instruction into the 25LC1024. After all eight bits of the instruction are transmitted, the CS must be brought high to set the write enable latch. If the write operation is initiated immediately after the WREN instruction without CS being brought high, the data will not be written to the array because the write enable latch will not have been properly set. A write sequence includes an automatic, self-timed erase cycle. It is not required to erase any portion of the memory prior to issuing a write command. Once the write enable latch is set, the user may proceed by setting the CS low, issuing a WRITE instruc-tion, followed by the 24-bit address, with seven MSBs of the address being “don’t care” bits, and then the data to be written. Up to 256 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page.

Note: When doing a write of less than 256 bytes, the data in the rest of the page are refreshed along with the data bytes being written. This will force the entire page to endure a write cycle and for this reason endurance is specified per page.
Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or ‘ page size ’) and end at addresses that are integer multiples of page size – 1. If a Page Write command attempts to write across a physical page boundary, the result is that the data wrap around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

For the data to be actually written to the array, the CS must be brought high after the Least Significant bit (D0) of the nth data byte has been clocked in. If CS is brought high at any other time, the write operation will not be completed. Refer to Figure 5 and Figure 6 for more detailed illustrations on the byte write sequence and the page write sequence, respectively. While the write is in progress, the STATUS register may be read to check the status of the WPEN,WIP, WEL, BP1 and BP0 bits (Figure 9). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset

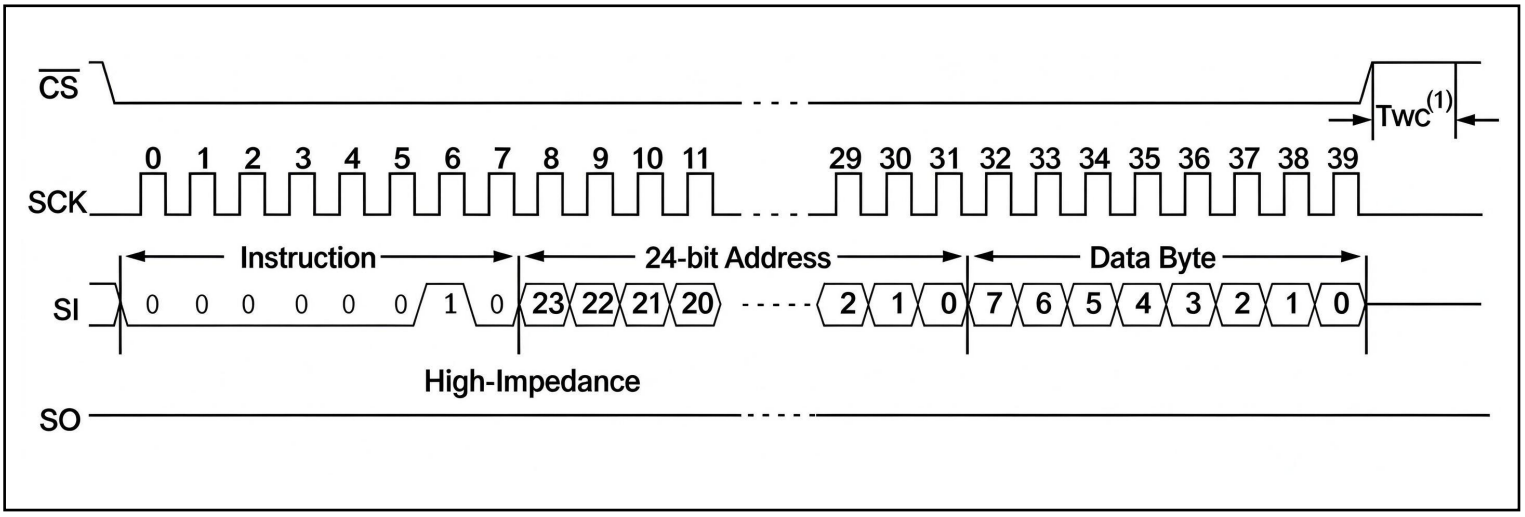


FIGURE 5: BYTE WRITE SEQUENCE

Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of CS after a valid sequence.

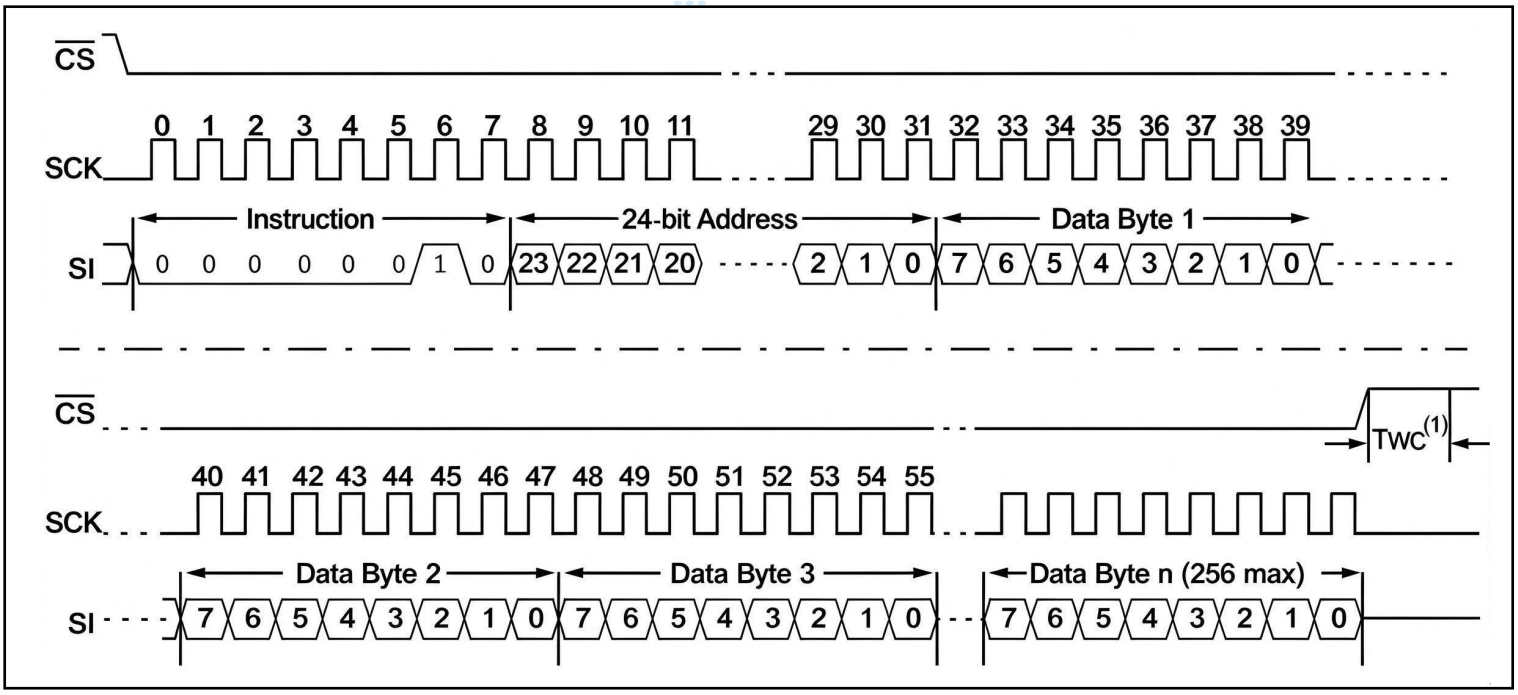


FIGURE 6: PAGE WRITE SEQUENCE

Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of CS after a valid sequence.

Write Enable (WREN) and Write Disable (WRDI)

The 25LC1024 contains a write enable latch. See Table 7 for the Write-Protect Functionality Matrix . This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch. The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed
- PE instruction successfully executed
- SE instruction successfully executed
- CE instruction successfully executed

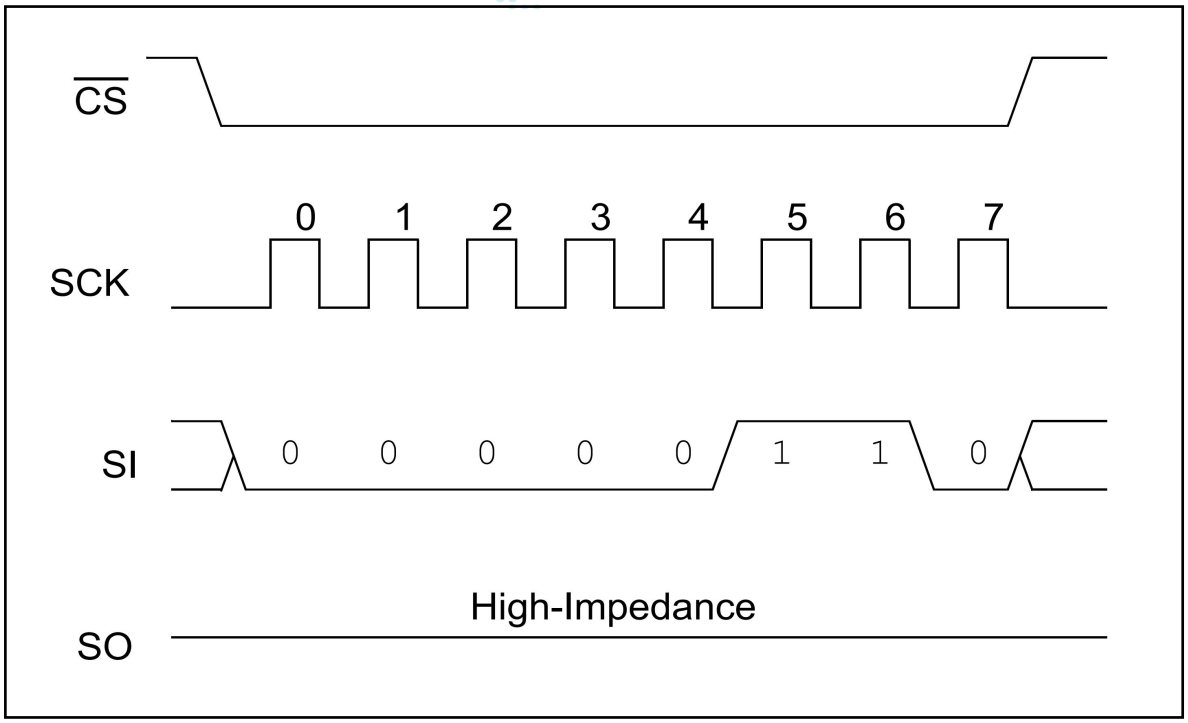


FIGURE 7: WRITE ENABLE SEQUENCE (WREN)

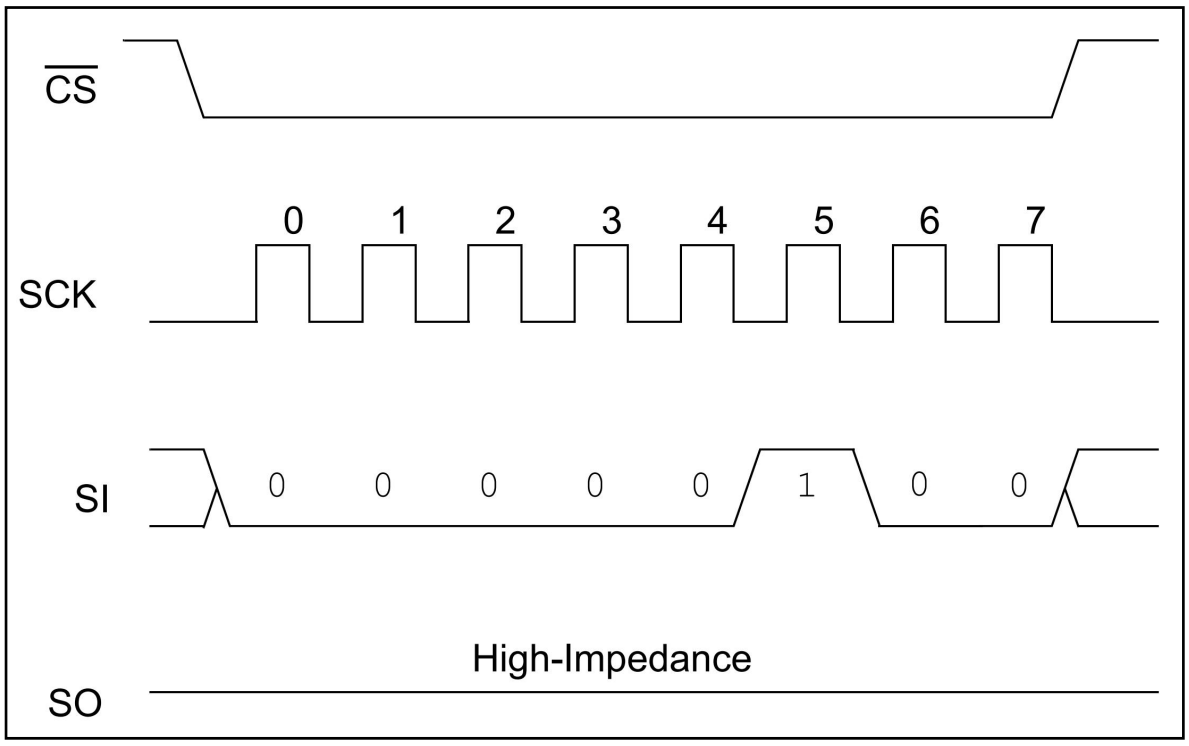


FIGURE 8: WRITE DISABLE SEQUENCE (WRDI)

Read STATUS Register Instruction (RDSR)

The Read STATUS Register instruction (RDSR) pro-vides access to the STATUS register. The STATUS reg-ister may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

TABLE 6: STATUS REGISTER

7	6	5	4	3	2	1	0
W/R	—	—	—	W/R	W/R	R	R
WPEN	X	X	X	BP1	BP0	WEL	WIP

Note 1: W/R = writable/readable. R = read-only.

The Write-In-Process (WIP) bit indicates whether the 25LC1024 is busy with a write operation. When set to a ‘ 1 ’ , a write is in progress, when set to a ‘ 0 ’ , no write is in progress. This bit is read-only. The Write Enable Latch (WEL) bit indicates the status of the write enable latch and is read-only. When set to a ‘ 1 ’ , the latch allows writes to the array, when set to a ‘ 0 ’ , the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the STATUS register. These commands are shown in Figure 7 and Figure 8. The Block Protection (BP0 and BP1) bits indicate which blocks are currently write-protected. These bits are set by the user issuing the WRSR instruction.
These bits are nonvolatile and are shown in Table 6. See Figure 9 for the RDSR timing sequence.

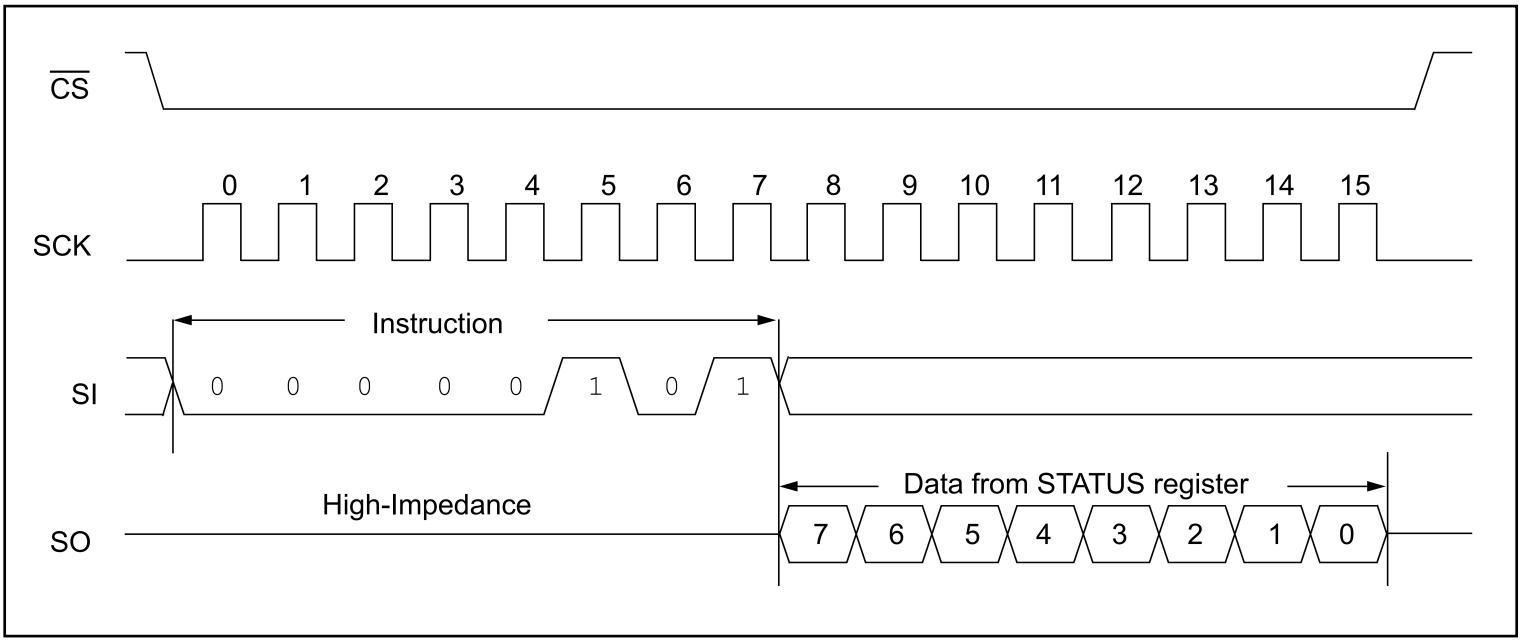


FIGURE 9: READ STATUS REGISTER TIMING SEQUENCE (RDSR)

Write STATUS Register Instruction (WRSR)

The Write STATUS Register instruction (WRSR) allows the user to write to the nonvolatile bits in the STATUS register as shown in Table 6. The user is able to select one of four levels of protection for the array by writing to the appropriate bits in the STATUS register. The array is divided up into four segments. The user has the ability to write-protect none, one, two or all four of the segments of the array. The partitioning is controlled as shown in Table 7. The Write-Protect Enable (WPEN) bit is a nonvolatile bit that is available as an enable bit for the WP pin. The Write-Protect (WP) pin and the Write-Protect Enable (WPEN) bit in the STATUS register control the programmable hardware write-protect feature. Hardware write protection is enabled when WP pin is low and the WPEN bit is high. Hardware write protection is disabled when either the WP pin is high or the WPEN bit is low. When the chip is hardware write-protected, only writes to nonvolatile bits in the STATUS register are disabled. See Table 8 for a matrix of functionality on the WPEN bit. See Figure 3-7 for the WRSR timing sequence.

TABLE 7: ARRAY PROTECTION

BP1	BP0	Array Addresses Write-Protected	Array Addresses Unprotected
0	0	none	All(Sectors 0,1,2&3)(00000h-1FFFFh)
0	1	Upper 1/4(Sector 3) (18000h-1FFFFh)	Lower 3/4(Sectors 0,1&2) (00000h-17FFFh)
1	0	Upper 1/2(Sectors 2&3) (10000h-1FFFFh)	Lower 1/2(Sectors 0&1) (00000h-0FFFFh)
1	1	All (Sectors 0,1,2&3) (00000h-1FFFFh)	none

TABLE 8: WRITE-PROTECT FUNCTIONALITY MATRIX

WEL (SR bit 1)	WPEN (SR bit 7)	WP (pin 3)	Protected Blocks	Unprotected Blocks	STATUS Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Writable	Writable
1	1	0(low)	Protected	Writable	Protected
1	1	1(high)	Protected	Writable	Writable

Note 1: x = don ' t care

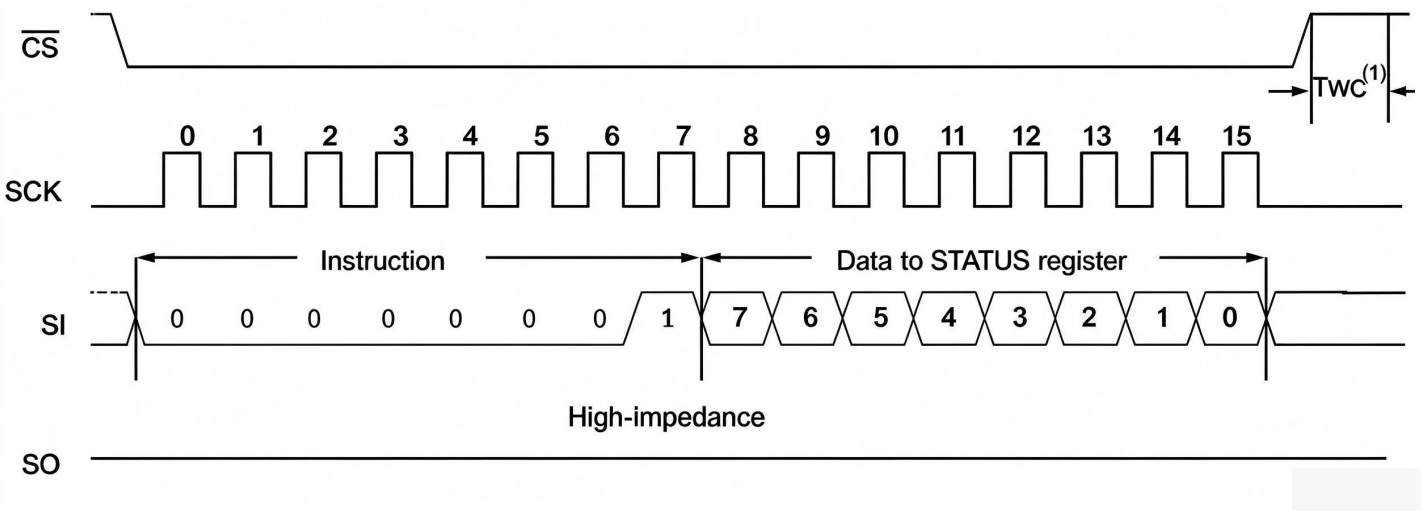


FIGURE 10: WRITE STATUS REGISTER TIMING SEQUENCE (WRSR)

Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of CS after a valid sequence.

PAGE ERASE

The Page Erase instruction will erase all bits (FFh) inside the given page. A Write Enable (WREN) instruc-tion must be given prior to attempting a Page Erase. This is done by setting CS low and then clocking out the proper instruction into the 25LC1024. After all eight bits of the instruction are transmitted, the CS must be brought high to set the write enable latch. The Page Erase instruction is entered by driving CS low, followed by the instruction code (Figure 11) and three address bytes. Any address inside the page to be erased is a valid address.
CS must then be driven high after the last bit if the address or the Page Erase will not execute. Once the CS is driven high, the self-timed Page Erase cycle is started. The WIP bit in the STATUS register can be read to determine when the Page Erase cycle is complete. If a Page Erase instruction is given to an address that has been protected by the Block Protect bits (BP0, BP1), then the sequence will be aborted and no erase will occur.

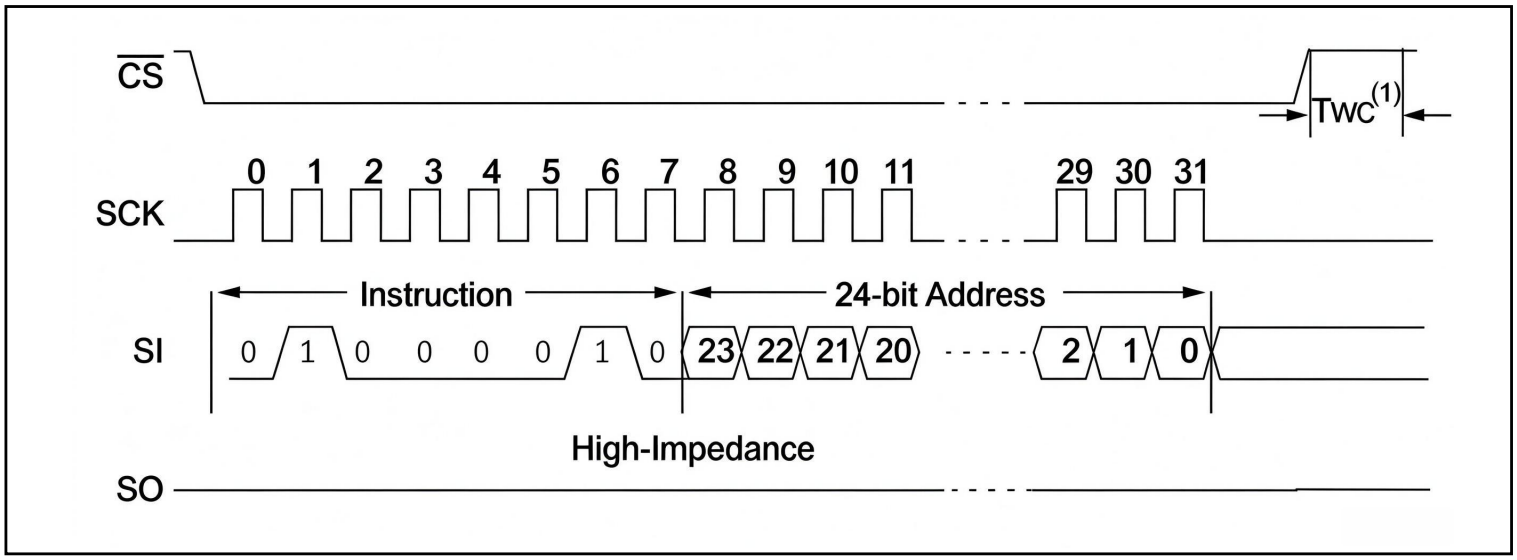


FIGURE 11: PAGE ERASE SEQUENCE

Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of CS after a valid sequence.

SECTOR ERASE

The Sector Erase instruction will erase all bits (FFh) inside the given sector. A Write Enable (WREN) instruc-tion must be given prior to attempting a Sector Erase. This is done by setting CS low and then clocking out the proper instruction into the 25LC1024. After all eight bits of the instruction are transmitted, the CS must be brought high to set the write enable latch. The Sector Erase instruction is entered by driving CS low, followed by the instruction code (Figure 12) and three address bytes. Any address inside the sector to be erased is a valid address. CS must then be driven high after the last bit if the address or the Sector Erase will not execute. Once the CS is driven high, the self-timed Sector Erase cycle is started. The WIP bit in the STATUS register can be read to determine when the Sector Erase cycle is complete. If a sector erase instruction is given to an address that has been protected by the Block Protect bits (BP0, BP1), then the sequence will be aborted and no erase will occur. See Table 7 for Sector Addressing.

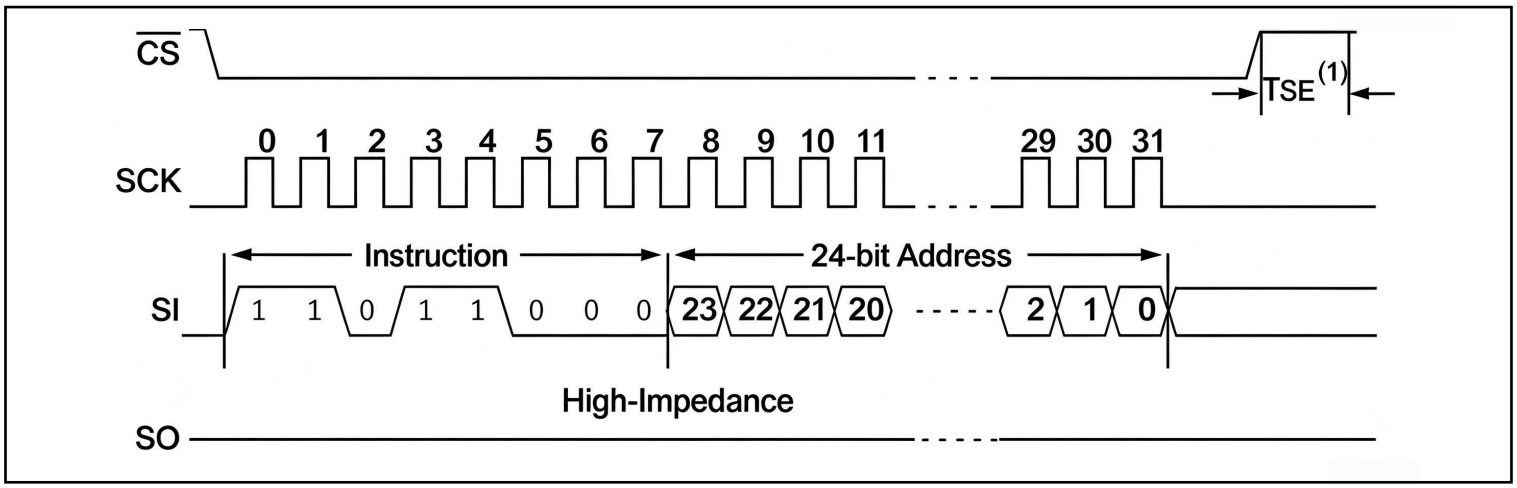


FIGURE 12: SECTOR ERASE SEQUENCE

Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of CS after a valid sequence.

CHIP ERASE

The Chip Erase instruction will erase all bits (FFh) in the array. A Write Enable (WREN) instruction must be given prior to executing a Chip Erase. This is done by setting CS low and then clocking out the proper instruction into the 25LC1024. After all eight bits of the instruction are transmitted , the CS must be brought high to set the write enable latch. The Chip Erase instruction is entered by driving the CS low, followed by the instruction code (Figure 13) onto the SI line. The CS pin must be driven high after the eighth bit of the instruction code has been given or the Chip Erase instruction will not be executed. Once the CS pin is driven high, the self-timed Chip Erase instruction begins. While the device is executing the Chip Erase instruction, the WIP bit in the STATUS register can be read to determine when the Chip Erase instruction is complete. The Chip Erase instruction is ignored if either of the Block Protect bits (BP0, BP1) are not 0, meaning 1/4, 1/2 or all of the array is protected.

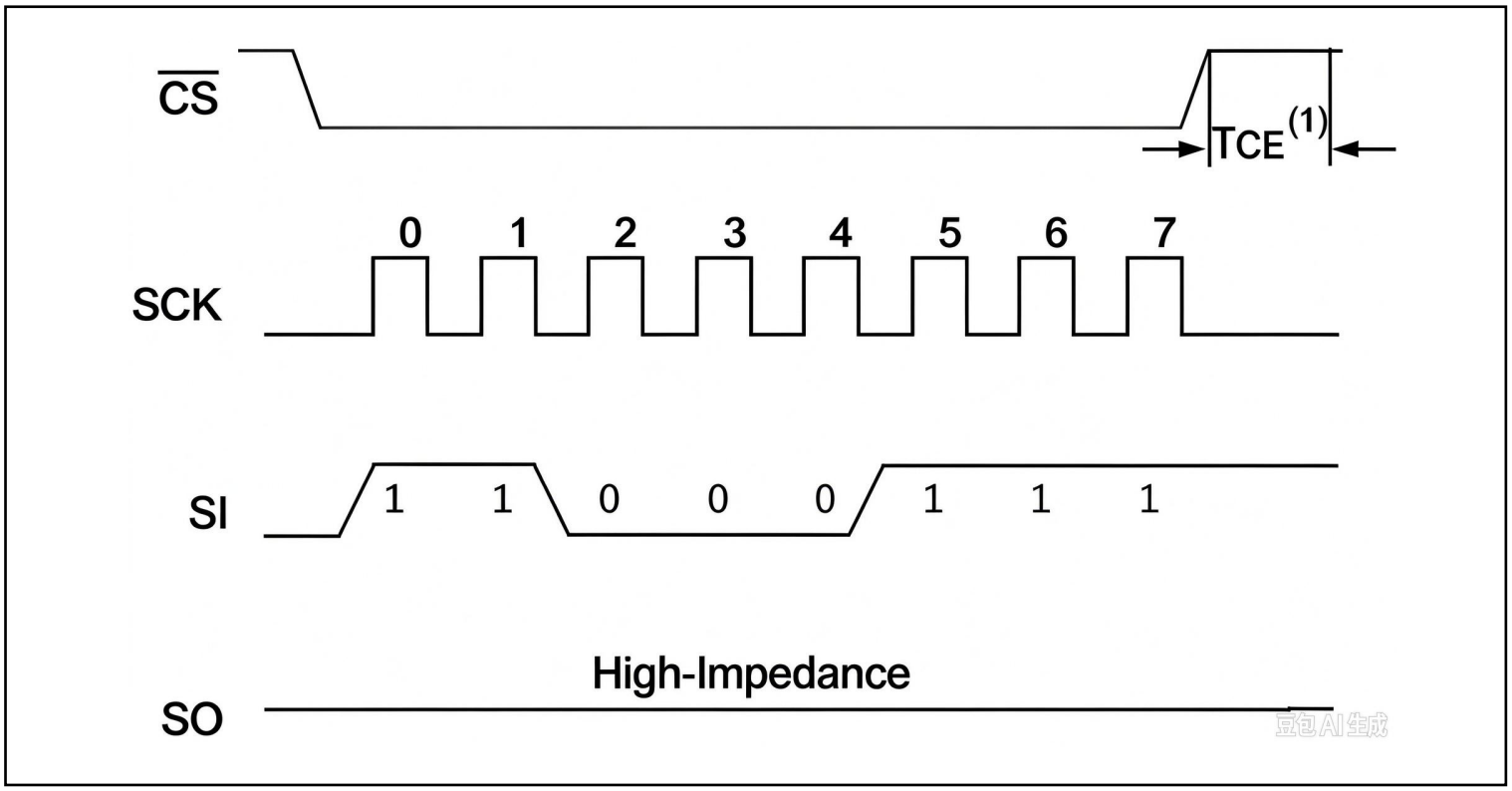


FIGURE 13: CHIP ERASE SEQUENCE

DEEP POWER-DOWN MODE

Deep Power-Down mode of the 25LC1024 is its lowest power consumption state. The device will not respond to any of the Read or Write commands while in Deep Power-Down mode and therefore it can be used as an additional software write protection feature. The Deep Power-Down mode is entered by driving CS low, followed by the instruction code (Figure 14) onto the SI line, followed by driving CS high. If the CS pin is not driven high after the eighth bit of the instruction code has been given, the device will not execute Deep power-down. Once the CS line is driven high, there is a delay (TDP) before the current settles to its lowest consumption. All instructions given during Deep Power-Down mode are ignored except the Read Electronic Signature Command (RDID). The RDID command will release the device from Deep power-down and output the electronic signature on the SO pin; then it returns the device to Standby mode after delay (TREL). Deep Power-Down mode automatically releases at device power-down. Once power is restored to the device, it will power-up in the Standby mode.

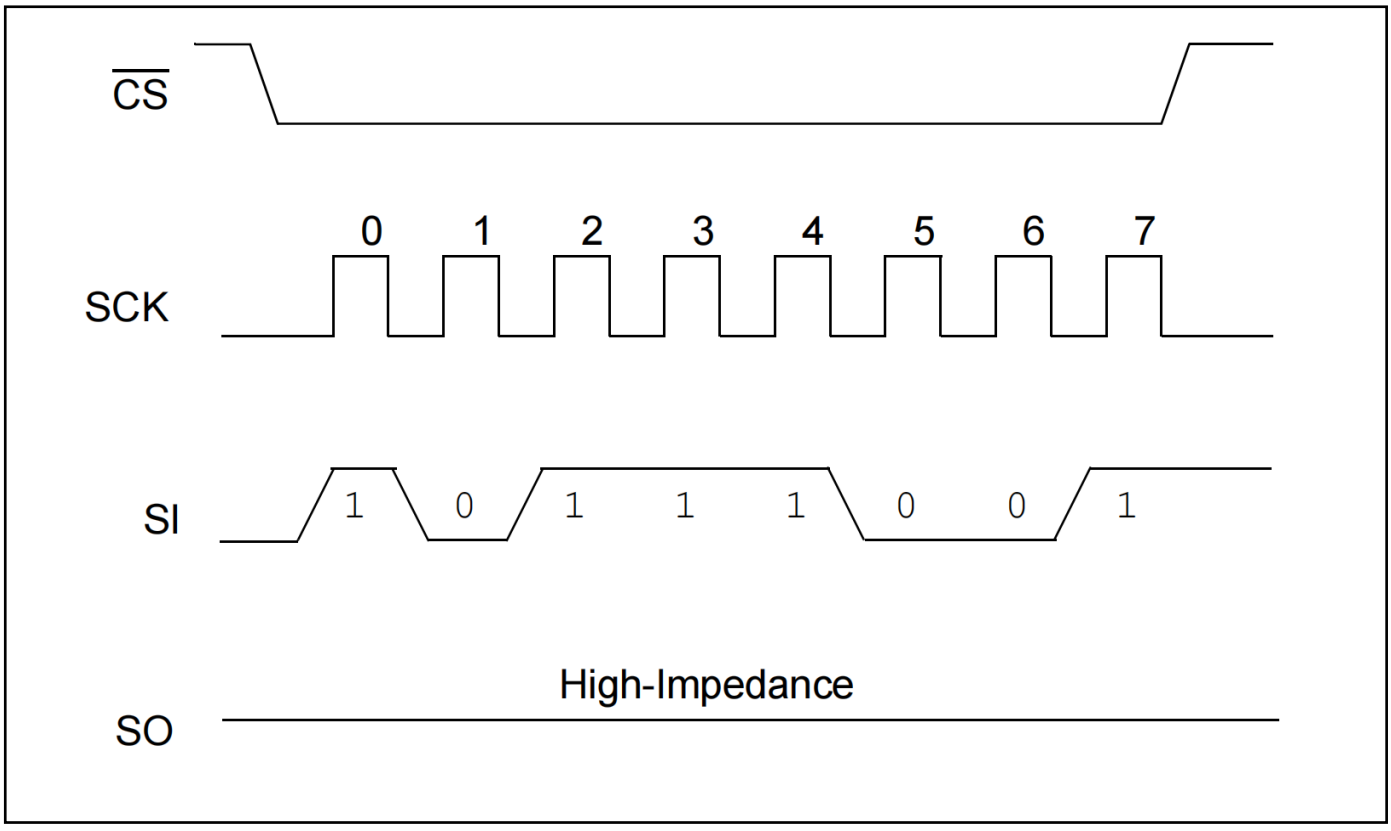


FIGURE 14: DEEP POWER-DOWN SEQUENCE

RELEASE FROM DEEP POWER-DOWN AND READ ELECTRONIC SIGNATURE

Once the device has entered Deep Power-Down mode, all instructions are ignored except the release from Deep Power-down and Read Electronic Signa-ture command. This command can also be used when the device is not in Deep Power-down to read the elec-tronic signature out on the SO pin unless another com-mand is being executed such as Erase, Program or Write STATUS register. Release from Deep Power-Down mode and Read Electronic Signature is entered by driving CS low, followed by the RDID instruction code (Figure 15) and then a dummy address of 24 bits (A23-A0). After the last bit of the dummy address is clocked in, the 8-bit electronic signature is clocked out on the SO pin. After the signature has been read out at least once, the sequence can be terminated by driving CS high. The device will then return to Standby mode and will wait to be selected so it can be given new instructions. If additional clockcycles are sent after the electronic signature has been read once, it will continue to output the signature on the SO line until the sequence is terminated.

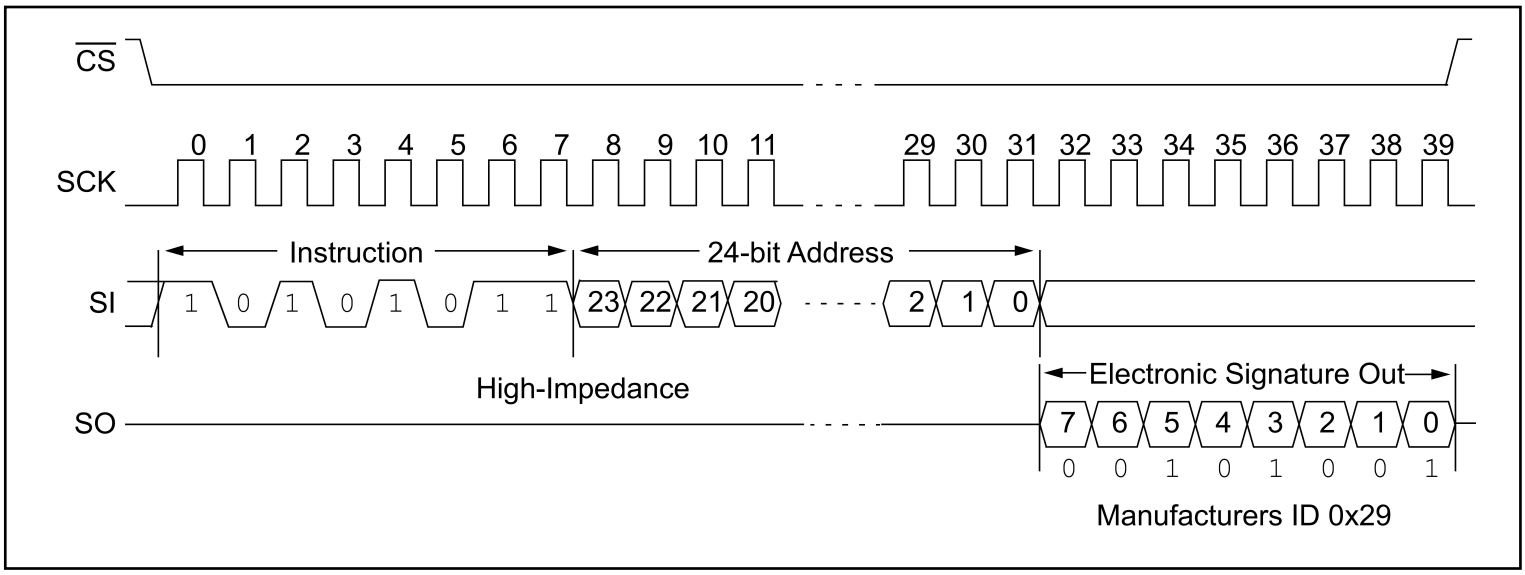


FIGURE 15: RELEASE FROM DEEP POWER-DOWN AND READ ELECTRONIC SIGNATURE

Driving CS high after the 8-bit RDID command, but before the Electronic Signature has been transmitted, will still ensure the device will be taken out of Deep Power-Down mode. However, there is a delay TREL that occurs before the device returns to Standby mode (ICCS), as shown in Figure 16.

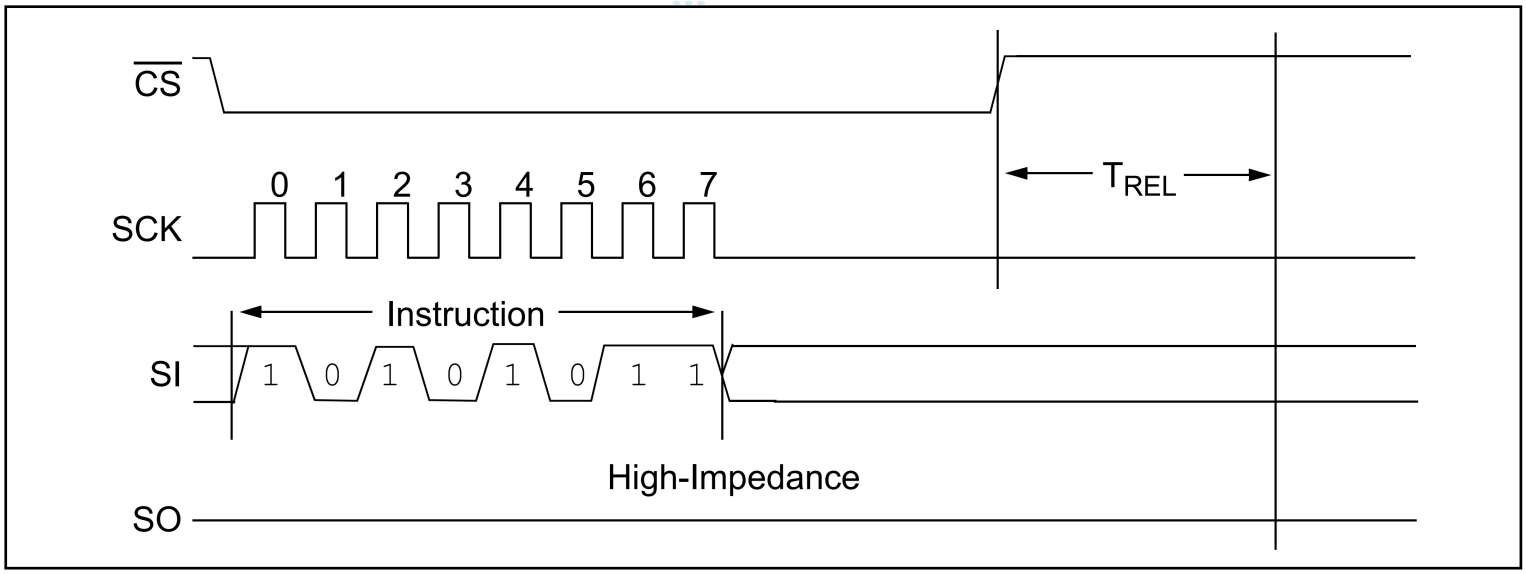


FIGURE 16: RELEASE FROM DEEP POWER-DOWN AND READ ELECTRONIC SIGNATURE

DATA PROTECTION

The following protection has been implemented to prevent inadvertent writes to the array:
- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or STATUS register write, the write enable latch is reset
- CS must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

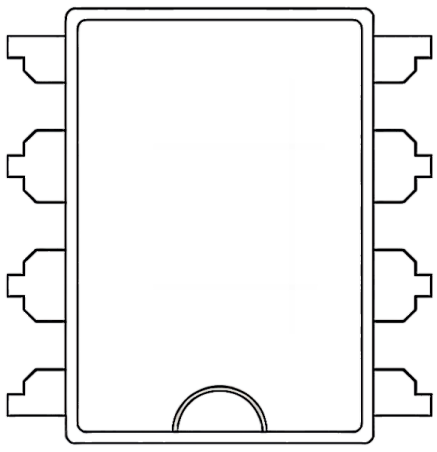
POWER-ON STATE

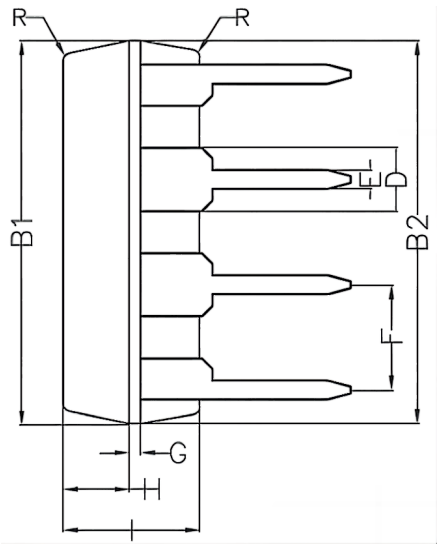
The 25LC1024 powers on in the following state:
- The device is in low-power Standby mode (CS= 1)
- The write enable latch is reset
- SO is in high-impedance state A high-to-low level transition on CS is required to enter active state

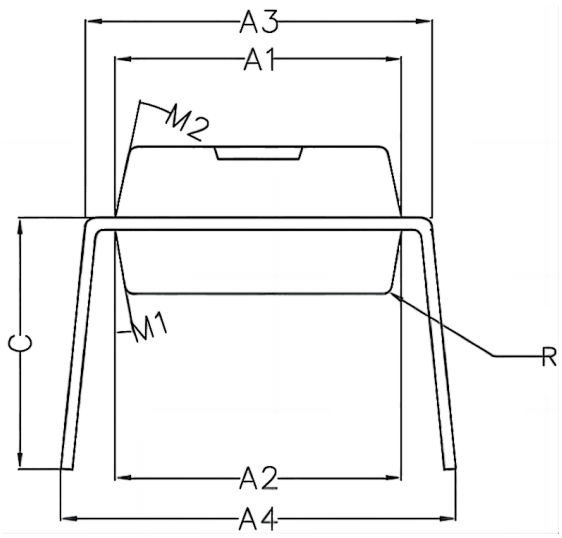
Order information

Order Number	Package	Package Quantity	Marking On The park	Temperature
25LC1024-E/P-TUDI	DIP8	Tube,50,A box of 2000	25LC1024-E/P	-40°C to+125°C

Package DIP8







Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

Important statement:

●TUDI Semiconductor reserves the right to modify the product manual without prior notice! Before placing an order, customers need to confirm whether the obtained information is the latest version and verify the completeness of the relevant information.

●Any semi-guide product is subject to failure or malfunction under specified conditions. It is the buyer's responsibility to comply with safety standards when using TUDI Semiconductor products for system design and whole machine manufacturing.And take the appropriate safety measures to avoid the potential in the risk of loss of personal injury or loss of property situation!

●TUDI Semiconductor products have not been licensed for life support, military, and aerospace applications,and therefore TUDI Semiconductor is not responsible for any consequences arising from the use of this product in these areas.

●If any or all TUDI Semiconductor products (including technical data, services) described or contained in this document are subject to any applicable local export control laws and regulations, they may not be exported without an export license from the relevant authorities in accordance with such laws.

●The specifications of any and all TUDI Semiconductor products described or contained in this document specify the performance, characteristics, and functionality of said products in their standalone state, but do not guarantee the performance, characteristics, and functionality of said products installed in Customer's products or equipment. In order to verify symptoms and conditions that cannot be evaluated in a standalone device, the Customer should ultimately evaluate and test the device installed in the Customer's product device.

●TUDI Semiconductor documentation is only allowed to be copied without any alteration of the content and with the relevant authorization.TUDI Semiconductor assumes no responsibility or liability for altered documents.

●TUDI Semiconductor is committed to becoming the preferred semiconductor brand for customers, and TUDI Semiconductor will strive to provide customers with better performance and better quallity products.