P-channel Enhancement Mode Power MOSFET

Features

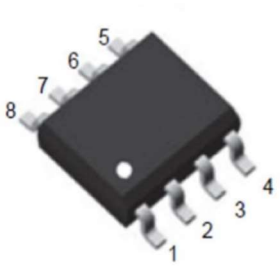
- V_{DS}= -20V, I_D= -13A
  $R_{DS(ON)}$ < 17 mΩ @ V_{GS} = -4.5V
  $R_{DS(ON)}$ < 20 mΩ @ V_{GS} = -2.5V

General Features

- Advanced Trench Technology
- Provide Excellent RDS(ON) and Low Gate Charge
- Lead Free and Green Available

100% UIS TESTED!
100% ΔVds TESTED!

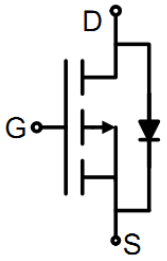
RoHS



SOP-8



pin assignment



Schematic diagram

■ **Absolute Maximum Ratings** (T_A=25℃unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	-20	V
Gate-source Voltage		V_{GS}	±10	V
Drain Current	T_A=25℃ @ Steady State	I_D	-13	A
	T_A=70℃ @ Steady State		-10.4	
Pulsed Drain Current [A]		I_{DM}	-55	A
Total Power Dissipation @ T_A=25℃		P_D	3.0	W
Thermal Resistance Junction-to-Ambient @ Steady State [B]		$R_{\theta JA}$	42	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V,V_{GS}=0V,T_C=25℃			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±10V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-0.4		-2.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -4.5V, I_D=-10A			17	mΩ
		V_{GS}= -2.5V, I_D=-6.5A			20	
		V_{GS}= -1.8V, I_D=-4.0A			26	
Diode Forward Voltage	V_{SD}	I_S=-13A,V_{GS}=0V			-1.2	V
Maximum Body-Diode Continuous Current	I_S				-13	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-10V,V_{GS}=0V,f=1MHZ		2992		pF
Output Capacitance	C_{oss}			330		
Reverse Transfer Capacitance	C_{rss}			272		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V,V_{DS}=-15V,I_D=-9.1A		72.8		nC
Gate Source Charge	Q_{gs}			6.6		
Gate Drain Charge	Q_{gd}			10.1		
Reverse Recovery Charge	Q_{rr}	I_F=-6A, di/dt=100A/us		34		
Reverse Recovery Time	t_{rr}			67		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V,V_{DS}=-15V, I_D=-6A, R_{GEN}=2.5Ω		7		
Turn-on Rise Time	t_r			33		
Turn-off Delay Time	$t_{D(off)}$			130		
Turn-off Fall Time	t_f			132		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{\theta JA}$ is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JL}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

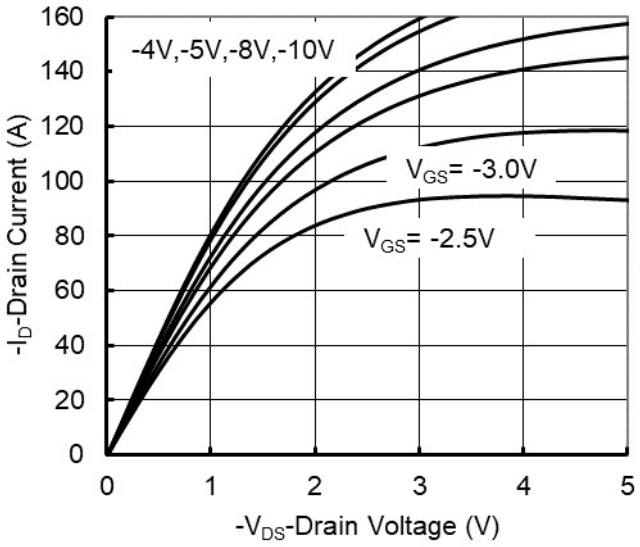


Figure 1. Output Characteristics

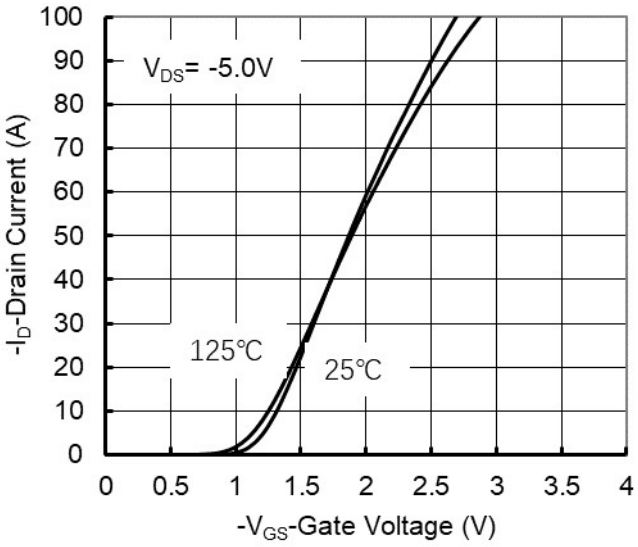


Figure 2. Transfer Characteristics

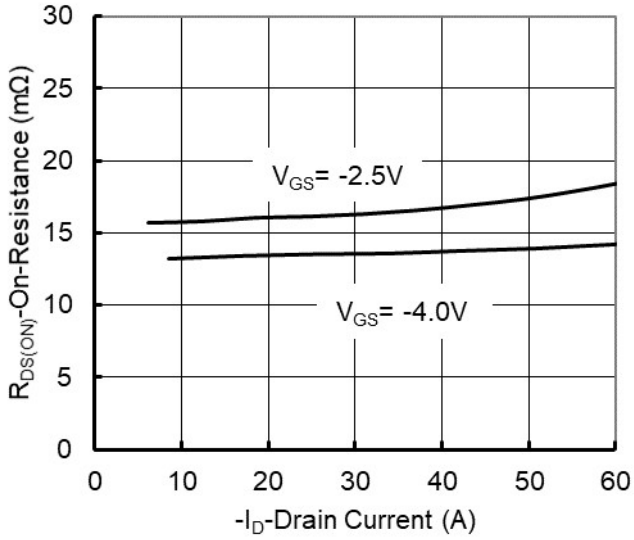


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

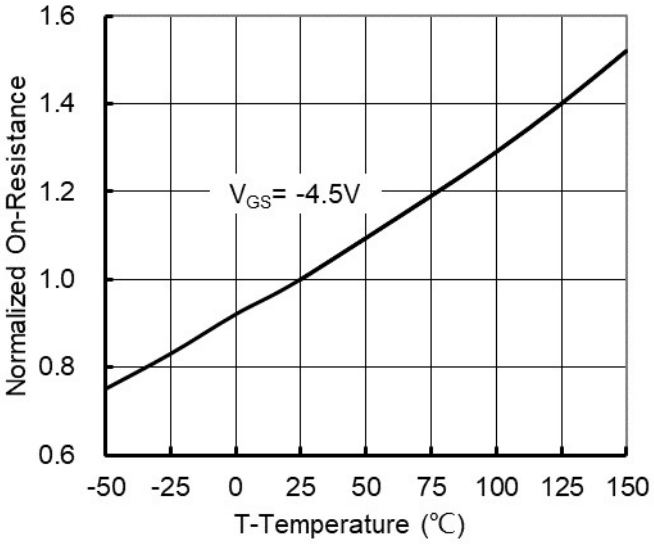


Figure 4. On-Resistance vs. Junction Temperature

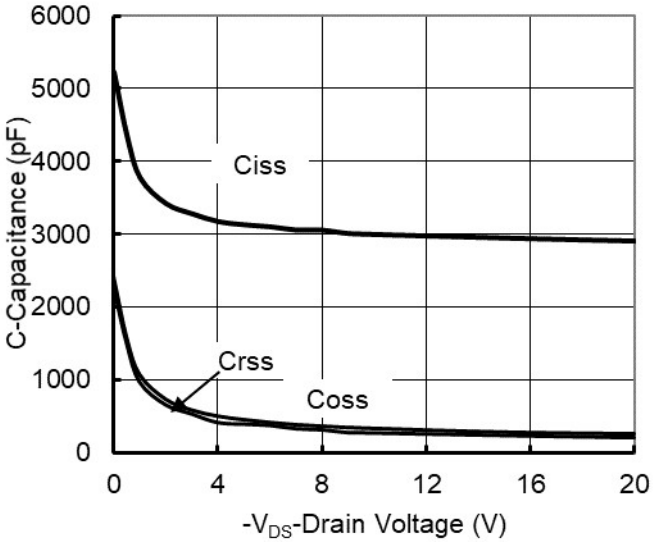


Figure 5. Capacitance Characteristics

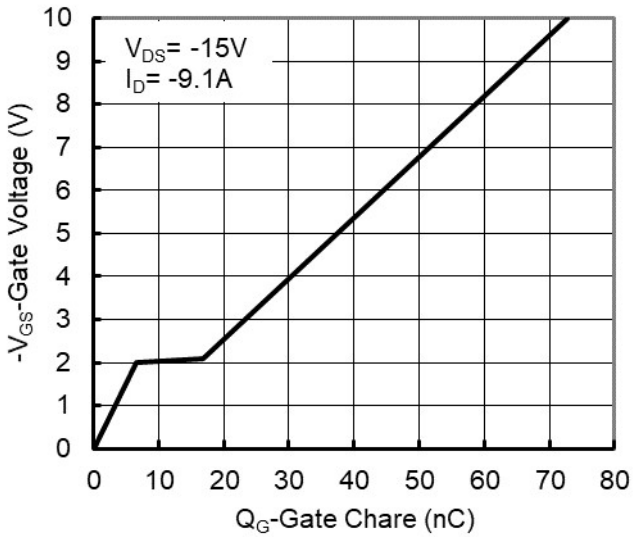


Figure 6. Gate Charge

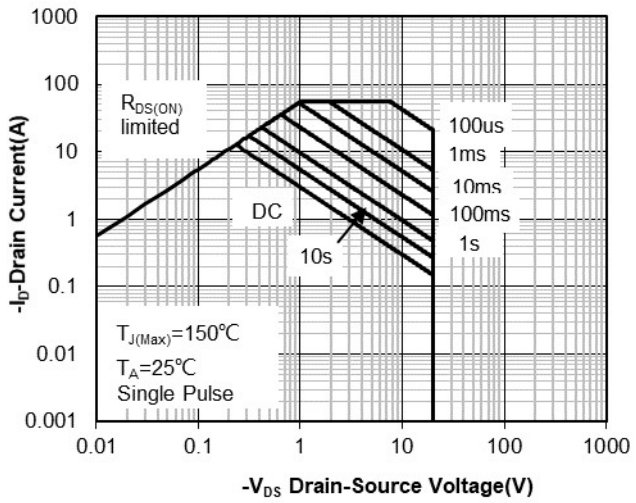


Figure 7. Safe Operation Area

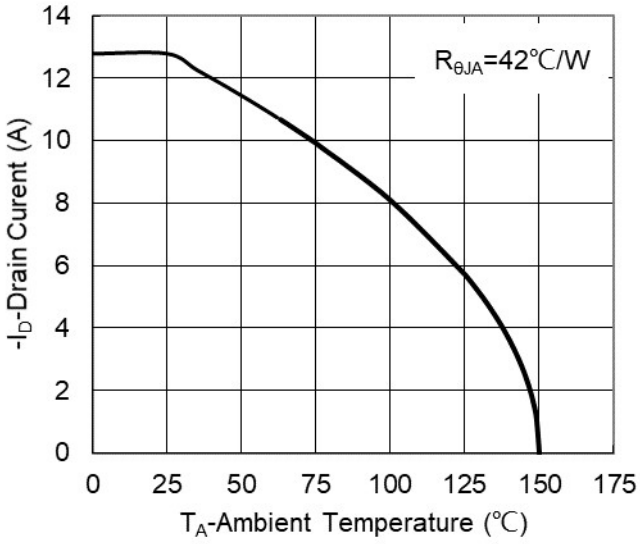


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

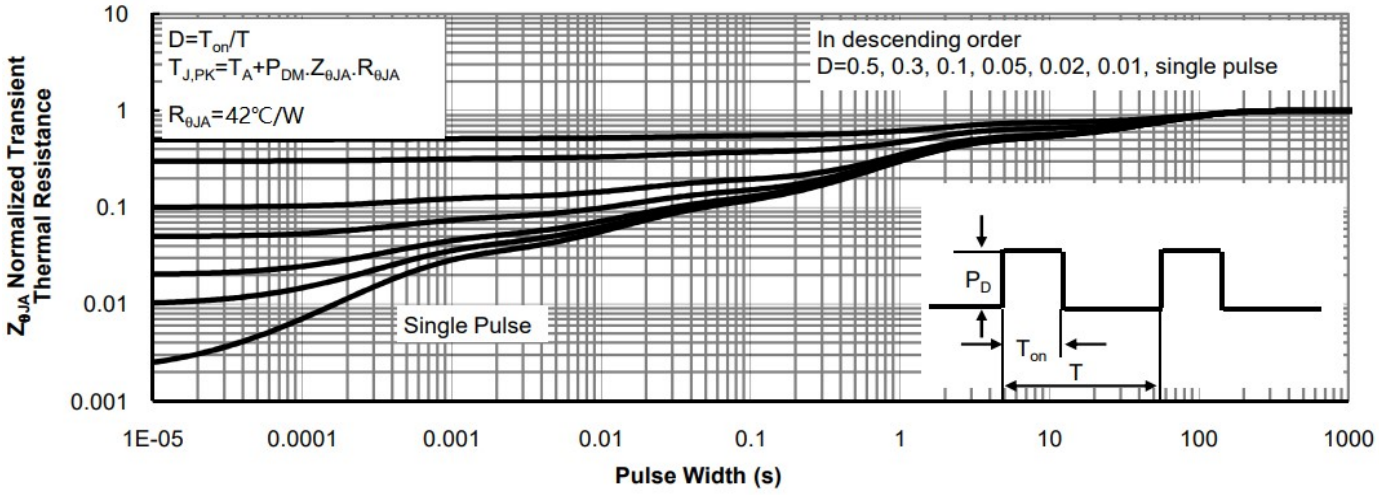
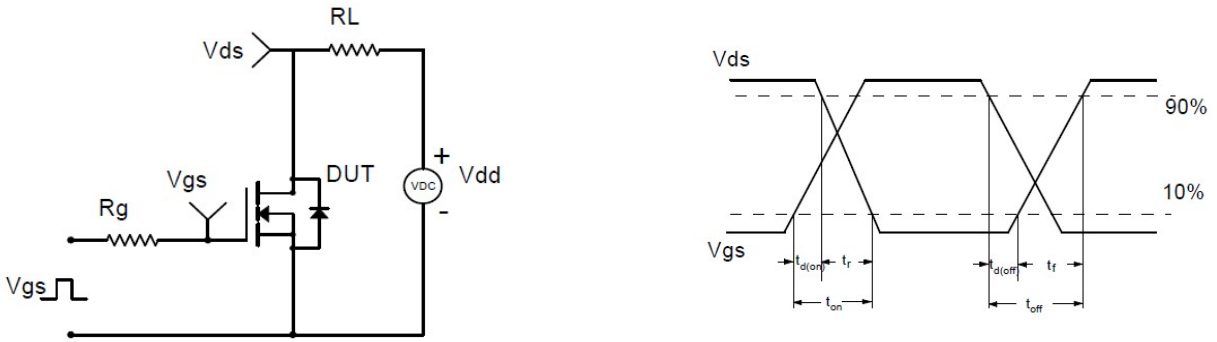
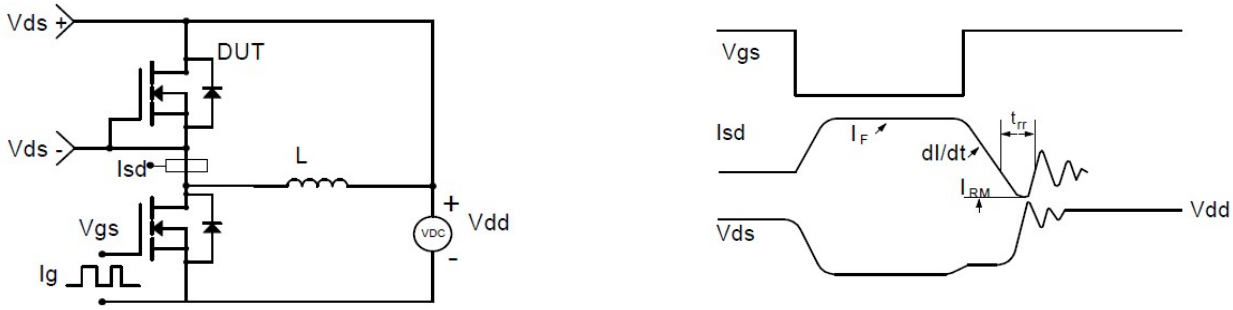


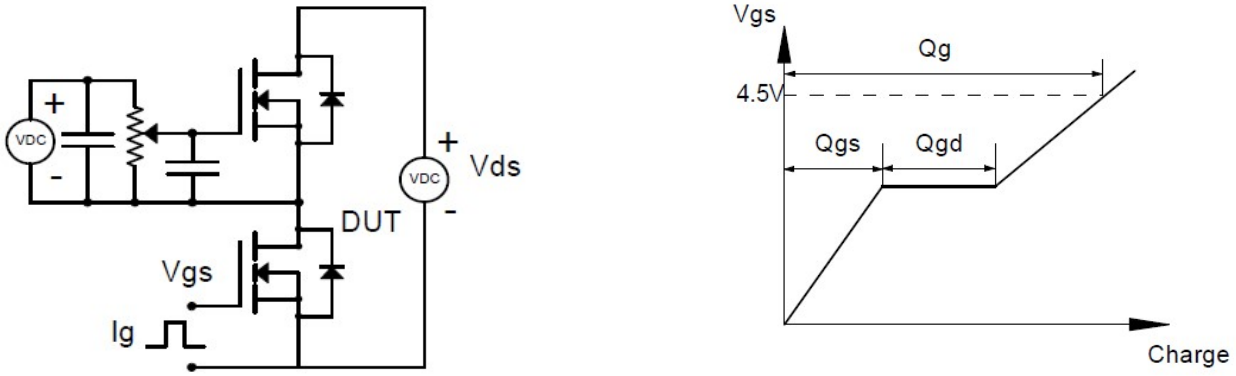
Figure 9. Normalized Maximum Transient Thermal Impedance



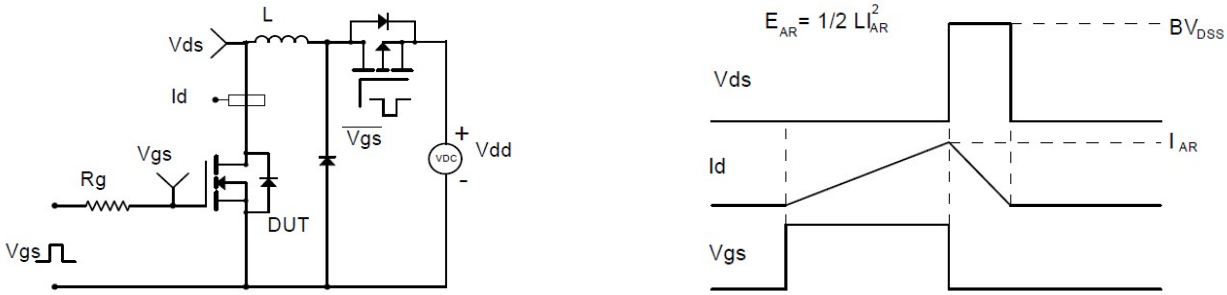
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms