ESD11L5.0DT5G

ESD Protection Diode
Ultra−Low Capacitance

The ESD11L5.0DT5G is designed to protect voltage sensitive components from damage due to ESD in applications that require ultra low capacitance to preserve signal integrity. Excellent clamping capability, low leakage and fast response time are combined with an ultra low diode capacitance of 0.5 pF to provide best in class protection from IC damage due to ESD. The ultra small SOT−1123 package is ideal for designs where board space is at a premium. The ESD11L5.0DT5G can be used to protect two uni−directional lines or one bi−directional line. When used to protect one bi−directional line, the effective capacitance is 0.25 pF. Because of its low capacitance, it is well suited for protecting high frequency signal lines such as USB2.0 high speed and antenna line applications.

Specification Features:

- Low Capacitance 0.5 pF Typical
- Low Clamping Voltage
- Small Body Outline Dimensions:
  0.039” x 0.024” (1.0 mm x 0.6 mm)
- Low Body Height: 0.015″ (0.37 mm)
- Stand−off Voltage: 5 V
- Low Leakage
- Response Time is Typically < 1.0 ns
- IEC61000−4−2 Level 4 ESD Protection
- AEC−Q101 Qualified and PPAP Capable
- This is a Pb−Free Device

Mechanical Characteristics:

CASE: Void-free, transfer-molded, thermosetting plastic Epoxy Meets UL 94 V−0
LEAD FINISH: 100% Matte Sn (Tin)
QUALIFIED MAX REFLOW TEMPERATURE: 260°C
Device Meets MSL 1 Requirements

Table 1. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IEC 61000−4−2 (ESD) Contact		±10	kV
Total Power Dissipation on FR−5 Board (Note 1) @ T_A = 25°C	P_D	150	mW
Storage Temperature Range	T_{stg}	−55 to +150	°C
Junction Temperature Range	T_J	−55 to +125	°C
Lead Solder Temperature − Maximum (10 Second Duration)	T_L	260	°C

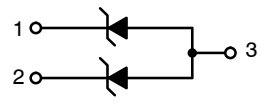
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. FR−5 = 1.0 x 0.75 x 0.62 in.

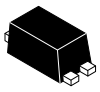
See Application Note AND8308/D for further description of survivability specs.

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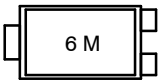
PIN 1. CATHODE
2. CATHODE
3. ANODE





SOT−1123
CASE 524AA

MARKING DIAGRAM



6 = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
ESD11L5.0DT5G	SOT−1123 (Pb−Free)	8000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DEVICE MARKING INFORMATION

See specific marking information in the device marking column of the Electrical Characteristics tables starting on page 2 of this data sheet.

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Table 2. ELECTRICAL CHARACTERISTICS
(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Capacitance @ V_R = 0 V and f = 1.0 MHz

*See Application Note AND8308/D for detailed explanations of datasheet parameters.

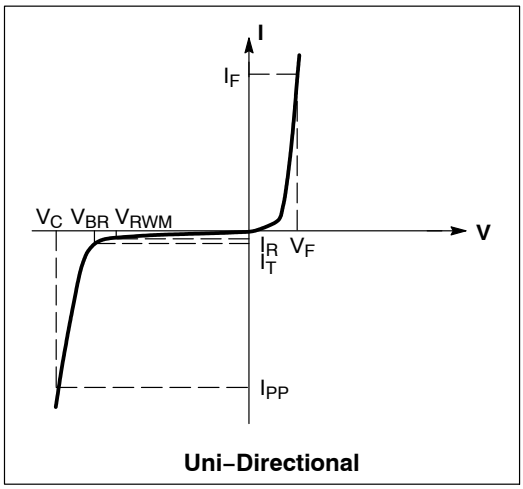


Table 3. ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, V_F = 1.1 V Max. @ I_F = 10 mA for all types)

Device	Device Marking	V_{RWM} (V)	I_R (μA) @ V_{RWM}	V_{BR} (V) @ I_T (Note 2)	I_T	C (pF), uni−directional (Note 3)		C (pF), bi−directional (Note 4)		V_C
		Max	Max	Min	mA	Typ	Max	Typ	Max	Per IEC61000−4−2 (Note 6)
ESD11L5.0DT5G	6	5.0	1.0	5.4	1.0	0.5	0.9	0.25	0.45	Figures 1 and 2

2. V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C.
3. Uni−directional capacitance at f = 1 MHz, V_R = 0 V, T_A = 25°C (pin1 to pin 3; pin 2 to pin 3).
4. Bi−directional capacitance at f = 1 MHz, V_R = 0 V, T_A = 25°C (pin1 to pin 2).
5. Surge current waveform per Figure 5.
6. Typical waveform. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

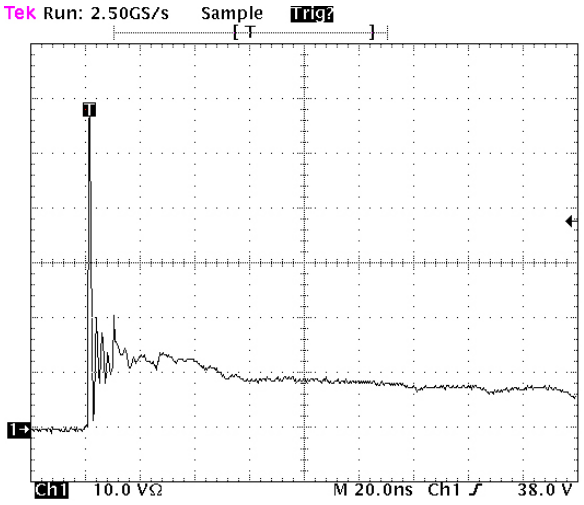


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV contact per IEC 61000−4−2

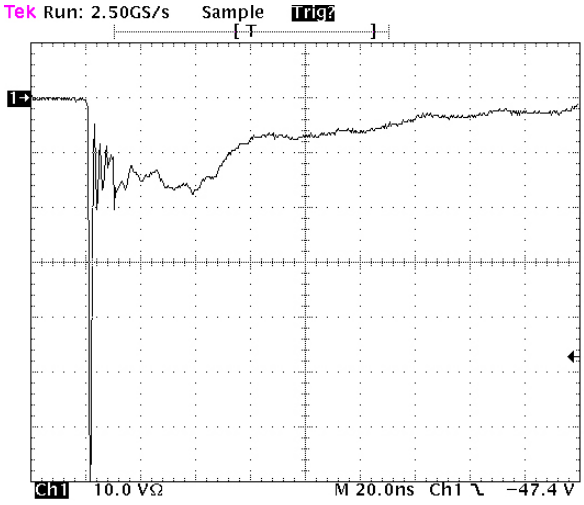


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV contact per IEC 61000−4−2

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

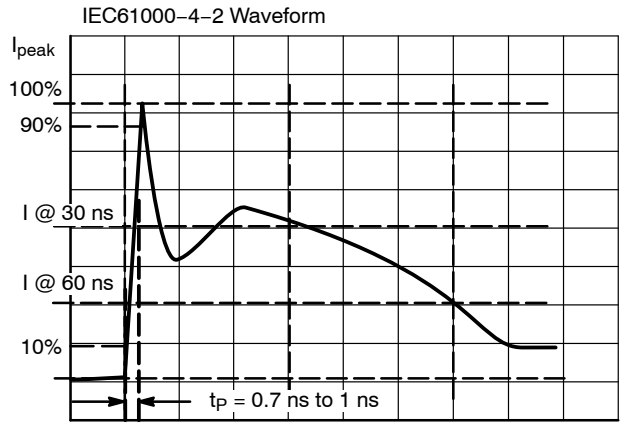


Figure 3. IEC61000−4−2 Spec

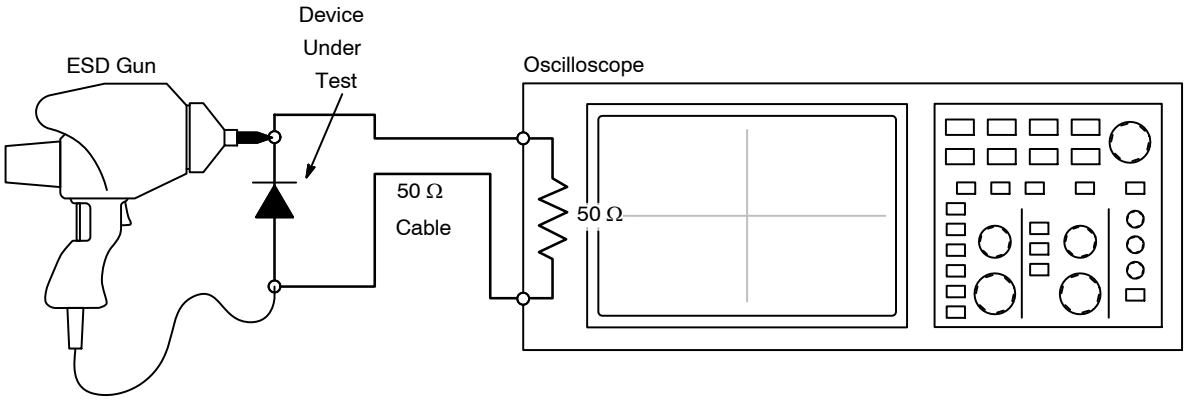


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

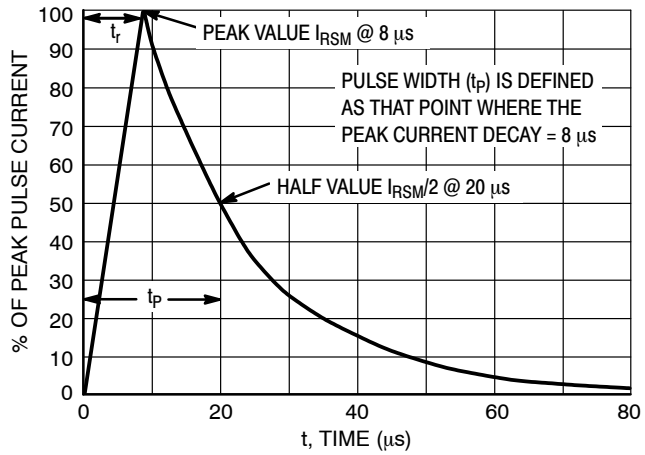
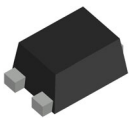


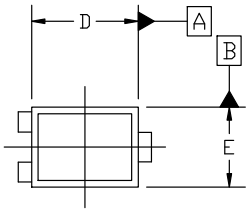
Figure 5. 8 X 20 μs Pulse Waveform

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

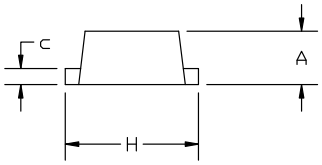


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CASE 524AA
ISSUE D

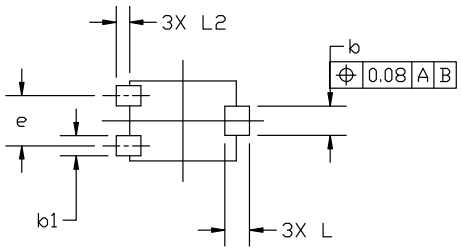
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TOP VIEW



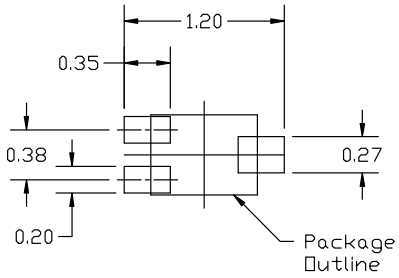
SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.15	0.22	0.28
b1	0.10	0.15	0.20
c	0.07	0.12	0.17
D	0.75	0.80	0.85
E	0.55	0.60	0.65
e	0.35	0.38	0.40
H	0.950	1.000	1.050
L	0.185 REF		
L2	0.05	0.10	0.15



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download th e ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN

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