

钍地半导体
Tudi Semiconductor

Product Specification

TUDI-SN75LBC175

Four-channel low-power differential line receiver

网址 www.sztdbdt.com

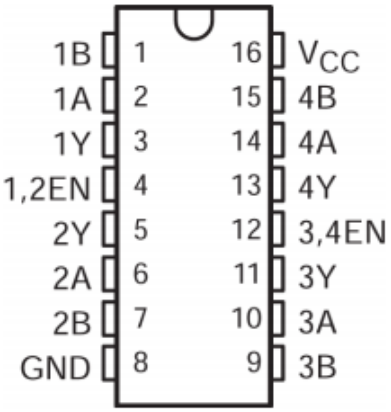
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- Complies with or exceeds EIA standards RS-422-A, RS-423-A, RS-485 CCITT recommendation V.11
- Can operate with pulse durations as low as 20ns
- Suitable for multi-point transmission on long buses in noisy environments Input sensitivity: ± 200mV
- Low power consumption: 20 mA (maximum)
- Open-circuit fail-safe design
- Common-mode input voltage of -7 V to 12V
- Pin compatible with SN75175 and LTC489



D, DW, or N Package
(Top View)

Applications

- Factory automation
- ATMs and bill counters
- Smart grids
- AC and servo motor drives

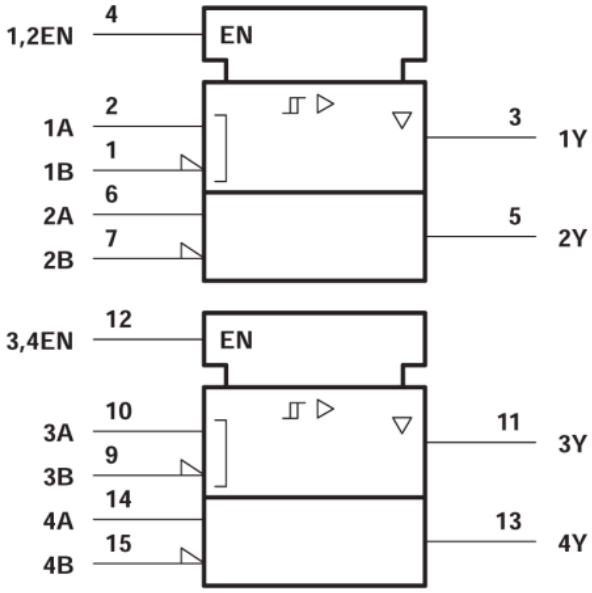
Description

The SN65LBC175 and SN75LBC175 are single-chip, four-channel differential receivers with three-state outputs, designed to meet the requirements of EIA standards RS-422-A, RS-423-A, RS-485, CCITT Recommendation V.11. This device is optimized for balanced multi-point bus transmission with data rates up to and exceeding 10 Mbps. The receivers are enabled in by active-high enable inputs. Each differential receiver input features high-impedance hysteresis to improve noise immunity, and a sensitivity of ±200mV within a common- input voltage range of – 12V to -7V. Fail-safe design ensures that the outputs always remain at a high level when the inputs are open-circuited. Both are designed using TI's proprietary LinBiCMOS™ technology, enabling low power consumption, high switching speeds, and robustness.

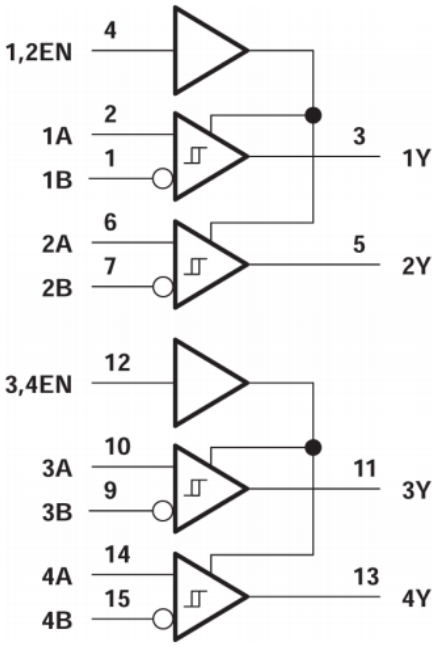
These devices provide excellent performance when used with the SN75LBC172 or SN75LBC174 quad-channel line drivers

The SN65LBC175 is available in 16-pin DIP (N), small outline (D), and wide outline (DW) packages. The SN5LBC175 is available in 16-pin DIP (N) and small outline (D) packages.

The SN65LBC175 rated for operation in the -40°C to 85°C industrial temperature range. The SN75LBC175 is rated for operation in the 0C to 70°C commercial temperature range.



逻辑符号†



逻辑图（正逻辑）

表 **4-1. Pin Functions**

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 Inverting Differential Input
1A	2	I	Channel 1 Non-Inverting Differential Input
1Y	3	O	Channel 1 Output
1,2 EN	4	I	Channel 1 and 2 Active High Enable
2Y	5	O	Channel 2 Output
2A	6	I	Channel 2 Non-Inverting Differential Input
2B	7	I	Channel 2 Inverting Differential Input
GND	8	GND	Device Ground
3B	9	I	Channel 3 Inverting Differential Input
3A	10	I	Channel 3 Non-Inverting Differential Input
3Y	11	O	Channel 3 Output
3,4 EN	12	I	Channel 3 and 4 Active High Enable
4Y	13	O	Channel 4 Output
4A	14	I	Channel 4 Non-Inverting Differential Input
4B	15	I	Channel 4 Inverting Differential Input
V_{CC}	16	POW	Device Supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC} (see (2))	Supply voltage range		−0.3	7	V
V_I	Input voltage	(A or B inputs)		±25	V
V_{ID} (see (3))	Differential input voltage			±25	V
	Voltage range at Y, 1/2EN, 3/4EN		−0.3	V_{CC} + 0.5	V
	Continuous total dissipation		See Dissipation Rating Table		
T_A	Operating free-air temperature range:	SN65LBC175	−40	85	°C
		SN75LBC175	0	70	°C
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	
		Machine Model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

over operating free-air temperature range (unless otherwise noted)

5.3 Dissipation Rating Table

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	1100 mW	8.7 mW/°C	709 mW	578 mW
DW	1200 mW	9.6 mW/°C	770 mW	625 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

5.4 Thermal Information

THERMAL METRIC(1)		SOIC (D)	SOIC (DW)	PDIP (N)	UNIT
		16 Pins	16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	71.1	60.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	37.4	48.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	36.8	40.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	13.3	27.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	36.4	40.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}		−7		12	V
Differential input voltage, V_{ID}				±6	V
High-level input voltage, V_{IH}	EN inputs	2			V
Low-level input voltage, V_{IL}	EN inputs			0.8	V
High-level output current, I_{OH}				−8	mA
Low-level output current, I_{OL}				8	mA
Operating free-air temperature, T_A	SN65LBC175	−40		85	°C
	SN75LBC175	0		70	

5.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		I_O = −8 mA			0.2			V
V_{IT-}	Negative-going input threshold voltage		I_O = 8 mA			−0.2			V
V_{hys}	Hysteresis voltage (V_{IT+} − V_{IT-})						45		mV
V_{IK}	Enable input clamp voltage		I_I = −18 mA				−0.9	−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = −8 mA		3.5	4.5		V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV,	I_{OL} = 8 mA			0.3	0.5	V
I_{OZ}	High-impedance-state output current		V_O = 0 V to V_{CC}					±20	µA
I_I	Bus input current	A or B inputs	V_{IH} = 12 V,	V_{CC} = 5 V,	Other inputs at 0 V	0.7		1	mA
			V_{IH} = 12 V,	V_{CC} = 0 V,	Other inputs at 0 V	0.8		1	
			V_{IH} = −7 V,	V_{CC} = 5 V,	Other inputs at 0 V	−0.5		−0.8	
			V_{IH} = −7 V,	V_{CC} = 0 V,	Other inputs at 0 V	−0.4		−0.8	
I_{IH}	High-level enable input current		V_{IH} = 5 V					±20	µA
I_{IL}	Low-level enable input current		V_{IL} = 0 V					−20	µA
I_{OS}	Short-circuit output current		V_O = 0			−80		−120	mA
I_{CC}	Supply current		Outputs enabled,	I_O = 0,	V_{ID} = 5 V		11	20	mA
			Outputs disabled				0.9	1.4	

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

5.7 Switching Characteristics

V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = −1.5 V to 1.5 V, See 图 6-1	11	22	30	ns
t_{PLH}	Propagation delay time, low- to high-level output		11	22	30	ns
t_{PZH}	Output enable time to high level	See 图 6-2		17	30	ns
t_{PZL}	Output enable time to low level	See 图 6-3		18	30	ns
t_{PHZ}	Output disable time from high level	See 图 6-2		30	40	ns
t_{PLZ}	Output disable time from low level	See 图 6-3		23	30	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	See 图 6-2		4	6	ns
t_t	Transition time	See 图 6-1		3	10	ns

6 Parameter Measurement Information

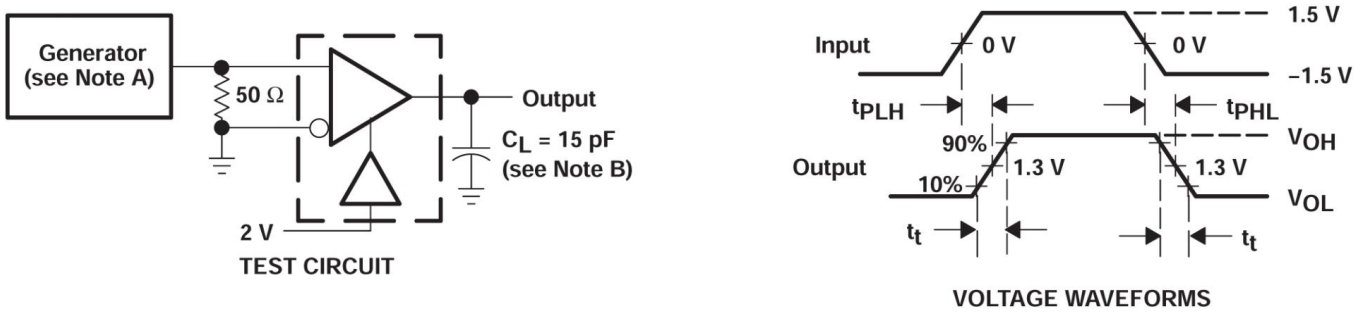
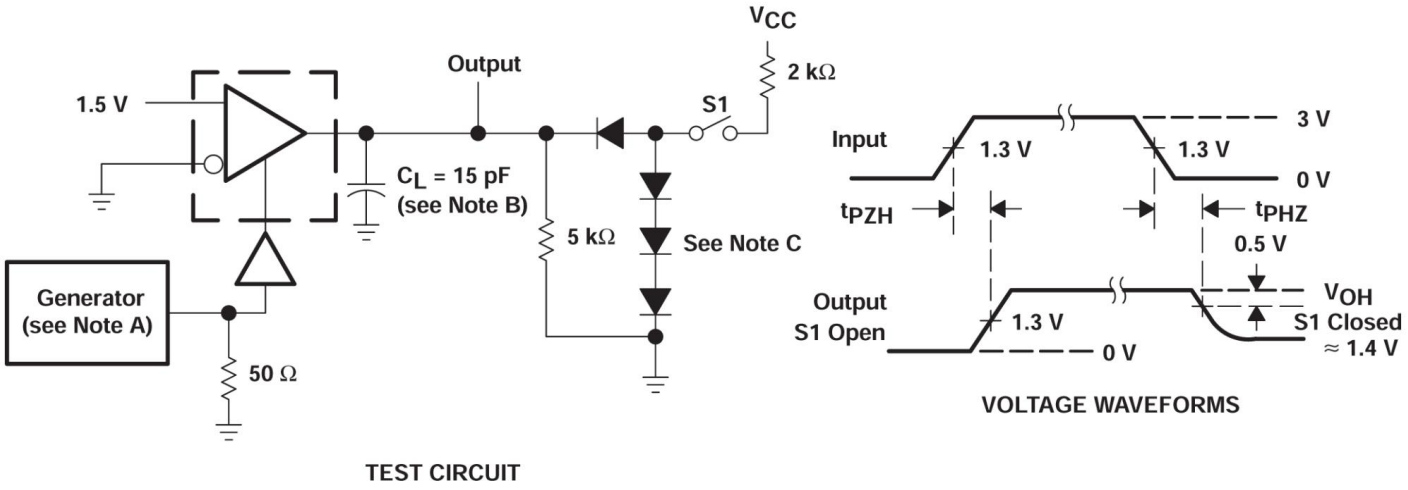


图 6-1. t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms

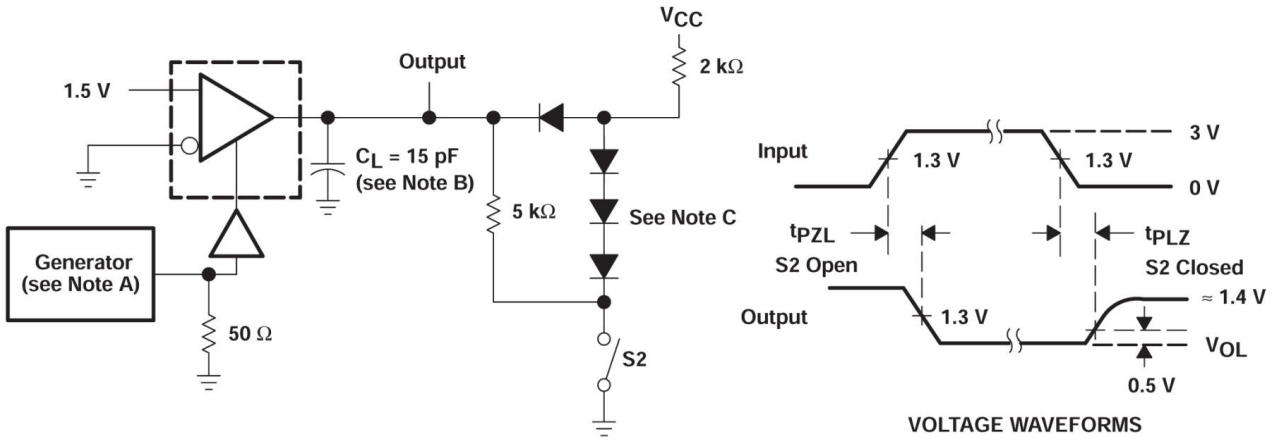


A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leqslant 6$ ns, $t_f \leqslant 6$ ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N916 or equivalent.

图 6-2. t_{PHZ} and t_{PZH} Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leqslant 6$ ns, $t_f \leqslant 6$ ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

7 Detailed Description

7.1 Device Functional Modes

表 7-1. Function Table (Each Receiver)

DIFFERENTIAL INPUTS	ENABLE(1)	OUTPUT
A–B		Y
$V_{ID} \geq 0.2$ V	H	H
−0.2 V < V_{ID} < 0.2 V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z
Open circuit	H	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

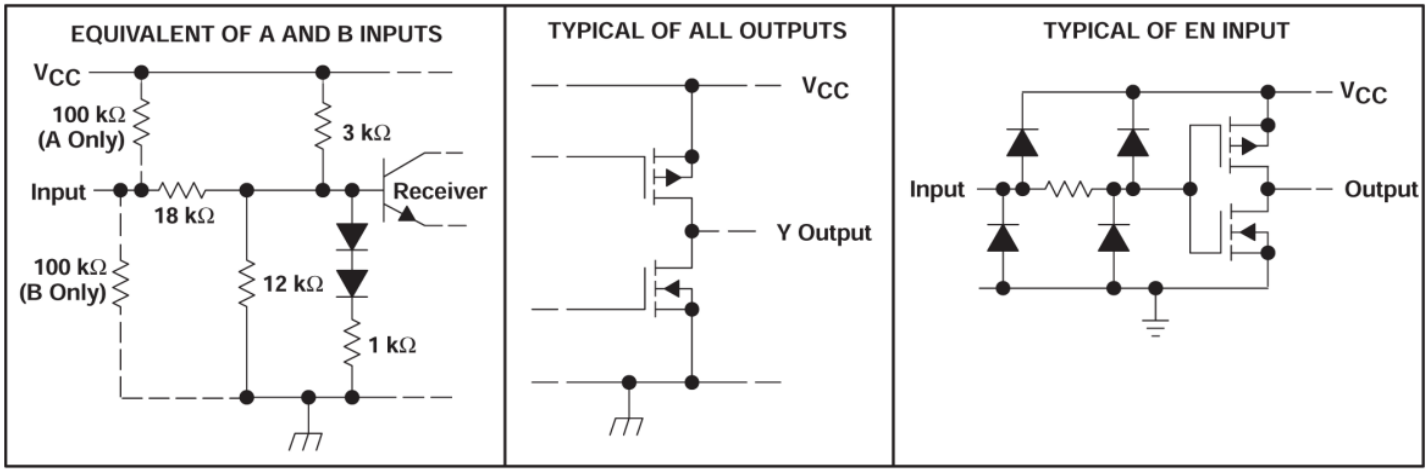
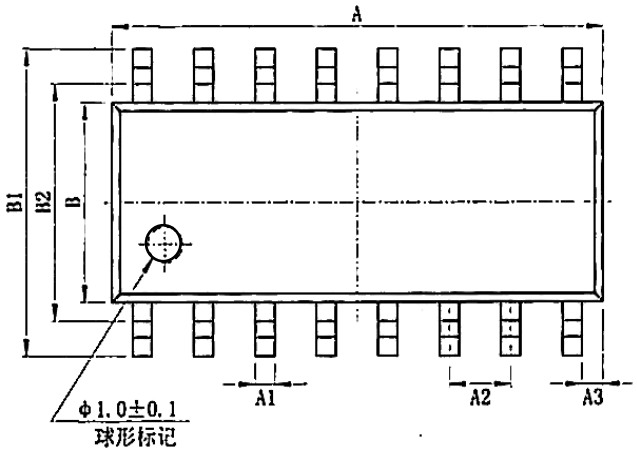


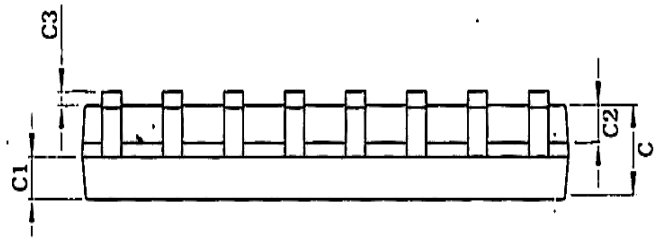
图 7-1. Schematics of Inputs and Outputs

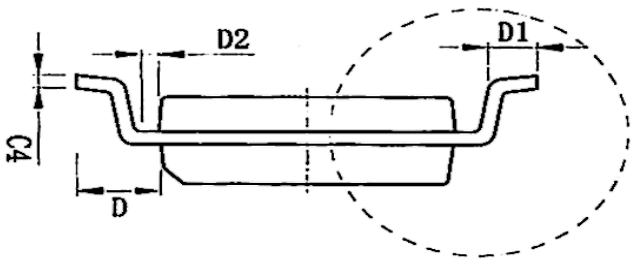
Order information

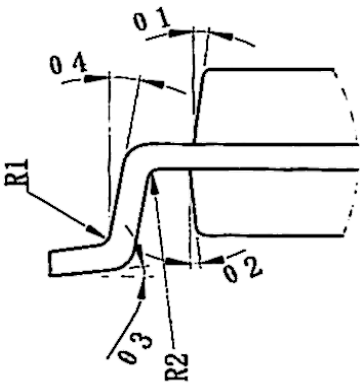
Order Number	Package	Package Quantity	Marking On The park
SN75LBC175DR-TUDI	SOP16	Tape,Reel,2500	SN75LBC175DR
SN75LBC175N-TUDI	DIP16	Tube,25,A box of 1000	SN75LBC175N

Package SOP16



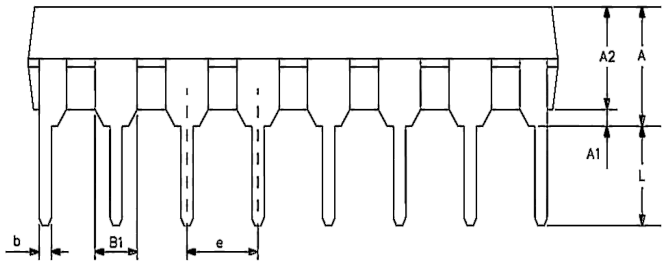


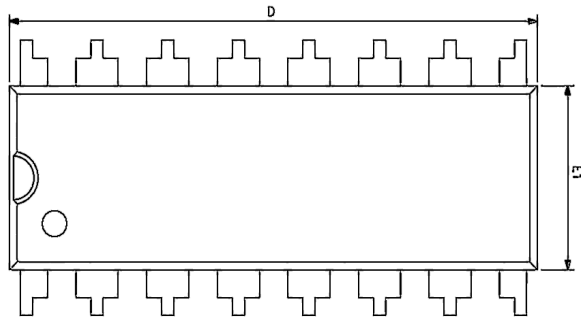


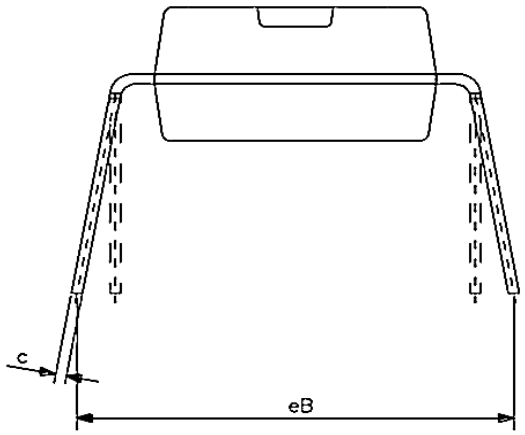


SIZE / SYMBOL	MIN./mm	MAX./mm
A	9.80	10.00
A1	0.356	0.456
A2	1.27TYP	
A3	0.302TYP	
B	3.85	3.95
B1	5.84	6.24
B2	5.00 TYP	
C	1.40	1.60
C1	0.61	0.71
C2	0.54	0.64
C3	0.05	0.25
C4	0.203	0.233
D	1.05 TYP	
D1	0.40	0.70
D2	0.15	0.25
R1	0.20TYP	
R2	0.20TYP	
01	8°~12°TYP4	
02	8°~12°TYP4	
03	0°~8°	
04	4°~12°	

Package DIP16







SIZE / SYMBOL	MIN./mm	MAX./mm
A2	3.20	3.60
A1	0.51	___
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
C	0.20	0.36
eB	7.62	9.30
R	0.20TYP	
R1	0.30TYP	
θ	0°	8°
θ1	45°TYP	
02	12°TYP	
03	0°	8°
04	0°	10°

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