NVH4L060N065SC1

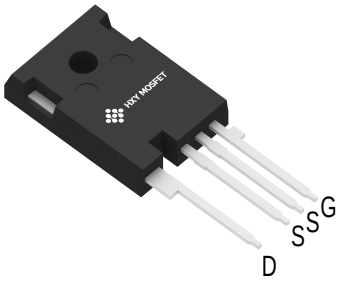
SiC Power MOSFET N-Channel Enhancement Mode

Features

- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

Benefits

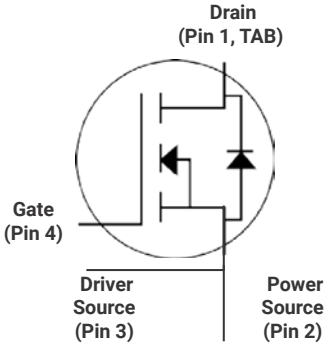
- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency



TO-247H-4L

Applications

- EV chargers
- Server & Telecom PSU
- UPS
- Solar inverters
- SMPS
- DC/DC converters



Ordering Part Number	Package	Brand	T_J , T_{stg} Range
NVH4L060N065SC1	TO-247H-4L	HXY MOSFET	-55 - 150 ˚C

Maximum Ratings (T_C = 25 ˚C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	650	V	V_{GS} = 0 V, I_D = 100 µA	
V_{GS}	Gate - Source voltage (Under transient events)	-8/+19	V	AC (f >1 Hz)	Fig.28
I_D	Continuous Drain Current	49	A	V_{GS} = 15 V, T_C = 25˚C	Fig. 19
		35		V_{GS} = 15 V, T_C = 100˚C	
$I_{D(pulse)}$	Pulsed Drain Current	132	A	Pulse width t_P limited by T_{jmax}	
P_D	Power Dissipation	176	W	T_C=25˚C, T_J = 175 ˚C	Fig. 20
T_J , T_{stg}	Operating Junction and Storage Temperature	-40 to +175	˚C		
T_L	Solder Temperature	260	˚C	1.6mm (0.063") from case for 10s	
M_d	Mounting Torque, (M3 or 6-32 screw)	1 8.8	Nm lbf-in		

Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	650			V	V_{GS} = 0 V, I_D = 100 µA	
V_{GSon}	Gate-Source Recommended Turn-On Voltage		15		V	Static	Fig. 28
V_{GSoff}	Gate-Source Recommended Turn-Off Voltage		-4		V		
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.6	3.6	V	V_{DS} = V_{GS}, I_D = 4.84 mA	Fig. 11
			2.2		V	V_{DS} = V_{GS}, I_D = 23 mA, T_J = 175°C	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	µA	V_{DS} = 650 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		45	60	mΩ	V_{GS} = 15 V, I_D = 17.6 A	Fig. 4, 5, 6
			61			V_{GS} = 15 V, I_D = 17.6A, T_J = 175°C	
g_{fs}	Transconductance		12		S	V_{DS}= 20 V, I_{DS}= 17.6 A	Fig. 7
			11			V_{DS}= 20 V, I_{DS}= 17.6 A, T_J = 175°C	
C_{iss}	Input Capacitance		1621		pF	V_{GS} = 0 V, V_{DS} = 0V to 600 V f = 1 MHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		101				
C_{rss}	Reverse Transfer Capacitance		8				
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		126			V_{GS} = 0 V, V_{DS} = 0V to 400 V	Note:1
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		178				
E_{oss}	C_{oss} Stored Energy		20		µJ	V_{GS} = 600 V, f = 1 MHz	Fig. 16
E_{ON}	Turn-On Switching Energy (Body Diode)		57		µJ	V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 17.6A, $R_{G(ext)}$ = 2.5 Ω, L = 99 µH, T_J = 175°C FWD = Internal Body Diode of MOSFET	Fig. 24
E_{OFF}	Turn-Off Switching Energy (Body Diode)		14				
E_{ON}	Turn-On Switching Energy (External Diode)		44		µJ	V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 17.6A, $R_{G(ext)}$ = 2.5 Ω, L = 99 µH, T_J = 175°C FWD = Internal Body Diode of MOSFET	Fig. 24
E_{OFF}	Turn Off Switching Energy (External Diode)		14				
$t_{d(on)}$	Turn-On Delay Time		9		ns	V_{DD} = 400 V, V_{GS} = -4 V/15 V I_D = 17.6 A, $R_{G(ext)}$ = 2.5 Ω, L = 99 µH, Timing relative to V_{DS} Inductive load	Fig. 25
t_r	Rise Time		12				
$t_{d(off)}$	Turn-Off Delay Time		18				
t_f	Fall Time		6				
$R_{G(int)}$	Internal Gate Resistance		3		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		21		nC	V_{DS} = 400 V, V_{GS} = -4 V/15 V I_D = 17.6 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		18				
Q_g	Total Gate Charge		63				

Note (1): $C_{o(er)}$, a lumped capacitance that gives same stored energy as Coss while Vds is rising from 0 to 400V
$C_{o(tr)}$, a lumped capacitance that gives same charging time as Coss while Vds is rising from 0 to 400V

Reverse Diode Characteristics (T_C = 25˚C unles1s otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.8		V	V_{GS} = -4 V, I_{SD} = 8.8 A T_J = 25 °C	Fig. 8, 9, 10
		4.2		V	V_{GS} = -4 V, I_{SD} = 8.8 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current		29	A	V_{GS} = -4 V, T_J = 25 ˚C	
$I_{S,\ pulse}$	Diode pulse Current		132	A	V_{GS} = -4 V, pulse width t_P limited by T_{jmax}	
t_{rr}	Reverse Recover time	13		ns	V_{GS} = -4 V, I_{SD} = 17.6A, V_R = 400 V dif/dt = 4000 A/μs, T_J = 175 °C	
Q_{rr}	Reverse Recovery Charge	247		nC		
I_{rrm}	Peak Reverse Recovery Current	36		A		
t_{rr}	Reverse Recover time	18		ns	V_{GS} = -4 V, I_{SD} = 17.6A, V_R = 400 V dif/dt = 5500 A/μs, T_J = 175 °C	
Q_{rr}	Reverse Recovery Charge	171		nC		
I_{rrm}	Peak Reverse Recovery Current	16		A		

Thermal Characteristics

Symbol	Parameter	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.85	°C/W		Fig. 21
$R_{\theta JA}$	Thermal Resistance From Junction to Ambient	40			

Typical Performance

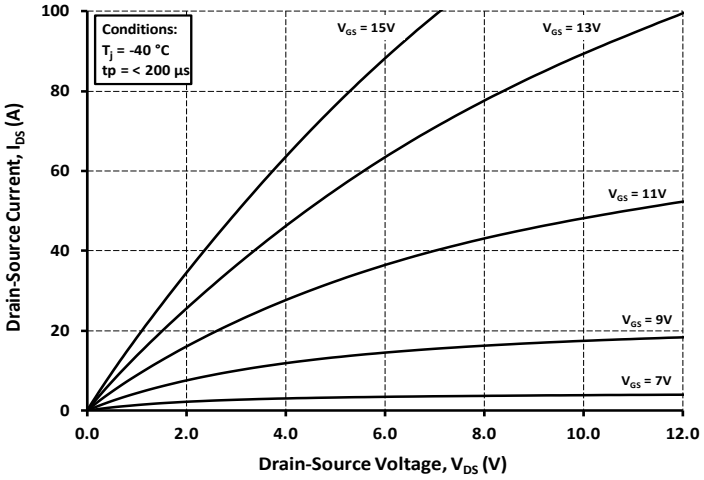


Figure 1. Output Characteristics T_J = -40 °C

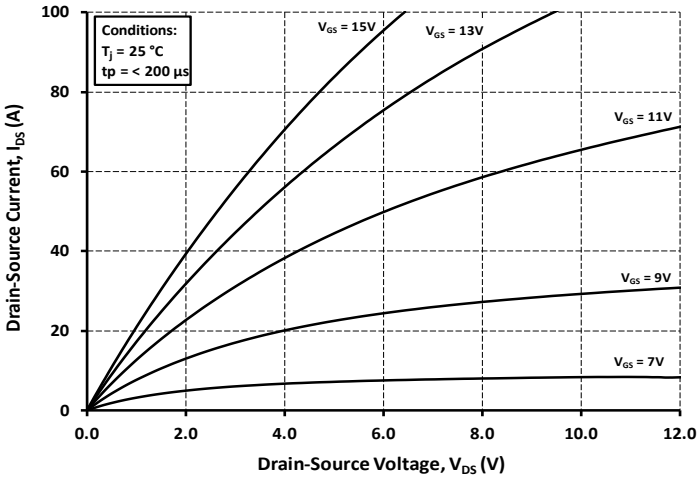


Figure 2. Output Characteristics T_J = 25 °C

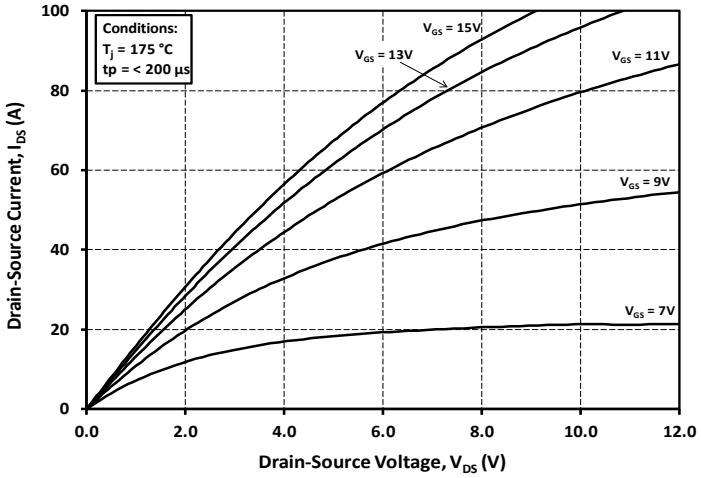


Figure 3. Output Characteristics T_J = 175 °C

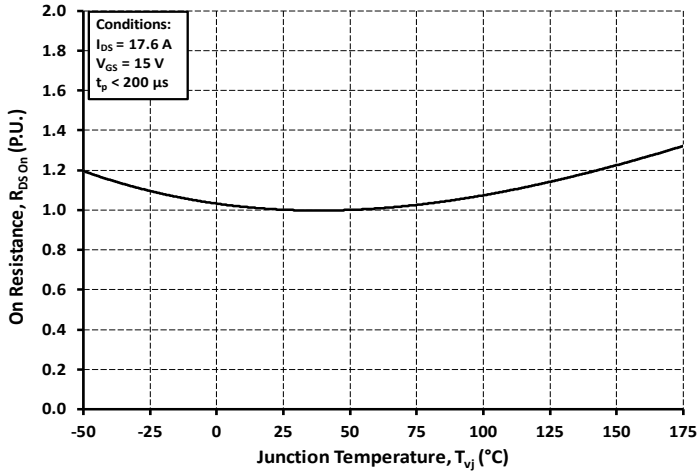


Figure 4. Normalized On-Resistance vs. Temperature

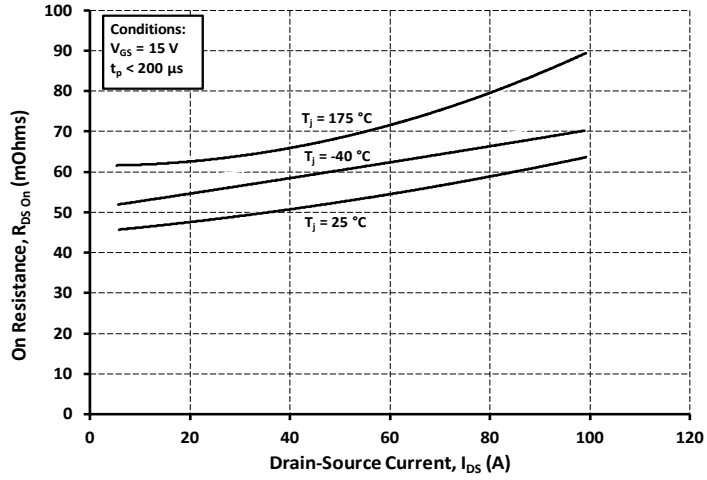


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

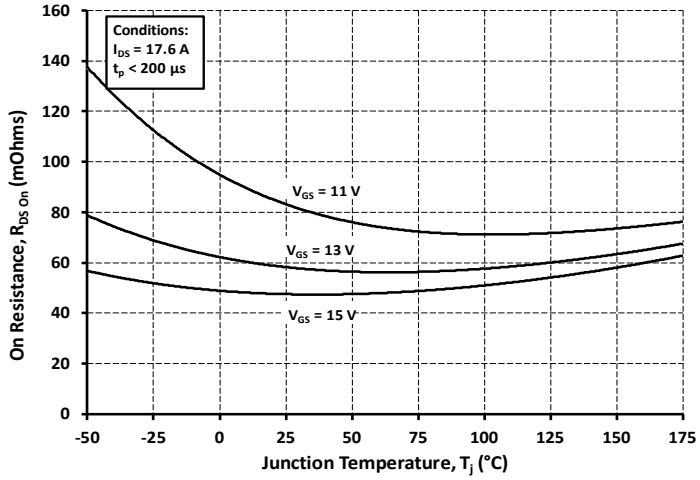


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

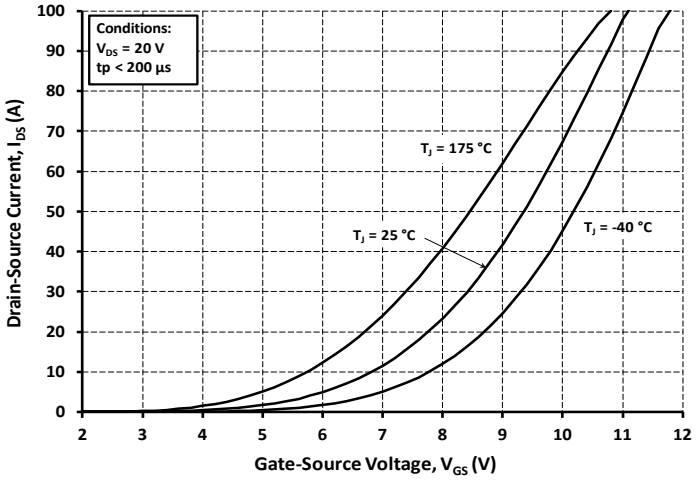


Figure 7. Transfer Characteristic for Various Junction Temperatures

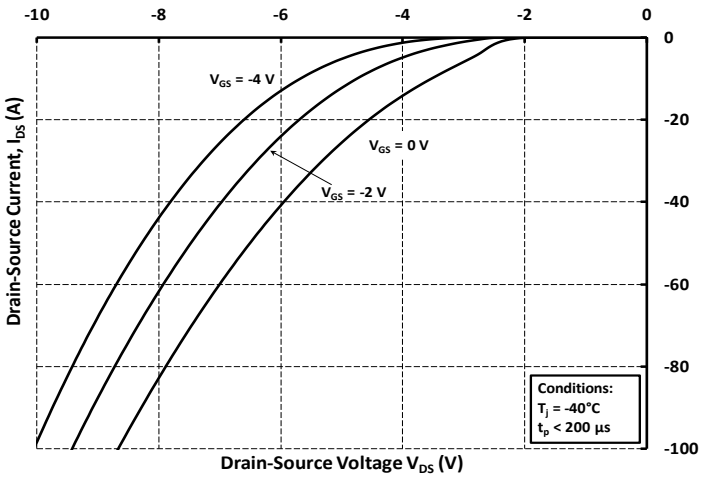


Figure 8. Body Diode Characteristic at -40 °C

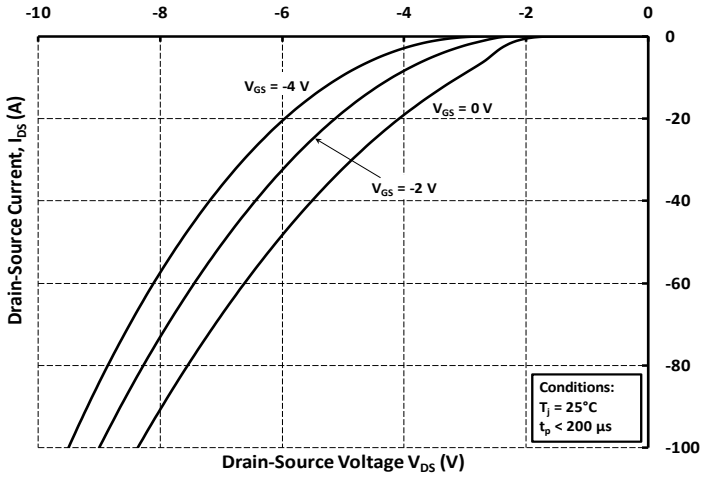


Figure 9. Body Diode Characteristic at 25 °C

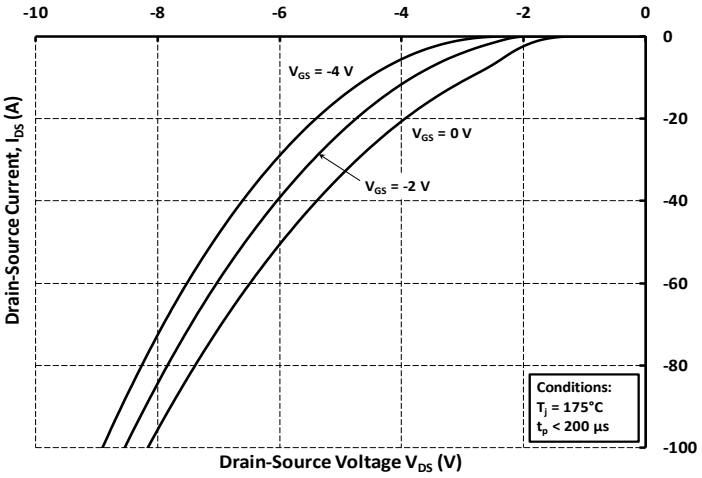


Figure 10. Body Diode Characteristic at 175 °C

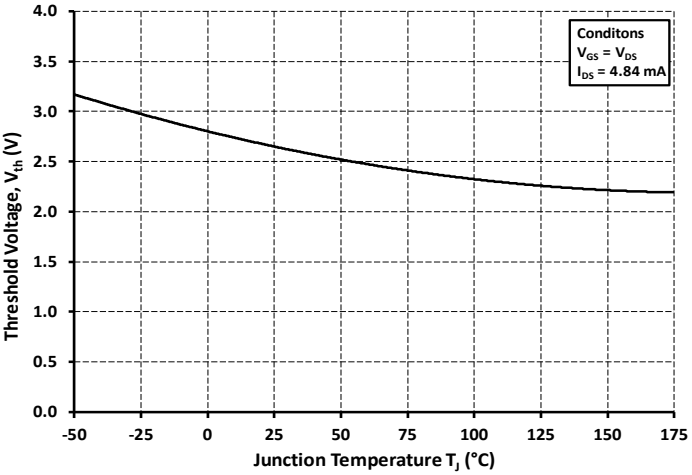


Figure 11. Threshold Voltage vs. Temperature

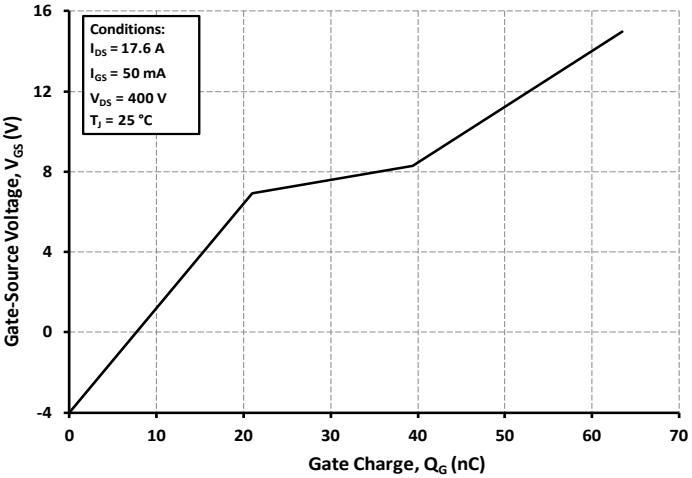


Figure 12. Gate Charge Characteristics

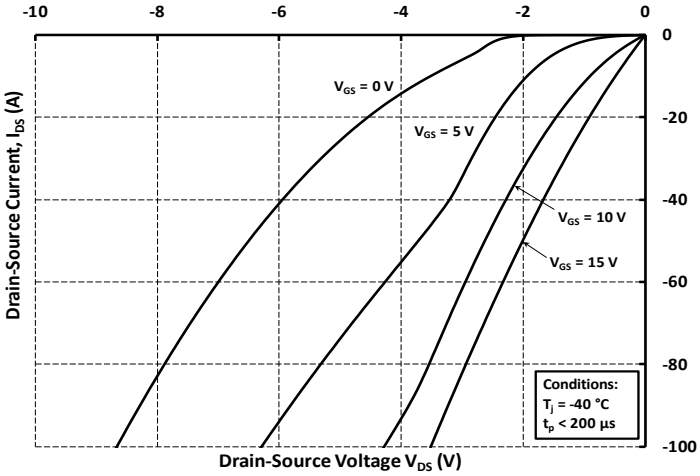


Figure 13. 3rd Quadrant Characteristic at -40 ºC

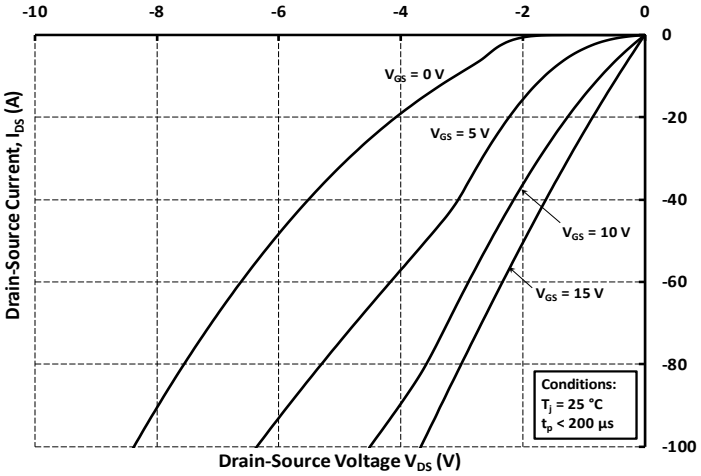


Figure 14. 3rd Quadrant Characteristic at 25 ºC

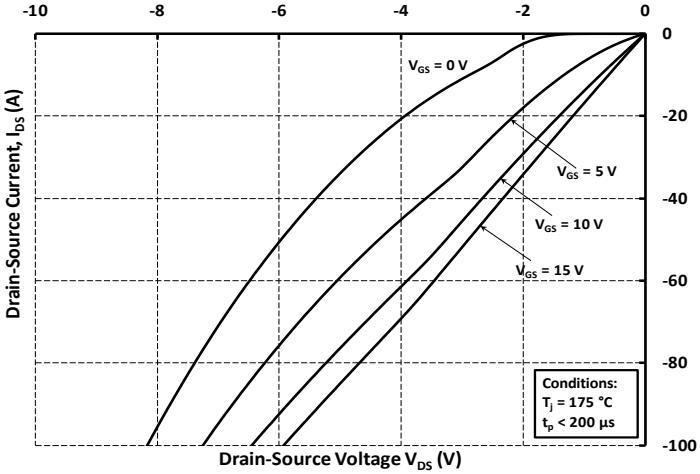


Figure 15. 3rd Quadrant Characteristic at 175 ºC

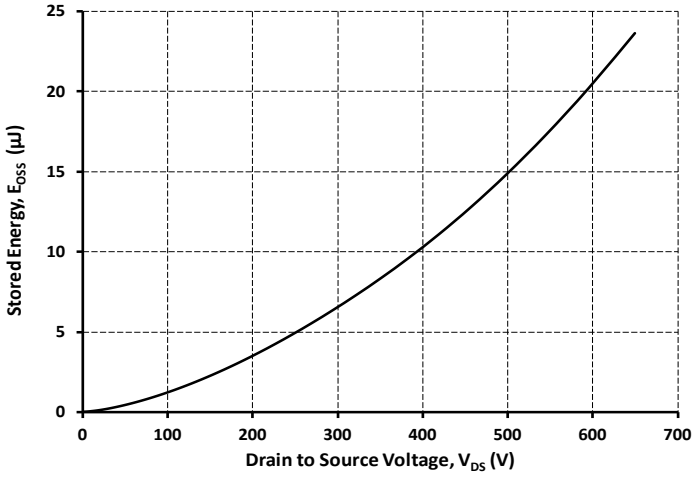


Figure 16. Output Capacitor Stored Energy

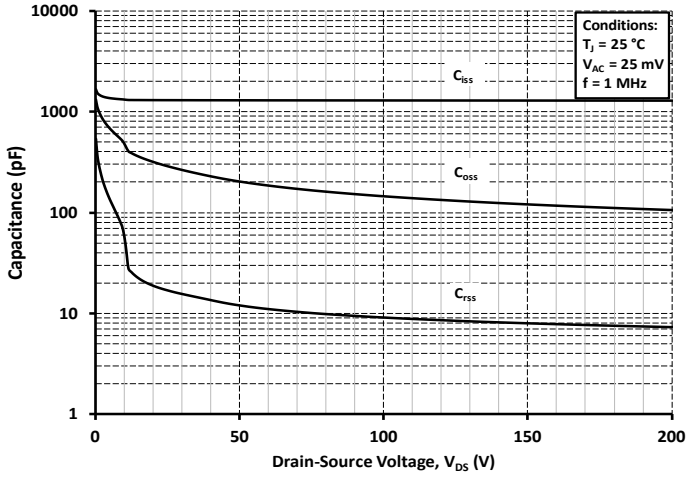


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

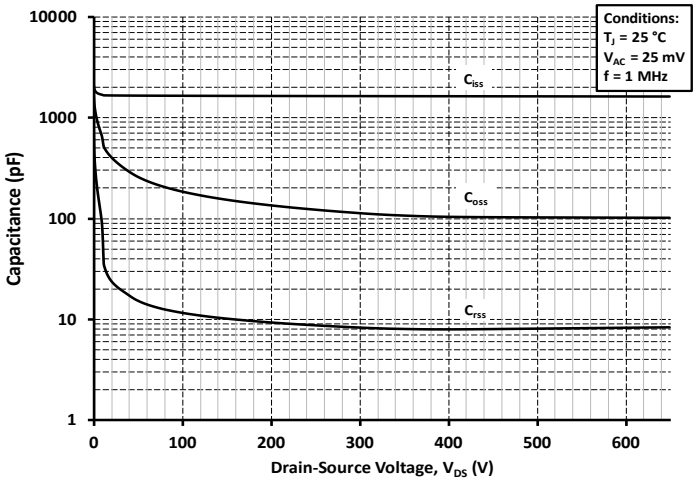


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650V)

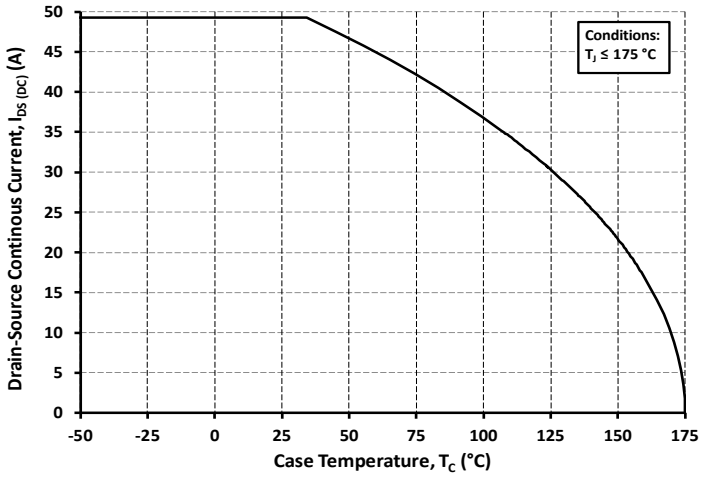


Figure 19. Continuous Drain Current Derating vs. Case Temperature

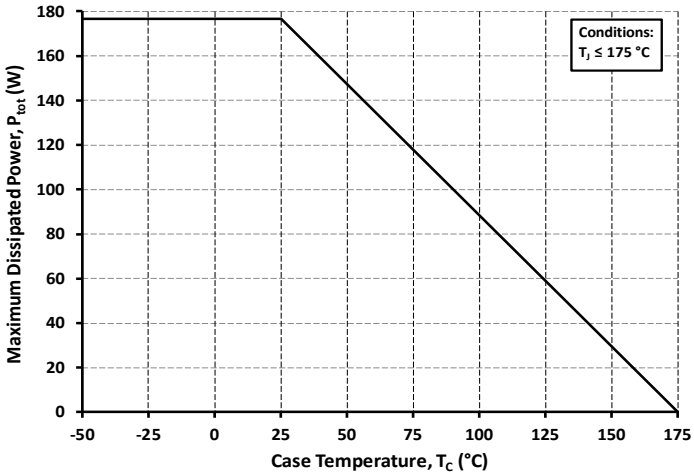


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

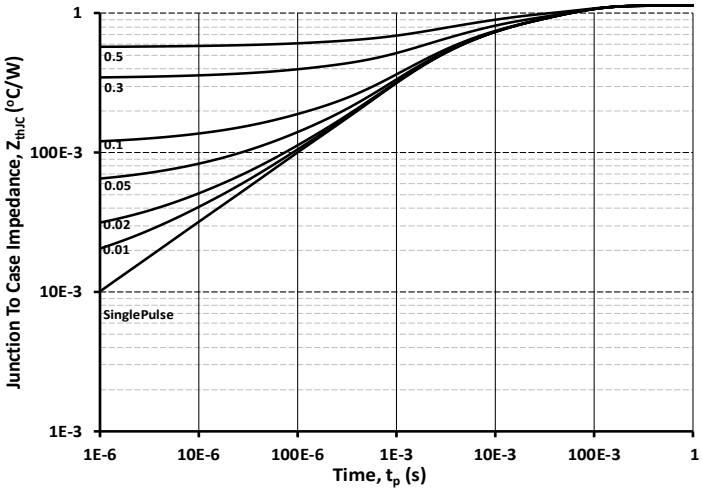


Figure 21. Transient Thermal Impedance (Junction - Case)

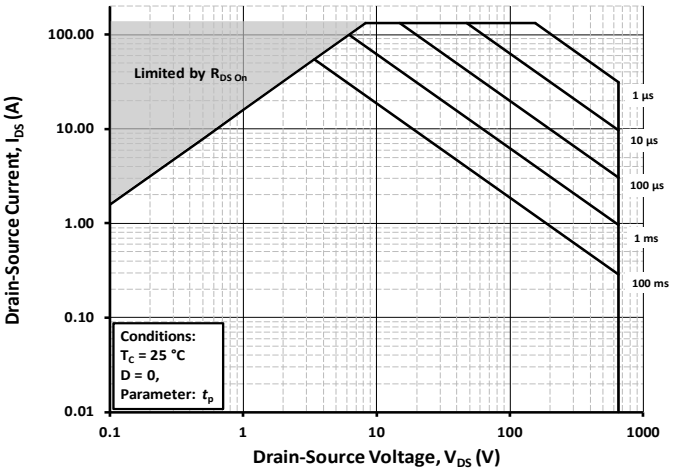


Figure 22. Safe Operating Area

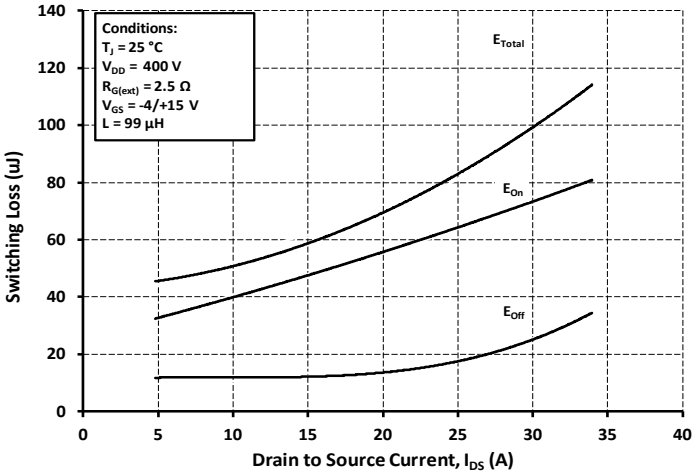


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 400V)

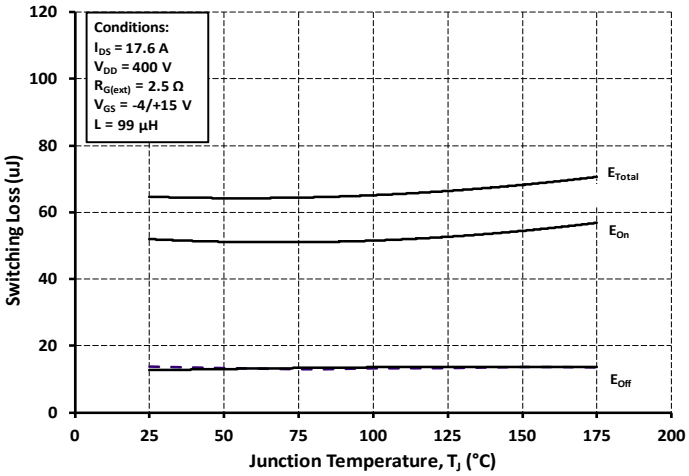


Figure 24. Clamped Inductive Switching Energy vs. Temperature

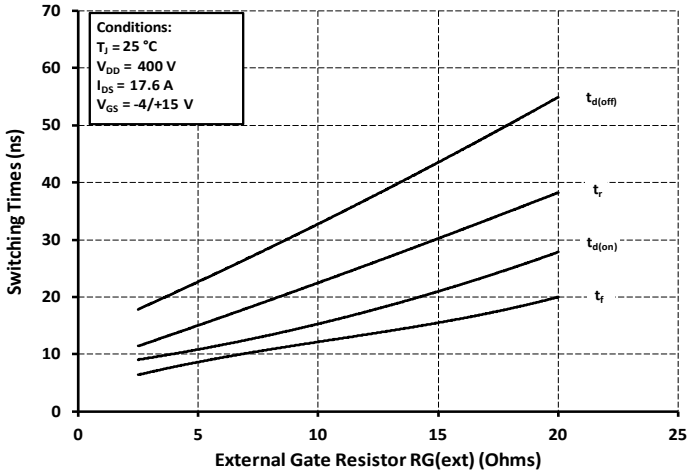


Figure 25. Switching Times vs. $R_{G(ext)}$

Test Circuit Schematic

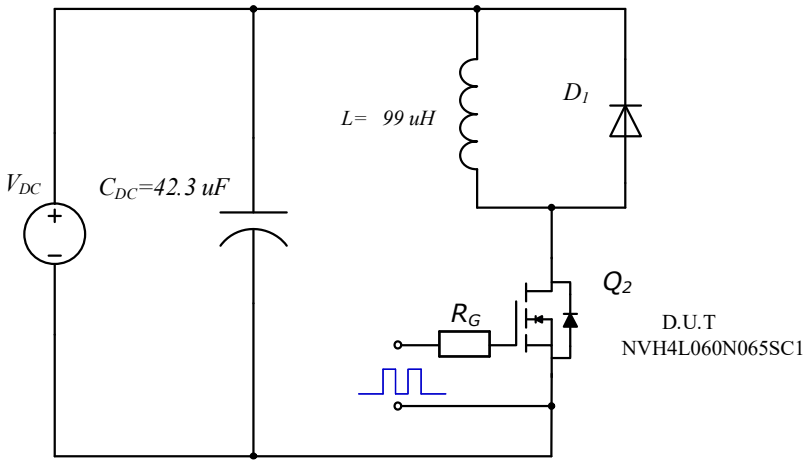


Figure 26. Clamped Inductive Switching Waveform Test Circuit

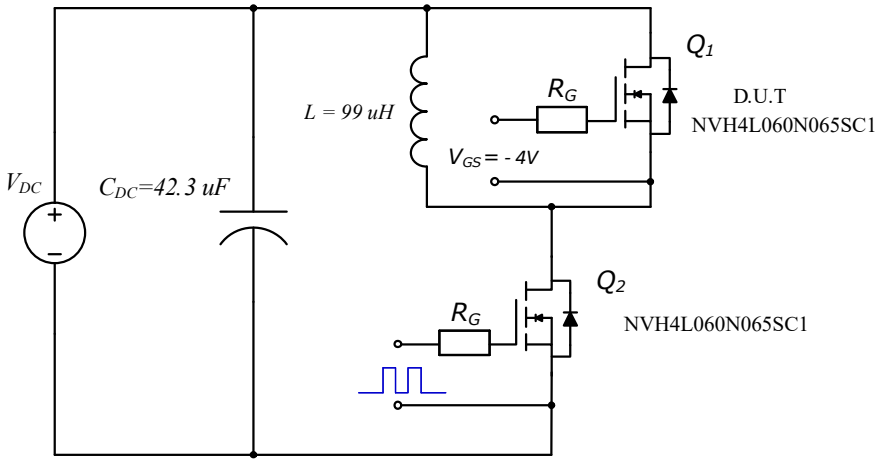


Figure 27. Body Diode Recovery Test Circuit

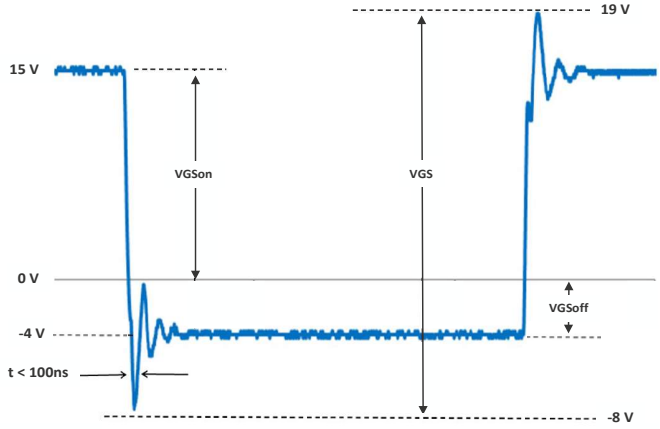
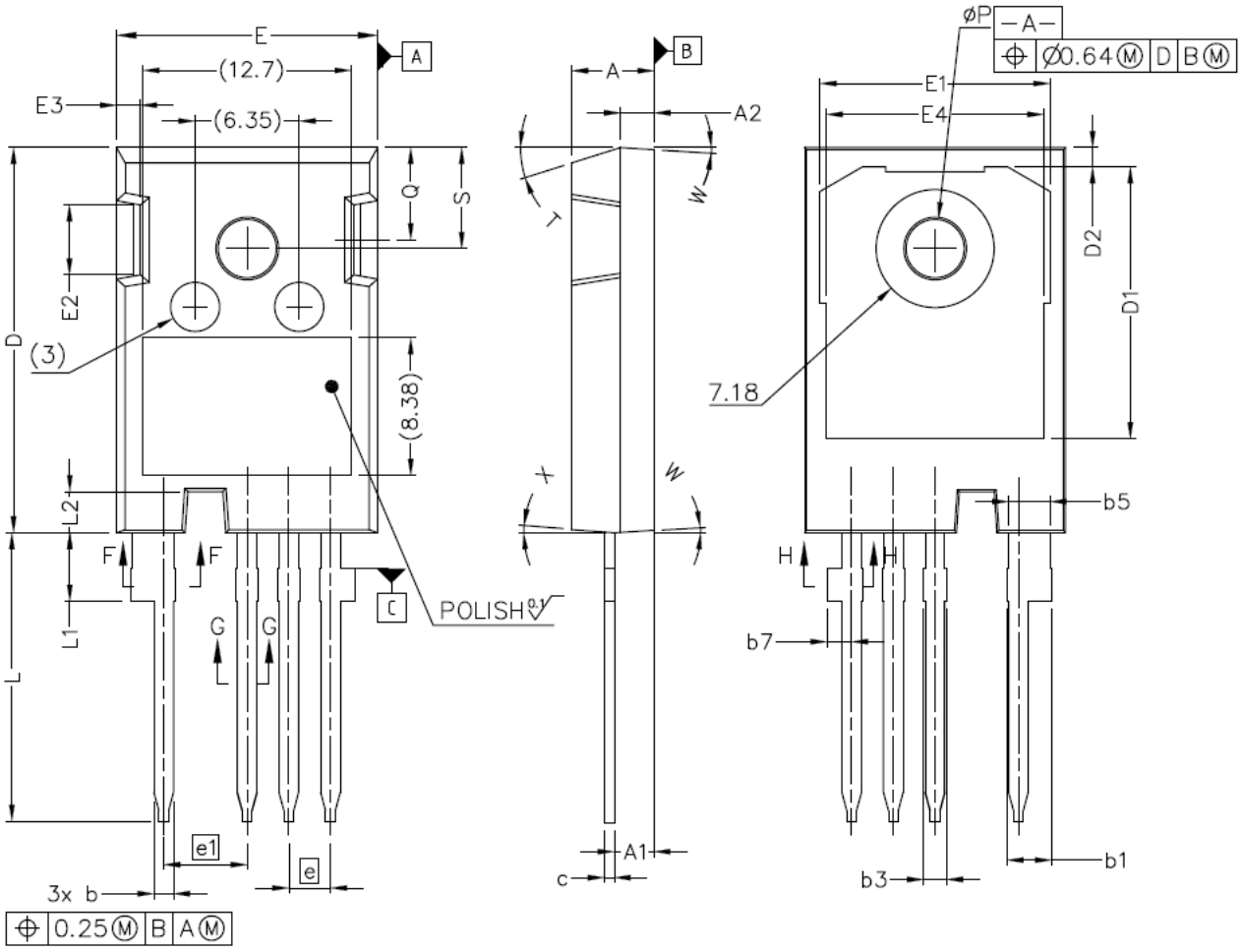
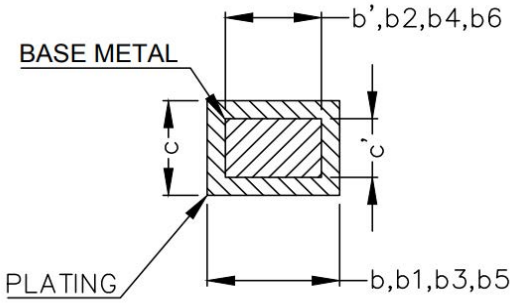


Figure 28. V_{GS} Waveform Example

Package Dimensions

Package TO-247H-4L





SECTION "F-F", "G-G" AND "H-H"
SCALE: NONE

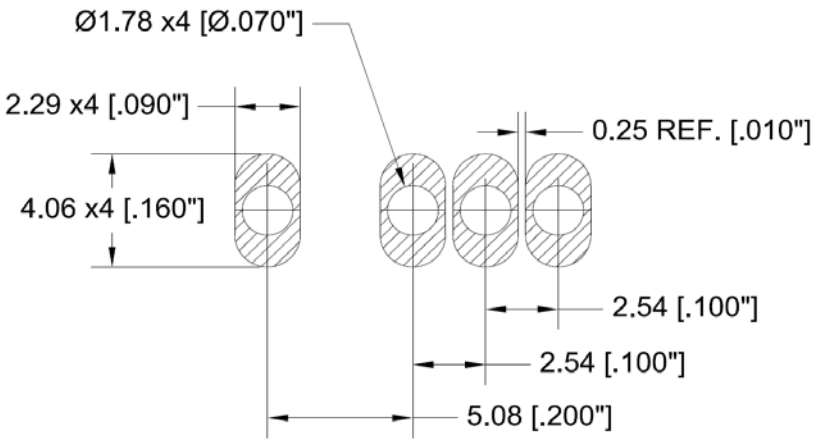
Package Dimensions

Package TO-247H-4L

NOTE ;
1. ALL METAL SURFACES: TIN PLATED, EXCEPT AREA OF CUT
2. DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. 'N' IS THE NUMBER OF TERMINAL POSITIONS

SYM	MILLIMETERS	
	MIN	MAX
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b`	1.07	1.28
b	1.07	1.33
b1	2.39	2.94
b2	2.39	2.84
b3	1.07	1.60
b4	1.07	1.50
b5	2.39	2.69
b6	2.39	2.64
b7	1.30	1.70
c`	0.55	0.65
c	0.55	0.68
D	23.30	23.60
D1	16.25	17.65
D2	0.95	1.25
E	15.75	16.13

SYM	MILLIMETERS	
	MIN	MAX
E1	13.10	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
e	2.54 BSC	
e1	5.08 BSC	
N*	4	
L	17.31	17.82
L1	3.97	4.37
L2	2.35	2.65
Ø P	3.51	3.65
Q	5.49	6.00
S	6.04	6.30
T	17.5° REF.	
W	3.5° REF.	
X	4° REF.	



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give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.

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HXY MOSFET:

60N06 AQ15C-01FTG AZ4007-01H ESD5LM5.0C-HXY HPTVSUC3D5VB HSD15C.TCT HSG3D15B3.3MA LM393DR-HXY PJEC5V0M1FN2 HSTS521050B331 PESDLC2FD3V3BH AZ4836-01L HCEZ36V,L3F HESD36VD3B HRCLAMP3371ZCTFT HSEN2411D3 ESD5L5.0C-HXY HESDSLC3V3D3B PESDNC2XD5VBL RLSD32A121V TPSMB100CA-VR HLY323BC1524L PESDSC2FD5VU TPSMB28A-VR HAZ4007-01H PESDNC2XD5VBF PJSD24CW_R1 BV05C-H HACPDQC5V0-HF HSEN3611D3