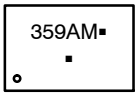
MOSFET – N-Channel, POWERTRENCH®, Logic Level

FDN359AN



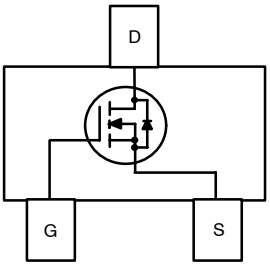
SOT−23
CASE 527AG

MARKING DIAGRAM



359A = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)



General Description

This N−Channel Logic Level MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize the on−state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in−line power loss and fast switching are required.

Features

- 2.7 A, 30 V
  - $R_{DS(ON)}$ = 0.046 Ω @ V_{GS} = 10 V
  - $R_{DS(ON)}$ = 0.060 Ω @ V_{GS} = 4.5 V
- Very Fast Switching
- Low Gate Charge (5 nC Typical)
- High Power Version of Industry Standard SOT−23 Package. Identical Pin out to SOT−23 with 30% Higher Power Handling Capability

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain−Source Voltage	30	V
V_{GSS}	Gate−Source Voltage	±20	V
I_D	Drain Current Continuous (Note 1a) Pulsed	 2.7 15	A
P_D	Power Dissipation for Single Operation (Note 1a) (Note 1b)	 0.5 0.46	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case (Note 1)	75	°C/W

ORDERING INFORMATION

Device	Package	Shipping†
FDN359AN	SOT−23 (Pb-Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	23	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 24 V, V_{GS} = 0 V ,T_J = 55°C	–	–	10	
I_{GSSF}	Gate−Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	–	–	100	nA
I_{GSSR}	Gate−Body Leakage, Reverse	V_{GS} = −20 V, V_{DS} = 0 V	–	–	−100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1	1.6	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	−4	–	mV/°C
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 2.7 A	–	0.037	0.046	Ω
		V_{GS} = 10 V, I_D = 2.7 A ,T_J = 125°C	–	0.055	0.075	
		V_{GS} = 4.5 V, I_D = 2.4 A	–	0.049	0.06	
$I_{D(on)}$	On−State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	15	–	–	A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 2.7 A	–	9.5	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	–	480	–	pF
C_{oss}	Output Capacitance		–	120	–	pF
C_{rss}	Reverse Transfer Capacitance		–	45	–	pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 5 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω	–	6	12	ns
t_r	Turn−On Rise Time		–	13	24	ns
$t_{d(off)}$	Turn−Off Delay Time		–	15	27	ns
t_f	Turn−Off Fall Time		–	4	10	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 2.7 A, V_{GS} = 5 V	–	5	7	nC
Q_{gs}	Gate−Source Charge		–	1.4	–	nC
Q_{gd}	Gate−Drain Charge		–	1.6	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	0.42	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.42 A (Note 2)	–	0.65	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
   Typical $R_{\theta JA}$ using the board layouts shown below on FR−4 PCB in a still air environment



a) 250°C/W when mounted on a 0.02 in^2 pad of 2 oz copper



b) 270°C/W when mounted on a minimum pad

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

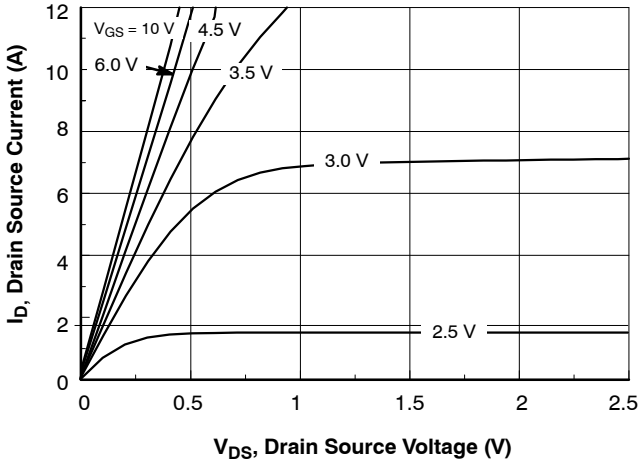


Figure 1. On−Region Characteristics

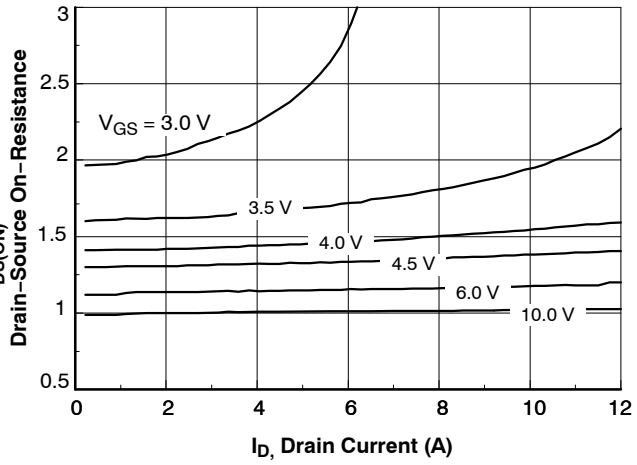


Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

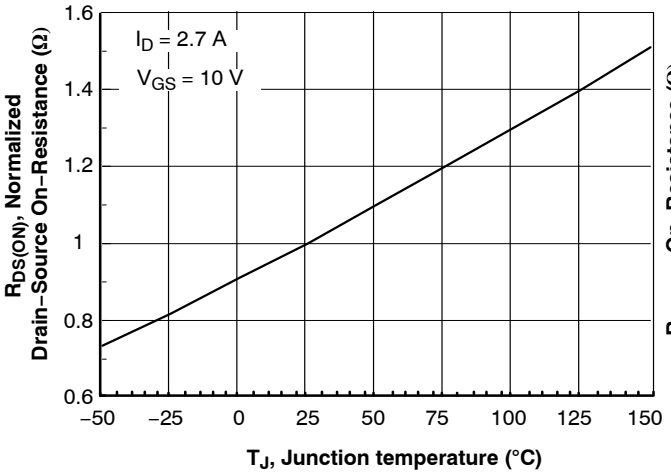


Figure 3. On−Resistance Variation with Temperature

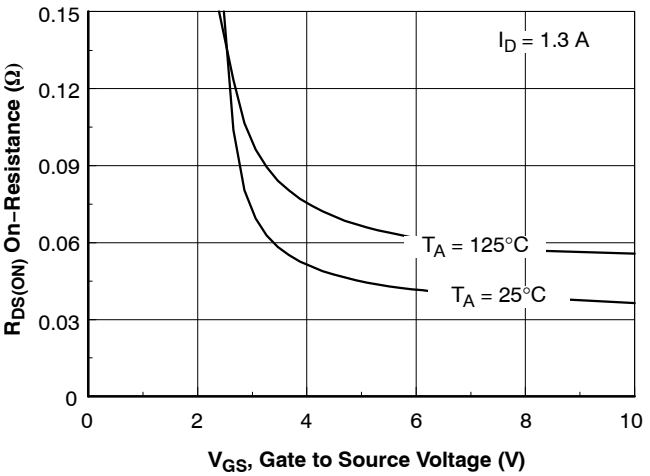


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

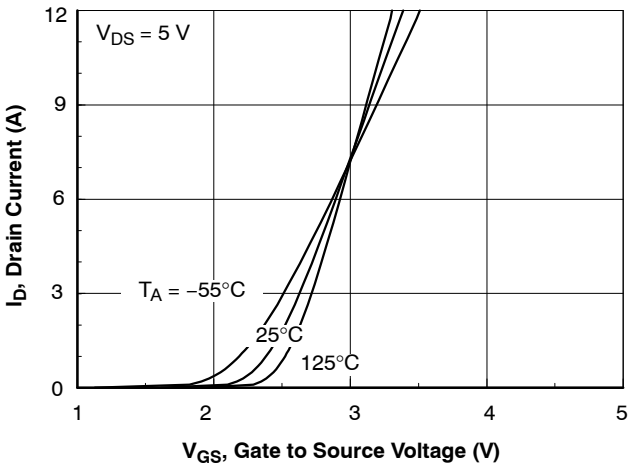


Figure 5. Transfer Characteristics

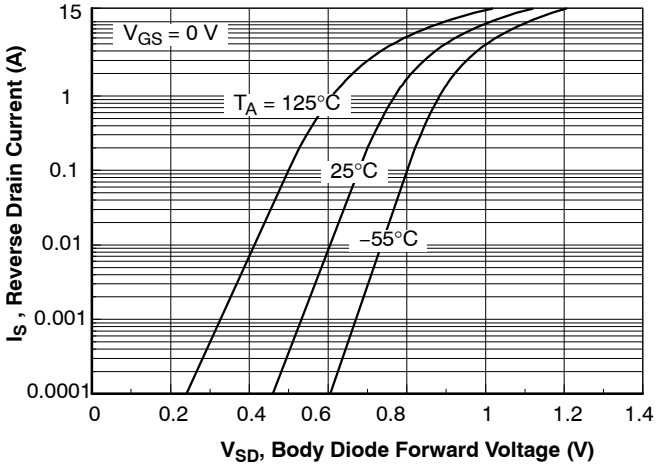


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (CONTINUED)

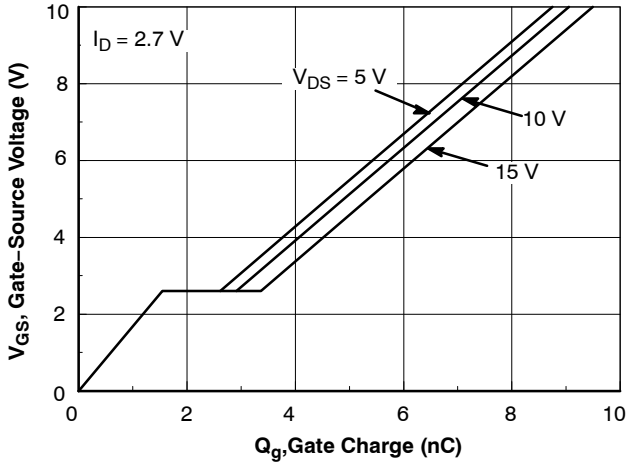


Figure 7. Gate Charge Characteristics

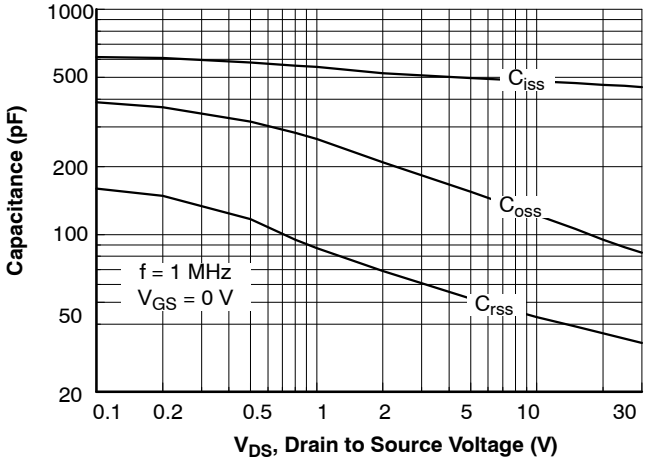


Figure 8. Capacitance Characteristics

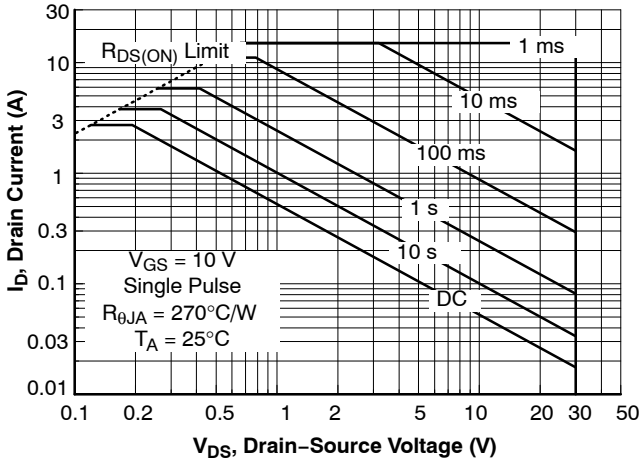


Figure 9. Maximum Safe Operating Area

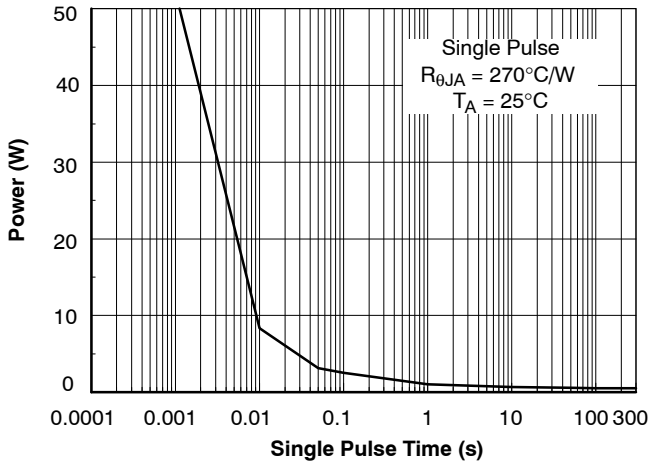


Figure 10. Single Pulse Maximum Power Dissipation

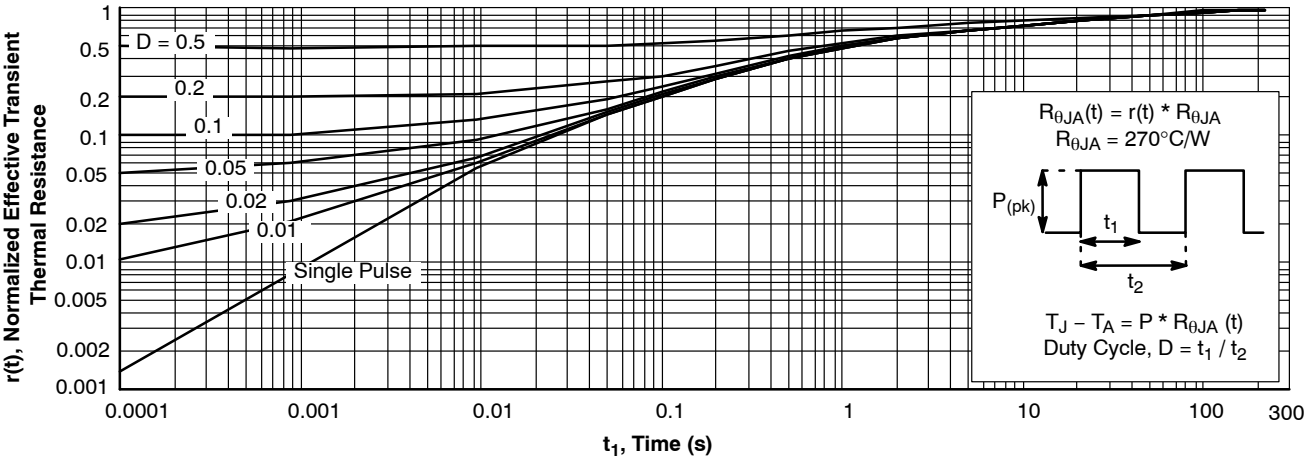
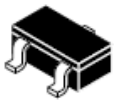


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

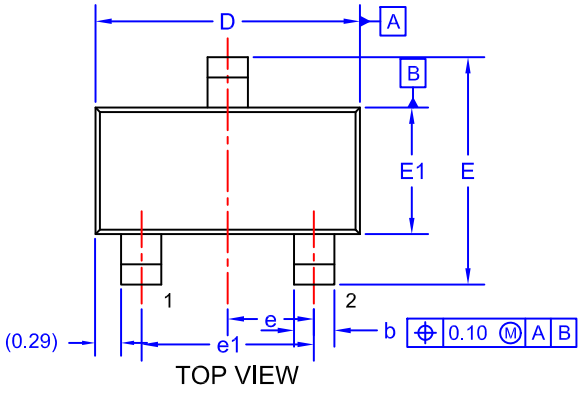
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SOT−23/SUPERSOT™ −23, 3 LEAD, 1.4x2.9
CASE 527AG
ISSUE A

DATE 09 DEC 2019

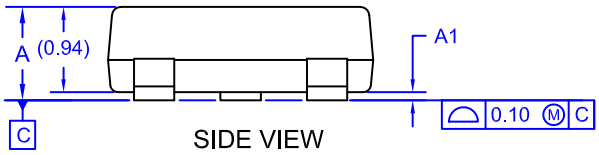


TOP VIEW

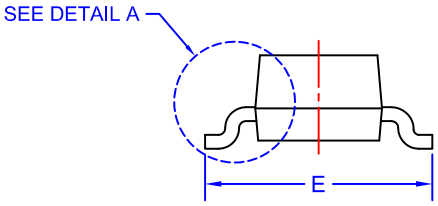
NOTES: UNLESS OTHERWISE SPECIFIED

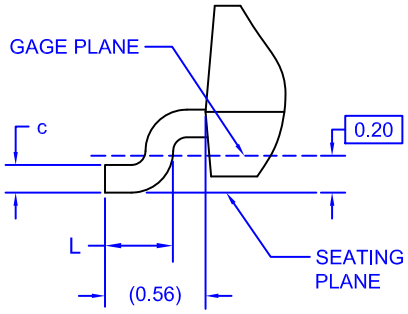
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

DIM	MIN.	NOM.	MAX.
A	0.85	0.95	1.12
A1	0.00	0.05	0.10
b	0.370	0.435	0.508
c	0.085	0.150	0.180
D	2.80	2.92	3.04
E	2.31	2.51	2.71
E1	1.20	1.40	1.52
e	0.95 BSC		
e1	1.90 BSC		
L	0.33	0.38	0.43

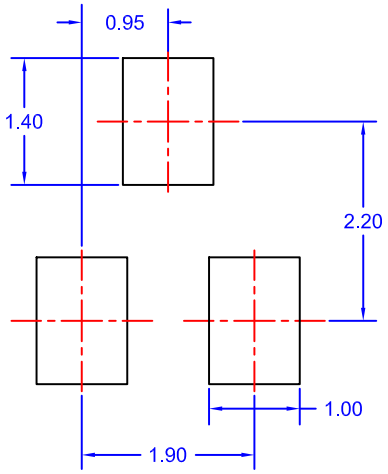


SIDE VIEW





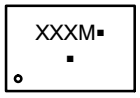
DETAIL A



LAND PATTERN RECOMMENDATION*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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