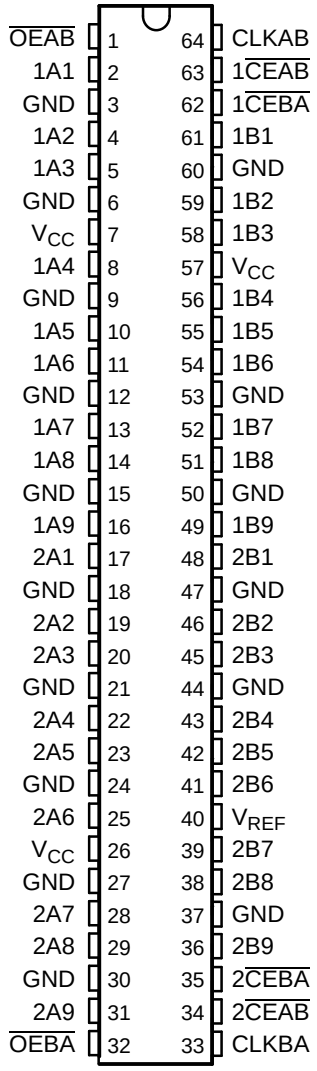
SN74GTL16622A
18-BIT LVTTL-TO-GTL/GTL+ BUS TRANSCEIVER

SCBS673F–AUGUST 1996–REVISED APRIL 2005

FEATURES

- **Member of Texas Instruments Widebus™ Family**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **D-Type Flip-Flops With Qualified Storage Enable**
- **Translates Between GTL/GTL+ Signal Levels and LVTTL Logic Levels**
- **Supports Mixed-Mode (3.3 V and 5 V) Signal Operation on A-Port and Control Inputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors on A Port**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Noise**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **– 2000-V Human-Body Model (A114-A)**
  - **– 200-V Machine Model (A115-A)**
  - **– 1000-V Charged-Device Model (C101)**

DGG PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74GTL16622A is an 18-bit registered bus transceiver that provides LVTTL-to-GTL/GTL+ and GTL/GTL+-to-LVTTL signal-level translation. This device is partitioned as two separate 9-bit transceivers with individual clock-enable controls and contains D-type flip-flops for temporary storage of data flowing in either direction. This device provides an interface between cards operating at LVTTL logic levels and a backplane operating at GTL/GTL+ signal levels. Higher-speed operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and OEC™ circuitry.

The user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or the preferred higher noise margin GTL+ (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels. GTL+ is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The B port normally operates at GTL or GTL+ signal levels, while the A-port and control inputs are compatible with LVTTL logic levels and are 5-V tolerant. V_{REF} is the reference input voltage for the B port.

Data flow in each direction is controlled by the output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) and clock (CLKAB and CLKBA) inputs. The clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs control each 9-bit transceiver independently, which makes the device more versatile.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus, OEC are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1996–2005, Texas Instruments Incorporated

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

For A-to-B data flow, the device operates on the low-to-high transition of CLKAB if $\overline{CEAB}$ is low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B, but uses $\overline{OEBA}$, CLKBA, and $\overline{CEBA}$.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Active bus-hold circuitry holds unused or undriven LVTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTL16622ADGGR	GTL16622A

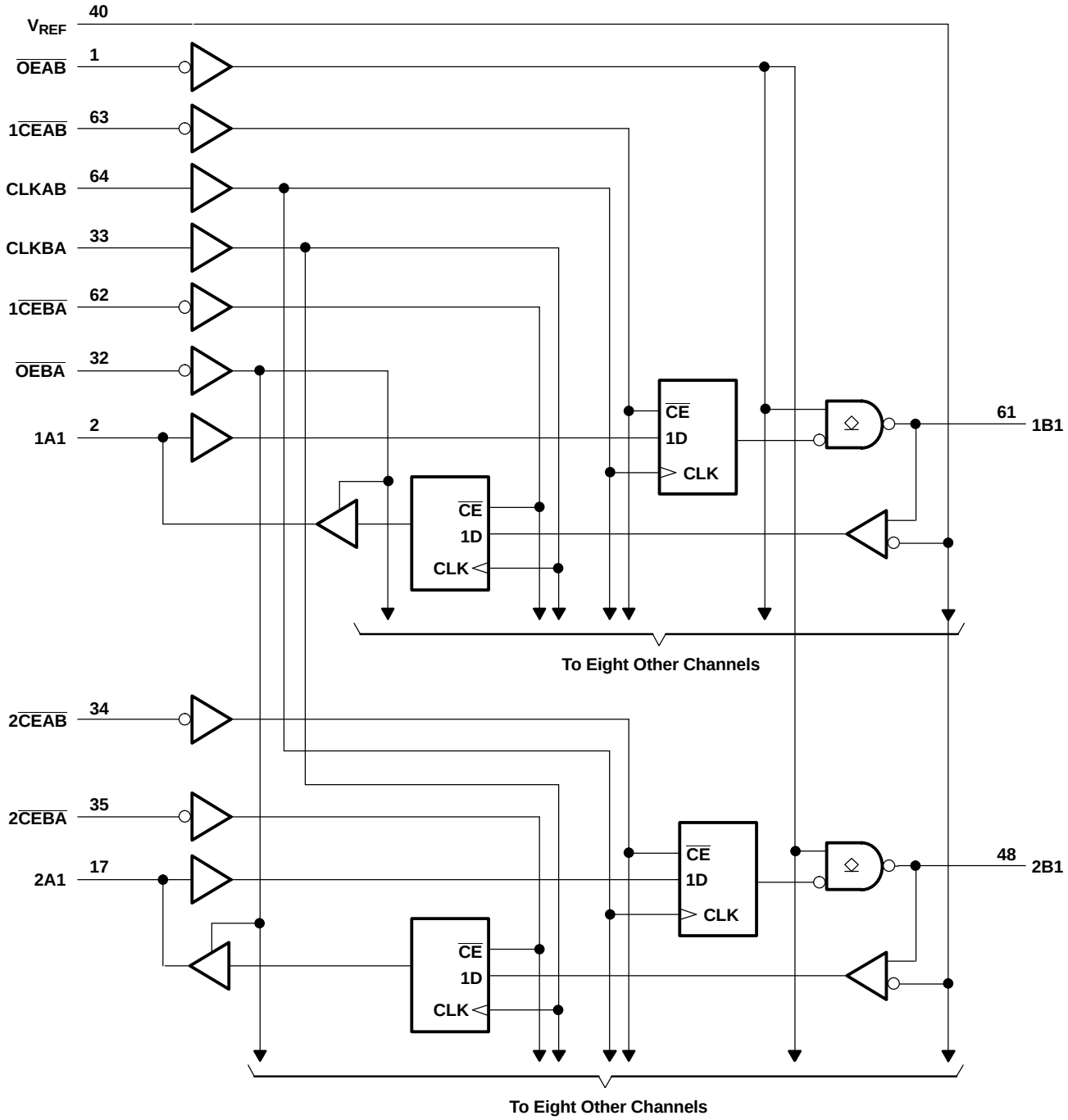
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE(1)

INPUTS				OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	CLKAB	A		
X	H	X	X	Z	Isolation
H	L	X	X	B_0(2)	Latched storage of A data
X	L	H or L	X	B_0(2)	
L	L	↑	L	L	Clocked storage of A data
L	L	↑	H	H	

(1) A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{OEBA}$, CLKBA, and $\overline{CEBA}$.
(2) Output level before the indicated steady-state input conditions are established

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)	A-port and control inputs	–0.5	6.5	V
		B port and V_{REF}	–0.5	4.6	
V_O	Voltage range applied to any output in the high or power-off state(2)	A port	–0.5	6.5	V
		B port	–0.5	4.6	
I_O	Current into any output in the low state	A port		48	mA
		B port		100	
I_O	Current into any A-port output in the high state(3)			48	mA
	Continuous current through each V_{CC} or GND			±100	mA
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
θ_{JA}	Package thermal impedance(4)			55	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The current flows only when the output is in the high state and $V_O > V_{CC}$.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)(2)(3)(4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port			5.5	
V_{IH}	High-level input voltage	B port	V_{REF} + 50 mV			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF} – 50 mV	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			50	
T_A	Operating free-air temperature		–40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) Normal connection sequence is GND first and V_{CC} = 3.3 V, I/O, control inputs, V_{TT} and V_{REF} (any order) last.
(3) V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
(4) V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}.

Electrical Characteristics

over recommended operating free-air temperature range for GTL/GTL+ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC} – 0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	
		V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 40 mA			0.4	
			I_{OL} = 50 mA			0.55	
I_I	B port	V_{CC} = 3.45 V,	V_I = V_{TT} or GND			±5	µA
	A-port and control inputs	V_{CC} = 3.45 V	V_I = V_{CC} or GND			±5	
			V_I = 5.5 V or GND			±20	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 5.5 V			100	µA
$I_{I(hold)}$	A port	V_{CC} = 3.15 V	V_I = 0.8 V	75			µA
			V_I = 2 V	–75			
		V_{CC} = 3.45 V(2),	V_I = 0.8 V to 2 V			±500	
I_{OZ}(3)	A port	V_{CC} = 3.45 V,	V_O = V_{CC} or GND			±10	µA
I_{OZH}	B port	V_{CC} = 3.45 V,	V_O = 1.5 V			10	µA
I_{CC}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			60	mA
			Outputs low			60	
			Outputs disabled			60	
ΔI_{CC}(4)		V_{CC} = 3.45 V, A-port or control inputs at V_{CC} or GND, One input at V_{CC} – 0.6 V				500	µA
C_i	Control inputs	V_I = 3.15 V or 0			2.5	3	pF
C_{io}	A port	V_O = 3.15 V or 0			6	8	pF
	B port				6.5	8.5	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature for GTL (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency			200	MHz
t_w	Pulse duration, CLK high or low		2.5		ns
t_{su}	Setup time	Data before CLK↑	2.1		ns
		$\overline{CE}$ before CLK↑	3.3		
t_h	Hold time	Data after CLK↑	0.3		ns
		$\overline{CE}$ after CLK↑	0		

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature for GTL (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
f_{max}			200			MHz
t_{PLH}	CLKAB	B	2.5		5.5	ns
t_{PHL}			2.2		5.5	
t_{dis}	$\overline{OEAB}$	B	1.7		4.8	ns
t_{en}			2.2		5.2	
Slew rate	Both transitions (B port)			0.5		V/ns
t_r	Transition time, B outputs (0.6 V to 1 V)		0.6		2.2	ns
t_f	Transition time, B outputs (1 V to 0.6 V)		0.4		1.5	ns
t_{PLH}	CLKBA	A	2.1		5.3	ns
t_{PHL}			2.1		5	
t_{en}	$\overline{OEBA}$	A	1.7		5	ns
t_{dis}			2.3		5.5	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature for GTL+ (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency			200	MHz
t_w	Pulse duration, CLK high or low		2.5		ns
t_{su}	Setup time	Data before CLK↑	2.4		ns
		$\overline{CE}$ before CLK↑	3.2		
t_h	Hold time	Data after CLK↑	0.2		ns
		$\overline{CE}$ after CLK↑	0		

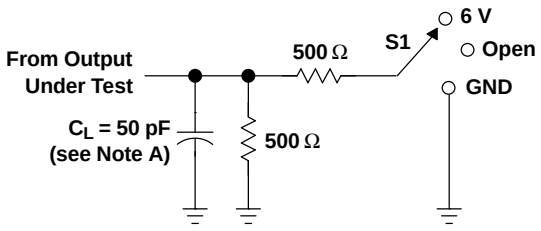
Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature for GTL+ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
f_{max}			200			MHz
t_{PLH}	CLKAB	B	2.6	4	5.6	ns
t_{PHL}			2.3	4	5.7	
t_{PLH}	$\overline{OEAB}$	B	2.4	3.8	5.2	ns
t_{PHL}			1.8	3.4	5	
Slew rate	Both transitions (B port)			0.5		V/ns
t_r	Transition time, B outputs (0.6 V to 1.3 V)		1	1.6	2.7	ns
t_f	Transition time, B outputs (1.3 V to 0.6 V)		0.5	1.1	3.2	ns
t_{PLH}	CLKBA	A	2	3.8	5.3	ns
t_{PHL}			1.9	3.6	5	
t_{en}	$\overline{OEBA}$	A	1.9	3.6	5	ns
t_{dis}			2.1	4	5.5	

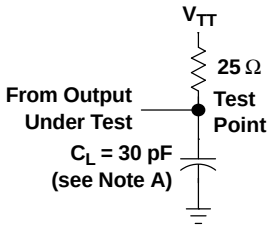
(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

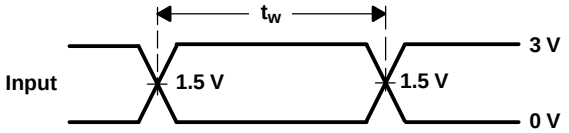


LOAD CIRCUIT FOR A OUTPUTS

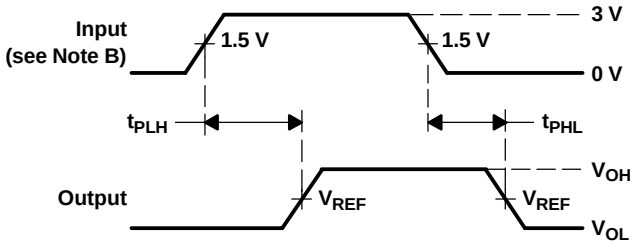
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



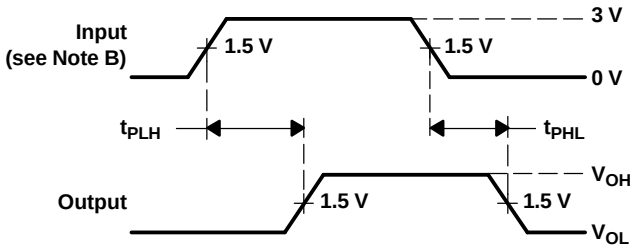
LOAD CIRCUIT FOR B OUTPUTS



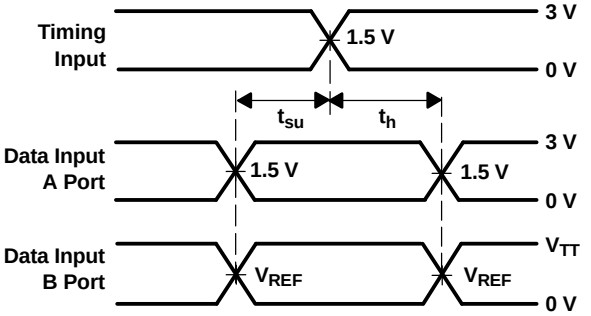
VOLTAGE WAVEFORMS
PULSE DURATION



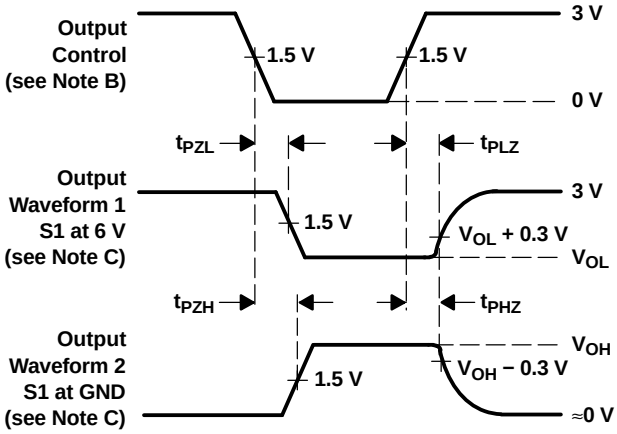
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(CLKAB to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(CLKBA to A port)



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
($\overline{OEBA}$ to A port)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74GTL16622ADGGRE4	ACTIVE	TSSOP	DGG	64		TBD	Call TI	Call TI	-40 to 85		Samples
74GTL16622ADGGRG4	ACTIVE	TSSOP	DGG	64		TBD	Call TI	Call TI	-40 to 85		Samples
SN74GTL16622ADGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTL16622A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

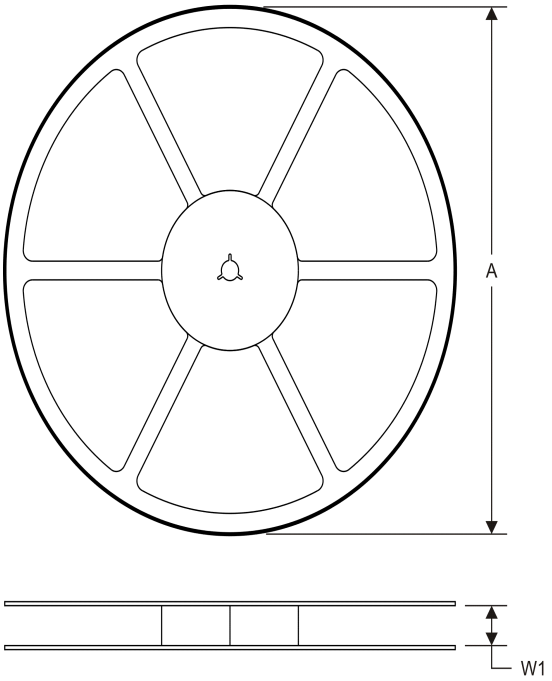
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

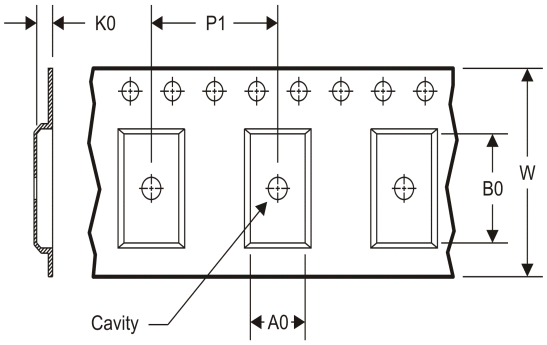
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



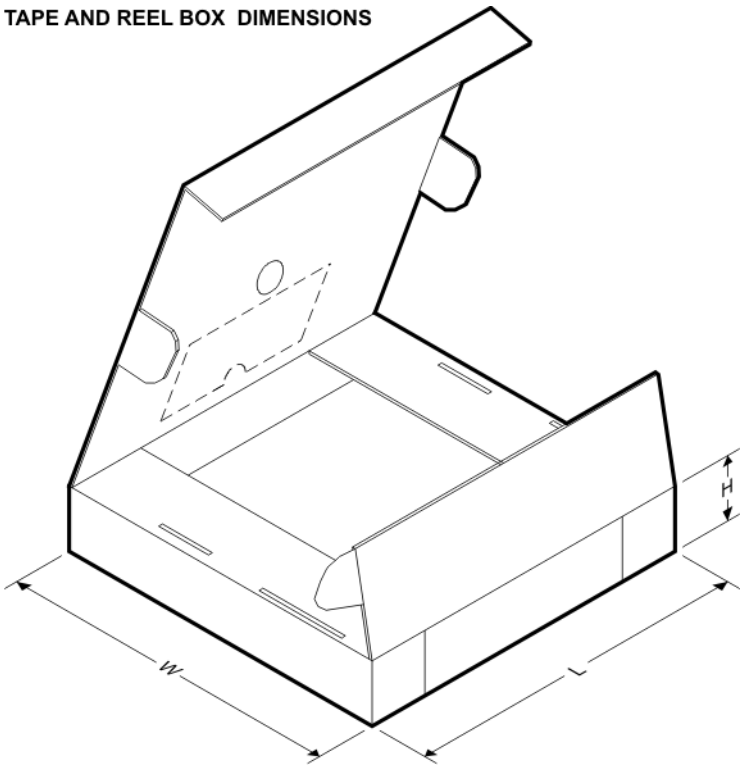
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTL16622ADGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

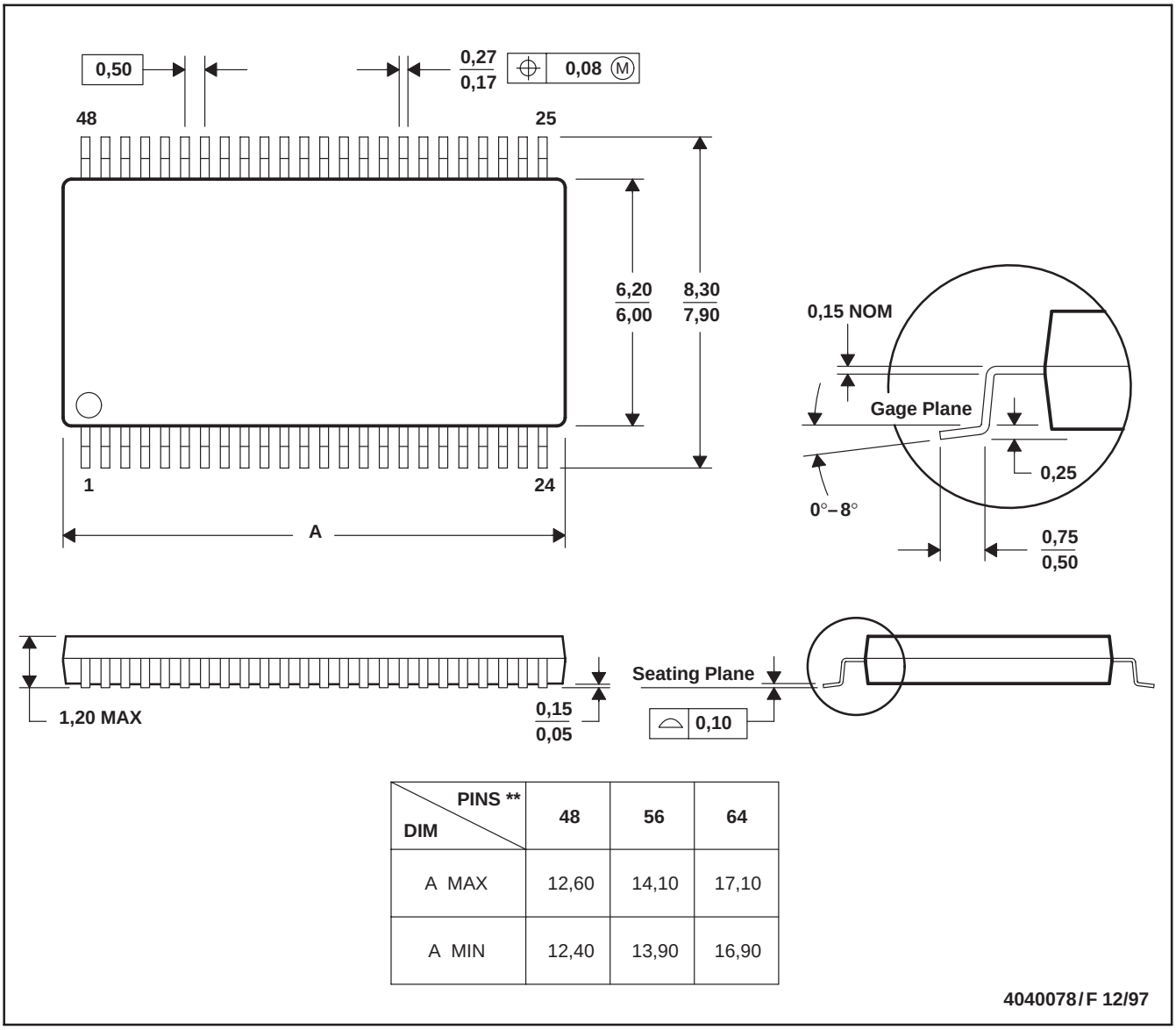


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTL16622ADGGR	TSSOP	DGG	64	2000	367.0	367.0	45.0

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2014, Texas Instruments Incorporated

Unikeyic Electronics

Global Electronic Components Distributor

Click to view pricing, inventory, delivery, and lifecycle information:

Texas Instruments:

ADS8344E ISO124U/1K MSP430F5172IRSBT TPS51125ARGER TPA6203A1DRBR UCC27210DR OPA643P TCAN332DR CC2520RHDR LMV358MMX/NOPB MSP430F2112TRHBT MSP430F47127IPZ MSP430G2332IN20 TPS92200D2DDCR BQ24314DSGR OPA2541BM SN74GTL2006PWR TLV990-28PFB SN75LV4735DBLE TPS71710DCKR MSP430F2001TRSAT MSP430G2403IPW28 OPT3101RHFR PCM56U SN74LVCZ240APW UA9637ACPS TPS7A8018DRBR DS90C383MTDX/NOPB MSP430F5131IDA TLC085CDR