

钍地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65HVD1040AQDRQ1

EMC-Optimized High-Speed CAN Transceiver

网址 www.sztdbdt.com

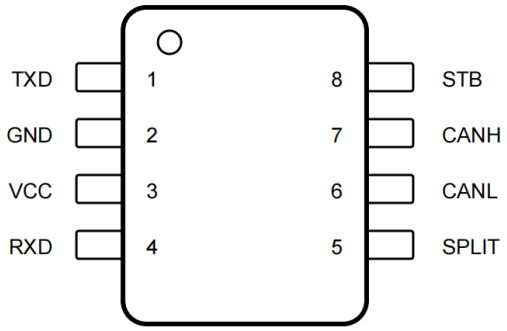
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

● Qualified for Automotive Applications
●AEC-Q100 Test Guidance With the Following:
– Device Temperature Grade 0: –40 ° C to +150 ° C Ambient Operating Temperature
– Device HBM ESD Classification Level:
– 3A Level for All Pins Except 5, 6, and 7
– 3B Level for Pins 5, 6 and 7
– Device CDM ESD Classification Level C6
– Device MM ESD Classification Level M3
● Improved Drop-In Replacement for TJA1040
● Meets or Exceeds the Requirements of ISO 11898-5
●GIFT/ICT Compliant
● ESD Protection up to ±12 kV (Human-Body Model) on Bus Pins
● Low-Current Standby Mode With Bus Wake-Up, <12 μA Maximum
● High Electromagnetic Compliance (EMC)
●Bus-Fault Protection of –27 V to 40 V
● Dominant Time-Out Function
●Thermal Shutdown Protection
● SPLIT Voltage Source for Common-Mode Stabilization of Bus Through Split Termination
● Digital Inputs Compatible With 3.3-V and 5-V Microprocessors.
● Power-Up and Power-Down Glitch-Free Bus Inputs and Outputs
– High Input Impedance With Low VCC
– Monotonic Outputs During Power Cycling



D Package 8-Pin SOIC
Top View

Applications

●GMW3122 Dual-Wire CAN Physical Layers
●SAE J2284 High-Speed CAN for Automotive Applications
● SAE J1939 Standard Data Bus Interface
● ISO 11783 Standard Data Bus Interface
●NMEA 2000 Standard Data Bus Interface

Description

Designed for operation in especially harsh environments, the SN65HVD1040A-Q1 features cross-wire, overvoltage, and loss of ground protection from –27 V to 40 V, overtemperature protection, a –12-V to 12-V common-mode range, and can withstand voltage transients according to ISO 7637.

STB (pin 8) provides two different modes of operation: high-speed mode or low-current standby mode. The high?speed mode of operation is selected by connecting STB (pin 8) to ground.

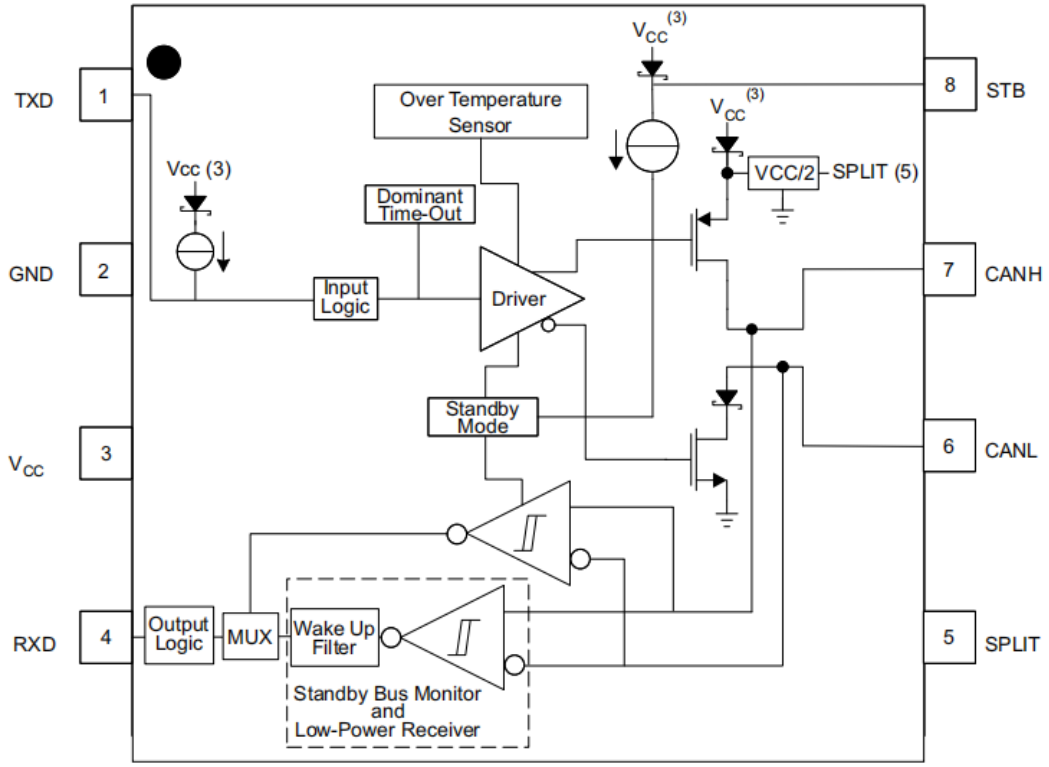
If a high logic level is applied to the STB pin of the SN65HVD1040A-Q1, the device enters a low-current standby mode, while the receiver remains active in a low-power bus-monitor standby mode.

In the low-current standby mode, a dominant bit greater than 5 µs on the bus is passed by the bus-monitor circuit to the receiver output. The local protocol controller may then reactivate the device when it needs to transmit to the bus.

A dominant time-out circuit in the SN65HVD1040A-Q1 prevents the driver from blocking network communication with a hardware or software failure. The time-out circuit is triggered by a falling edge on TXD (pin 1). If no rising edge is seen before the time-out constant of the circuit expires, the driver is disabled. The circuit is then reset by the next rising edge on TXD.

SPLIT (pin 5) is available as a $V_{CC}/2$ common-mode bus voltage bias for a split-termination network (see Application and Implementation).

Functional Block Diagram



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	TXD	I	CAN transmit data input (low for dominant bus state, high for recessive bus state)
2	GND	GND	Ground connection
3	V_{CC}	Supply	Transceiver 5-V supply voltage input
4	RXD	O	CAN receive data output (low in dominant bus state, high in recessive bus state)
5	SPLIT	O	Common-mode stabilization output
6	CANL	I/O	Low-level CAN bus line
7	CANH	I/O	High-level CAN bus line
8	STB	I	Standby mode select pin (active high)
—	NC	NC	No connect

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
	Voltage at bus terminals (CANH, CANL, SPLIT)	–27	40	V
I_O	Receiver output current		20	mA
V_I	Voltage input, ISO 7637 transient pulse(3) (CANH, CANL)	–150	100	V
V_I	Voltage input (TXD, STB)	–0.3	6	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with ISO 7637 test pulses 1, 2, 3a, 3b per IBEE system level test (Pulse 1 = –100 V, Pulse 2 = 100 V, Pulse 3a = –150 V, Pulse 3b = 100 V). If dc may be coupled with AC transients, externally protect the bus pins within the absolute maximum voltage range at any bus terminal. This device has been tested with DC bus shorts to +40 V with leading common-mode chokes. If common-mode chokes are used in the system and the bus lines may be shorted to DC, ensure that the choke type and value in combination with the node termination and shorting voltage either does not create inductive flyback outside of voltage maximum specification or use an external transient-suppression circuit to protect the transceiver from the inductive transients.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	All pins except 5, 6, and 7	±4000	V
			Pins 6 and 7(2)	±12000	
			Pin 5(3)	±10000	
		Charged-device model (CDM), per AEC Q100-011		±1500	
		Machine model (MM)(4)		±200	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) Test method based upon JEDEC Standard 22 Test Method A114F and AEC-Q100-002, CANH and CANL bus pins stressed with respect to each other and GND.
(3) Test method based upon JEDEC Standard 22 Test Method A114F and AEC-Q100-002, SPLIT pin stressed with respect to GND.
(4) Tested in accordance JEDEC Standard 22 Test Method A115A and AEC-Q100-003.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–12	12	V
V_{IH}	High-level input voltage	TXD, STB	2	5.25	V
V_{IL}	Low-level input voltage	TXD, STB	0	0.8	V
V_{ID}	Differential input voltage		–6	6	V
I_{OH}	High-level output current	Driver	–70		mA
		Receiver (RXD)	–2		
I_{OL}	Low-level output current	Driver		70	mA
		Receiver (RXD)		2	
T_A	Operating free-air temperature range	See *Thermal Information*	–40	125	°C
T_J	Junction temperature		–40	150	°C

7.4 Thermal Information

THERMAL METRIC(1)			SN65HVD1040A-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K thermal resistance(2)	140	°C/W
		High-K thermal resistance(3)	112	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		56	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		50	°C/W
ψ_{JT}	Junction-to-top characterization parameter		13	°C/W
ψ_{JB}	Junction-to-board characterization parameter		55	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		—	°C/W

(1) For more information about traditional and new thermal metrics, see the application report, *Semiconductor and IC Package Thermal Metrics*.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, Low-K board, as specified in JESD51-3, in an environment described in JESD51-2a.
(3) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

7.5 Electrical Characteristics

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
SUPPLY							
I_{CC}	5-V supply current	Standby mode	STB at V_{CC}, V_I = V_{CC}		6	12	µA
		Dominant	V_I = 0 V, 60-Ω load, STB at 0 V		50	70	mA
		Recessive	V_I = V_{CC}, No load, STB at 0 V		6	10	mA
UV_{VCC}	Undervoltage reset threshold			2.8		4	V
DRIVER							
$V_{O(D)}$	Bus output voltage (dominant)	CANH	V_I = 0 V, STB at 0 V, R_L = 60 Ω, See Figure 3 and Figure 15	2.9	3.4	4.5	V
		CANL		0.8		1.75	V
$V_{O(R)}$	Bus output voltage (recessive)		V_I = 3 V, STB at 0 V, R_L = 60 Ω, See Figure 3 and Figure 15	2	2.5	3	V
V_O	Bus output voltage (standby mode)		STB at Vcc, R_L = 60 Ω, See Figure 3 and Figure 15	–0.1		0.1	V
$V_{OD(D)}$	Differential output voltage (dominant)		V_I = 0 V, R_L = 60 Ω, STB at 0 V, See Figure 3, Figure 15, and Figure 4	1.5		3	V
			V_I = 0 V, R_L = 45 Ω, STB at 0 V, See Figure 3, Figure 15, and Figure 4	1.4		3	V
$V_{OD(R)}$	Differential output voltage (recessive)		V_I = 3 V, STB at 0 V, R_L = 60 Ω, See Figure 3 and Figure 15	–0.012		0.012	V
			V_I = 3 V, STB at 0 V, No load	–0.5		0.05	V
V_{SYM}	Output symmetry (dominant or recessive) ($V_{O(CANH)}$ + $V_{O(CANL)}$)		STB at 0 V, R_L = 60 Ω, See Figure 14	0.9 V_{CC}	V_{CC}	1.1 V_{CC}	V
$V_{OC(ss)}$	Steady-state common-mode output voltage		STB at 0 V, R_L = 60 Ω, See Figure 9	2	2.5	3	V
$\Delta V_{OC(ss)}$	Change in steady-state common-mode output voltage		STB at 0 V, R_L = 60 Ω, See Figure 9		30		mV
V_{IH}	High-level input voltage, TXD input			2			V
V_{IL}	Low-level input voltage, TXD input					0.8	V
I_{IH}	High-level input current, TXD input		V_I at V_{CC}	–2		2	µA
I_{IL}	Low-level input current, TXD input		V_I at 0 V	–50		–10	µA
$I_{O(off)}$	Power-off TXD output current		V_{CC} at 0 V, TXD at 5 V			1	µA

Electrical Characteristics (continued)

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$I_{OS(ss)}$	Short-circuit steady-state output current, Dominant	V_{CANH} = –12 V, CANL open, TXD = low, See Figure 12	–120	–85		mA
		V_{CANH} = 12 V, CANL open, TXD = low, See Figure 12		0.4	1	
		V_{CANL} = –12 V, CANH open, TXD = low, See Figure 12	–1	–0.6		
		V_{CANL} = 12 V, CANH open, TXD = low, See Figure 12		75	120	
		V_{CANH} = 0 V, CANL open, TXD = low, See Figure 12	–100	–75		
		V_{CANL} = 32 V, CANH open, , TXD = low, See Figure 12		75	125	
$I_{OS(ss)}$	Short-circuit steady-state output current, Recessive	–20 V ≤ V_{CANH} ≤ 32 V, CANL open, TXD = high, See Figure 12	–10		10	mA
		–20 V ≤ V_{CANL} ≤ 32 V, CANH open, TXD = high, See Figure 12	–10		10	
C_O	Output capacitance	See receiver input capacitance				
RECEIVER						
V_{IT+}	Positive-going input threshold voltage, high-speed mode	STB at 0 V, See Table 1		800	900	mV
$V_{IT–}$	Negative-going input threshold voltage, high-speed mode	STB at 0 V, See Table 1	500	650		mV
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT–}$)		100	125		mV
V_{IT}	Input threshold voltage, standby mode	STB at V_{CC}	500		1150	mV
V_{OH}	High-level output voltage	I_O = –2 mA, See Figure 7	4	4.6		V
V_{OL}	Low-level output voltage	I_O = 2 mA, See Figure 7		0.2	0.4	V
$I_{I(off)}$	Power-off bus input current (unpowered bus leakage current)	CANH = CANL = 5 V, V_{CC} at 0 V, TXD at 0 V			3	µA
$I_{O(off)}$	Power-off RXD leakage current	V_{CC} at 0 V, RXD at 5 V			20	µA
C_I	Input capacitance to ground (CANH or CANL)	TXD at 3 V, V_I = 0.4 sin (4E6πt) + 2.5 V		13		pF
C_{ID}	Differential input capacitance	TXD at 3 V, V_I = 0.4 sin (4E6πt)		6		pF
R_{ID}	Differential input resistance	TXD at 3 V, STB at 0 V	30		80	kΩ
R_{IN}	Input resistance (CANH or CANL)	TXD at 3 V, STB at 0 V	15	30	40	kΩ
$R_{I(m)}$	Input resistance matching [1 – ($R_{IN\ (CANH)}$ / $R_{IN\ (CANL)}$)] × 100%	$V_{(CANH)}$ = $V_{(CANL)}$	–3%	0%	3%	
STB PIN						
V_{IH}	High-level input voltage, STB input		2			V
V_{IL}	Low-level input voltage, STB input				0.8	V
I_{IH}	High-level input current	STB at 2 V	–10		0	µA
I_{IL}	Low-level input current	STB at 0.8 V	–10		0	µA
SPLIT PIN						
V_O	Output voltage	–500 µA < I_O < 500 µA	0.3 × V_{CC}	0.5 × V_{CC}	0.7 × V_{CC}	V
$I_{O(stb)}$	Leakage current, standby mode	STB at 2 V, –12 V ≤ V_O ≤ 12 V	–5		5	µA

7.6 Power Dissipation Characteristics

over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted)

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Average power dissipation	V_{CC} = 5 V, T_J = 27°C, R_L = 60 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF		112		mW
		V_{CC} = 5.5 V, T_J = 130°C, R_L = 45 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF			170	

Power Dissipation Characteristics (continued)

over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted)

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal shutdown temperature			185		°C

7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE SWITCHING CHARACTERISTICS						
$t_{d(LOOP1)}$	Total loop delay, driver input to receiver output, recessive to dominant	STB at 0 V, see Figure 10	90		230	ns
$t_{d(LOOP2)}$	Total loop delay, driver input to receiver output, dominant to recessive	STB at 0 V, see Figure 10	90		230	ns
DRIVER SWITCHING CHARACTERISTICS						
t_{PLH}	Propagation delay time, low-to-high level output	STB at 0 V, see Figure 5	25	65	120	ns
t_{PHL}	Propagation delay time, high-to-low level output	STB at 0 V, see Figure 5	25	45	120	ns
t_r	Differential output signal rise time	STB at 0 V, see Figure 5		25		ns
t_f	Differential output signal fall time	STB at 0 V, see Figure 5		45		ns
t_{en}	Enable time from standby mode to normal mode and transmission of dominant	See Figure 8			10	µs
$t_{(dom)}$	Dominant time-out (1)	↓V_I, see Figure 11	300	450	700	µs
RECEIVER SWITCHING CHARACTERISTICS						
t_{PLH}	Propagation delay time, low-to-high-level output	STB at 0 V , see Figure 7	60	90	130	ns
t_{PHL}	Propagation delay time, high-to-low-level output	STB at 0 V , see Figure 7	45	70	130	ns
t_r	Output signal rise time	STB at 0 V , see Figure 7		8		ns
t_f	Output signal fall time	STB at 0 V , see Figure 7		8		ns
t_{BUS}	Dominant time required on bus for wakeup from standby	STB at V_{CC}, see Figure 13	1.5		5	µs

(1) The TXD dominant time-out ($t_{(dom)}$) disables the driver of the transceiver once the TXD has been dominant longer than $t_{(dom)}$, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where 5 successive dominant bits are followed immediately by an error frame. This, along with the $t_{(dom)}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by:
Minimum Bit Rate = 11/ $t_{(dom)}$ = 11 bits / 300 µs = 37 kbps

8 Parameter Measurement Information

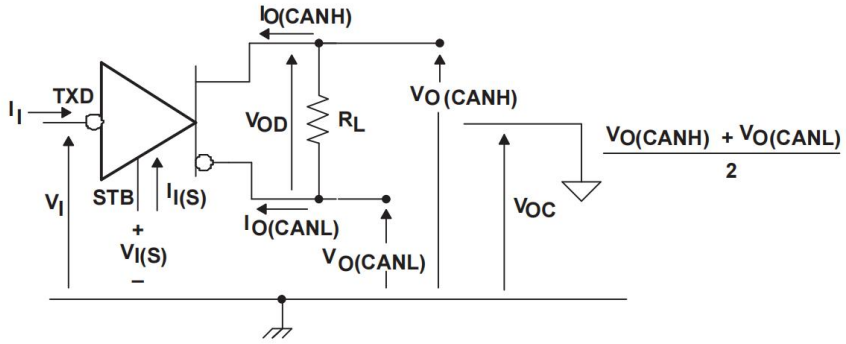


Figure 3. Driver Voltage, Current, and Test Definition

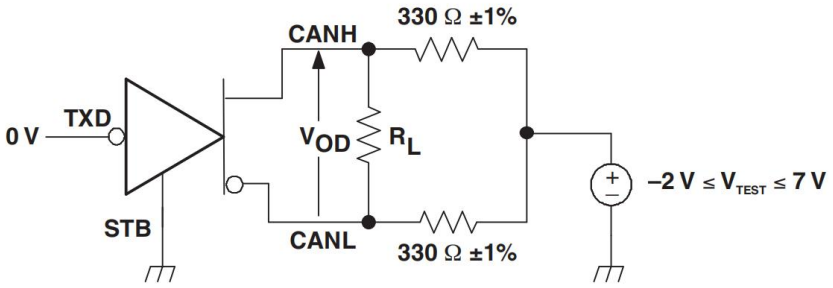


Figure 4. Driver V_{OD} Test Circuit

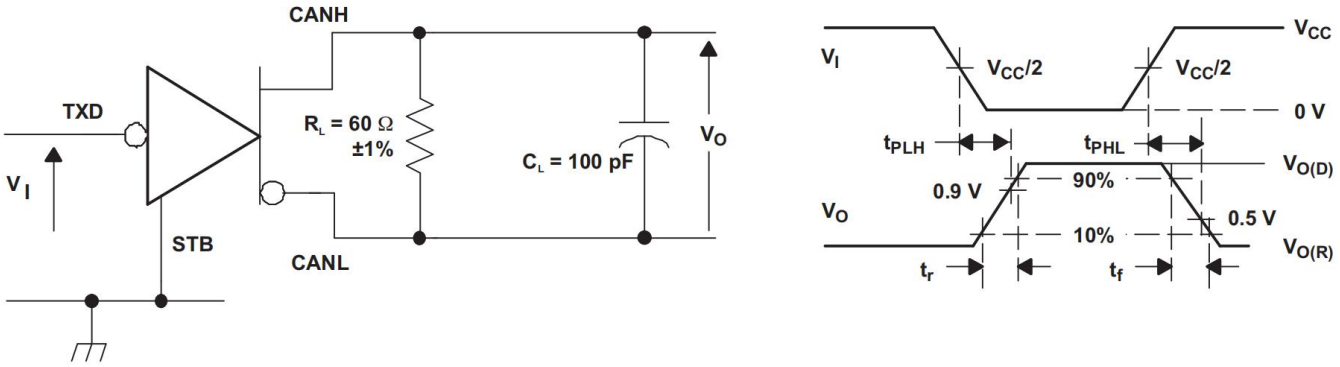


Figure 5. Driver Test Circuit and Voltage Waveforms

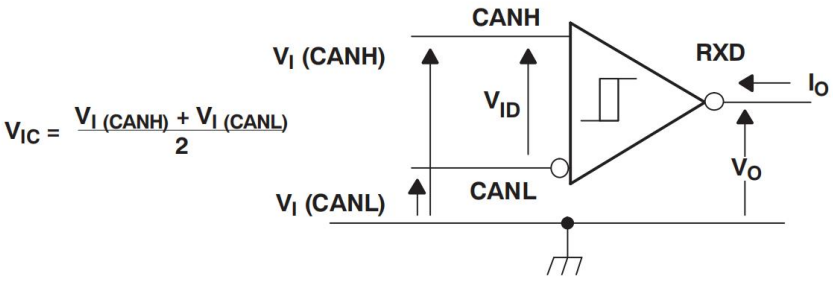
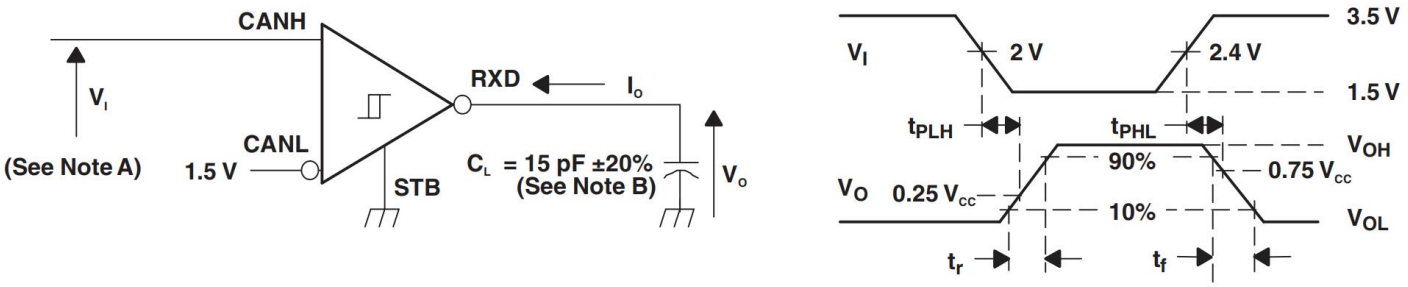


Figure 6. Receiver Voltage and Current Definitions

Parameter Measurement Information (continued)



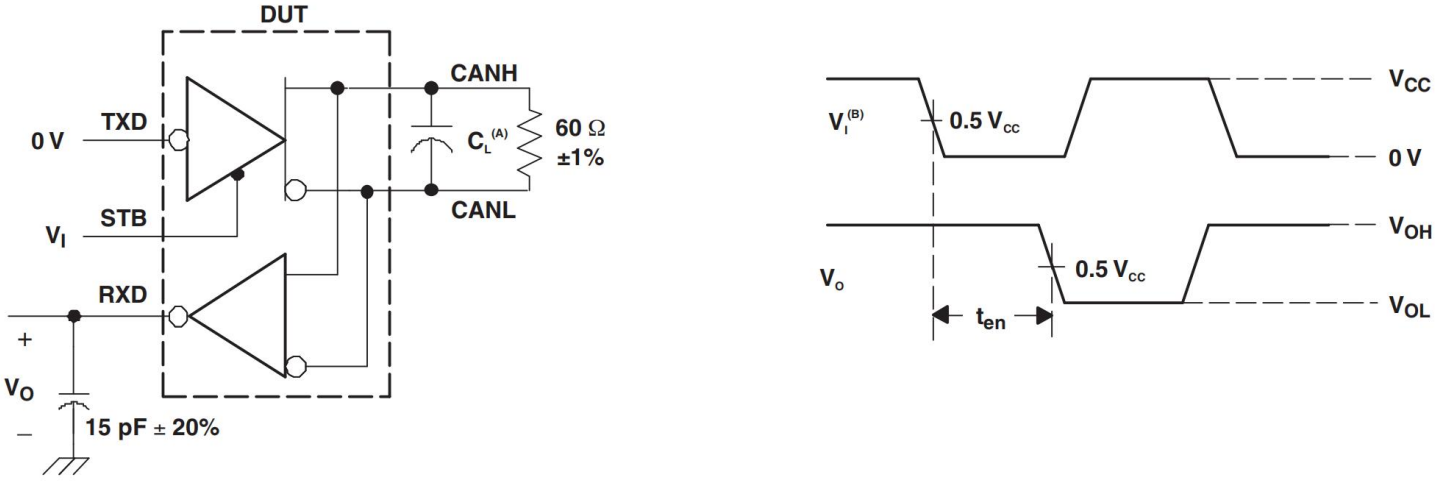
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 7. Receiver Test Circuit and Voltage Waveforms

Table 1. Differential Input Voltage Threshold Test

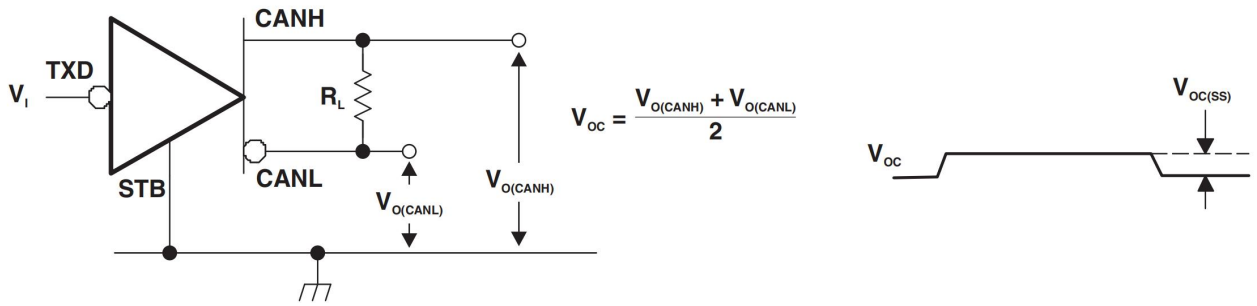
INPUT			OUTPUT R	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$		
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	



A. C_L = 100 pF and includes instrumentation and fixture capacitance within ±20%.

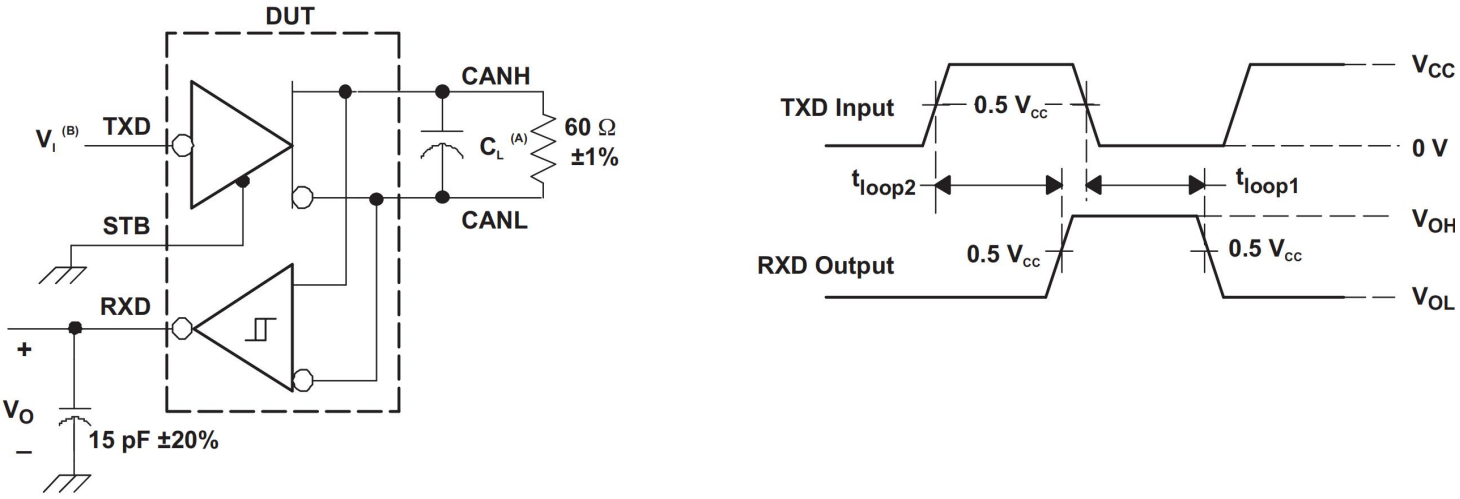
B. All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 8. t_{en} Test Circuit and Waveforms



NOTE: All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

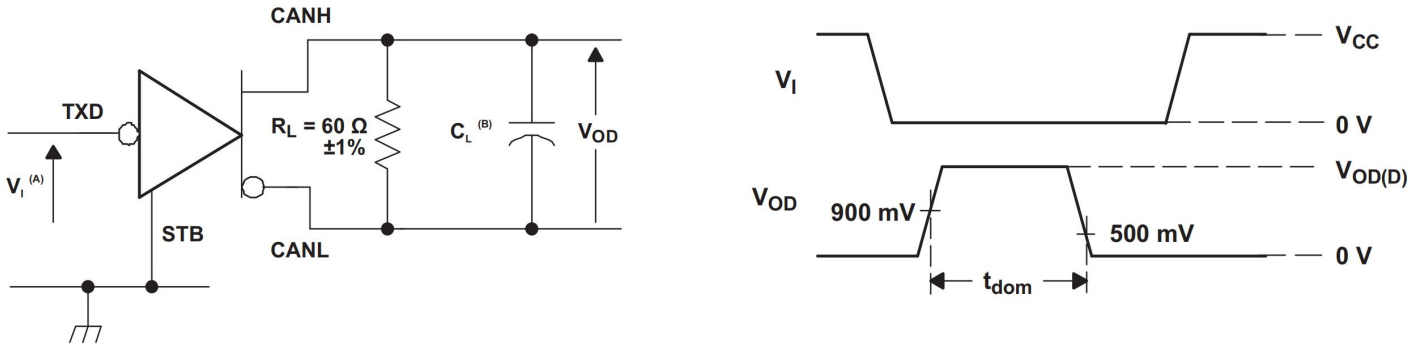
Figure 9. Common-Mode Output Voltage Test and Waveforms



A. C_L = 100 pF and includes instrumentation and fixture capacitance within ±20%.

B. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 10. $t_{(LOOP)}$ Test Circuit and Waveforms



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 500 Hz, 50% duty cycle.

B. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

Figure 11. Dominant Time-Out Test Circuit and Waveforms

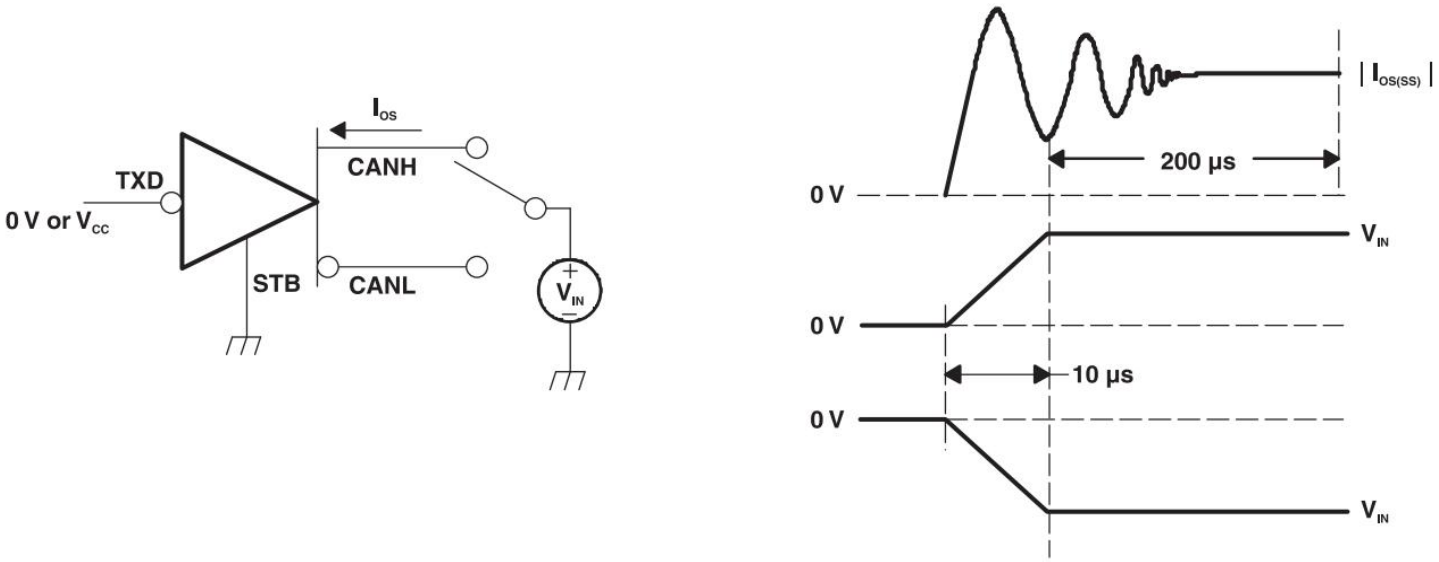
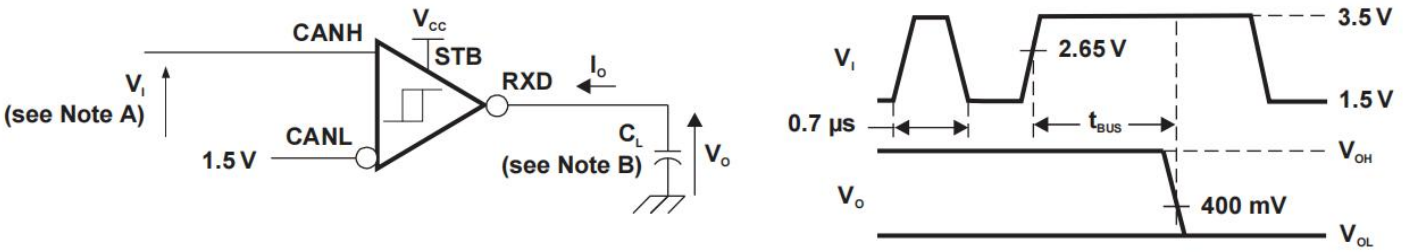


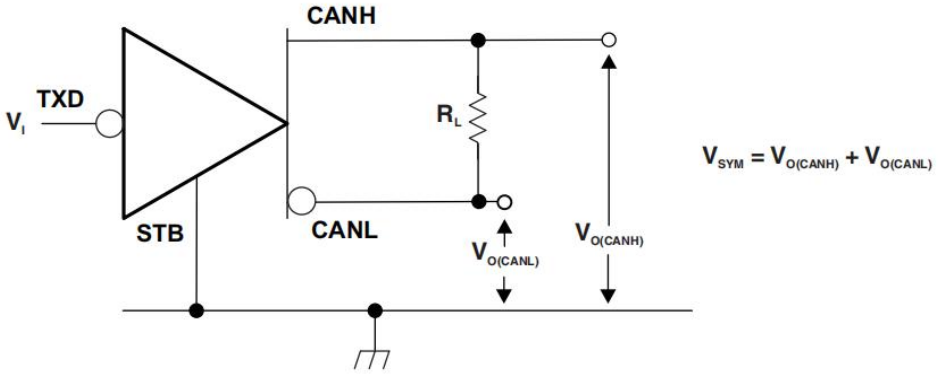
Figure 12. Driver Short-Circuit Current Test and Waveforms



A. For V_I bit width ≤ 0.7 µs, $V_O = V_{OH}$. For V_I bit width ≥ 5 µs, $V_O = V_{OL}$. V_I input pulses are supplied from a generator with the following characteristics: t_r/t_f < 6 ns.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 13. t_{BUS} Test Circuit and Waveforms



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r/t_f ≤ 6 ns, pulse repetition rate (PRR) = 250 kHz, 50% duty cycle.

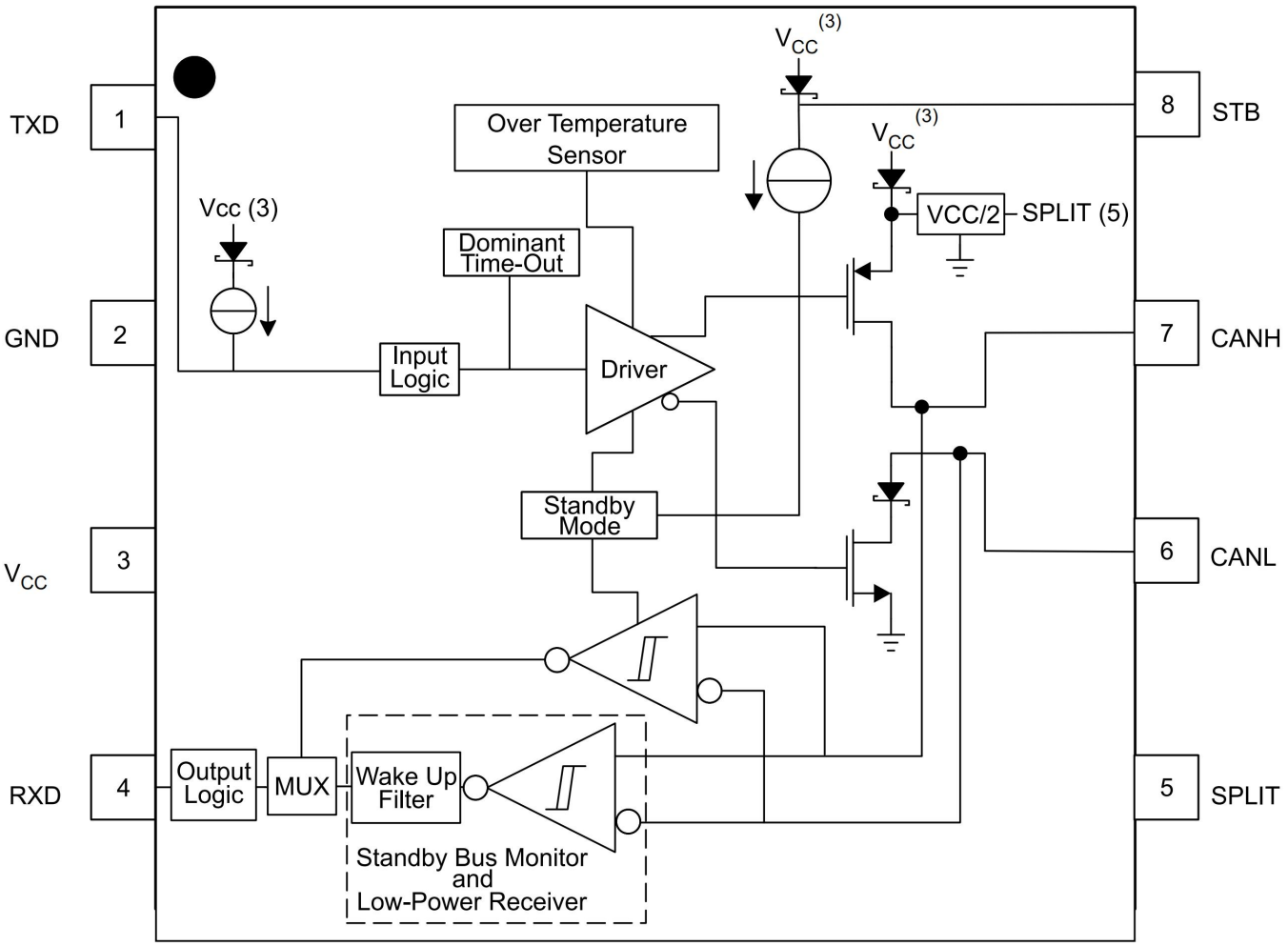
Figure 14. Driver Output Symmetry Test Circuit

9 Detailed Description

9.1 Overview

The SN65HVD1040A-Q1 CAN tranceiver is compatible with the ISO 11898-2 high-speed CAN (Controller Area Network) physical layer standard. The device is designed to interface between the differential bus lines in controller area network and the CAN protocol controller at data rates up to 1 Mbps.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 Operating Modes

The device has two main operating modes: normal mode and standby mode. Operating mode selection is made through the STB input pin.

Table 2. Operating Modes

STB PIN	MODE	DRIVER	RECEIVER	RXD PIN
LOW	NORMAL	Enabled (On)	Enabled (On)	Mirrors CAN bus
HIGH	STANDBY	Disabled (Off)	Low-power wake-up receiver and bus monitor enabled (On)	Low = wake-up request received High = no wake-up request received

9.3.1.1 Bus States by Mode

The CAN bus has three valid states during powered operation depending on the mode of the device. In normal mode the bus may be dominant (logic low) where the bus lines are driven differentially apart or recessive (logic high) where the bus lines are biased to $V_{CC}/2$ through the high-ohmic internal input resistors R_{IN} of the receiver. The third state is low-power standby mode where the bus lines are biased to GND through the high-ohmic internal input resistors R_{IN} of the receiver.

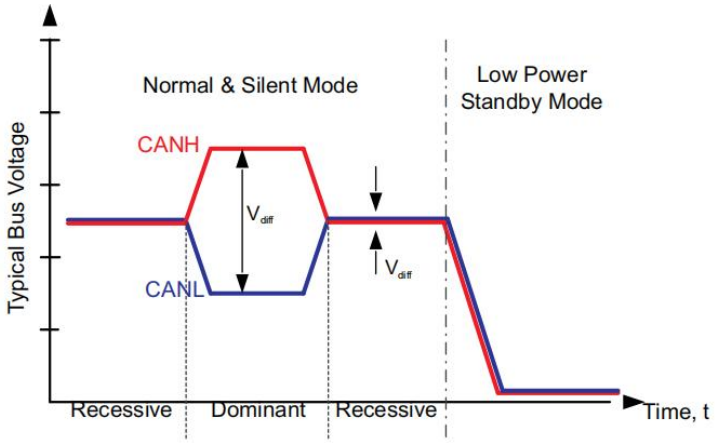


Figure 15. Bus States (Physical Bit Representation)

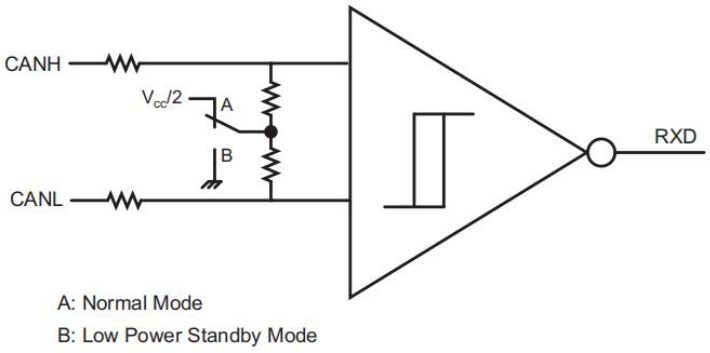


Figure 16. Simplified Common-Mode Bias and Receiver Implementation

9.3.1.2 Normal Mode

This is the normal operating mode of the device. It is selected by setting STB low. The CAN driver and receiver are fully operational and CAN communication is bidirectional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD. In recessive state the bus pins are biased to 0.5 × V_{CC}. In dominant state the bus pins (CANH and CANL) are driven differentially apart. Logic high is equivalent to recessive on the bus and logic low is equivalent to a dominant (differential) signal on the bus.

The SPLIT pin is biased to 0.5 × V_{CC} for bus common-mode bus voltage bias stabilization in split termination network applications (see *Application and Implementation*).

9.3.1.3 Standby Mode and RXD Wake-Up Request

This is the low-power mode of the device. It is selected by setting STB high. The CAN driver and main receiver are turned off and bidirectional CAN communication is not possible. The low-power receiver and bus monitor are enabled to allow for wake-up requests through the bus. A wake-up request will be output to RXD (driven low) for any dominant bus transmissions longer than the filter time t_{BUS}. The local protocol controller (MCU) should monitor RXD for transitions and then reactivate the device to normal mode based on the wake-up request. The CAN bus pins are weakly pulled to GND and the SPLIT pin is off (floating).

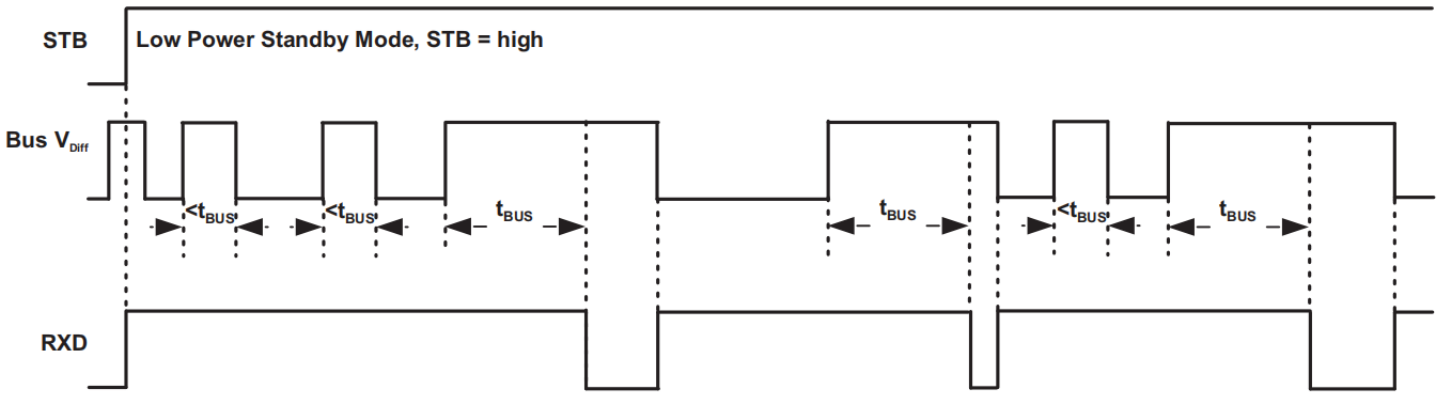


Figure 17. Standby Mode Low-Power Receiver and Bus Monitor Behavior

9.3.2 Protection Features

9.3.2.1 TXD Dominant State Time-Out

During normal mode (the only mode in which the CAN driver is active) the TXD dominant time-out circuit prevents the transceiver from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the time-out period t_{DST}. The dominant time-out circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time-out constant of the circuit expires (t_{DST}), the CAN bus driver is disabled, thus freeing the bus for communication between other network nodes. The CAN driver is re-activated when a recessive signal is seen on the TXD pin, thus clearing the dominant state time-out. The CAN bus pins are biased to recessive level during a TXD dominant state time-out and SPLIT remains on.

9.3.2.2 Thermal Shutdown

If the junction temperature of the device exceeds the thermal shutdown threshold the device turns off the CAN driver circuits, including the SPLIT pin. This condition is cleared when the temperature drops below the thermal shutdown temperature of the device.

9.3.2.3 Undervoltage Lockout and Unpowered Device

The device has undervoltage detection and lockout on the V_{CC} supply. If an undervoltage condition is detected on V_{CC}, the device protects the bus.

The TXD pin is pulled up to V_{CC} to force a recessive input level if the pin floats. The STB is pulled up to V_{CC} to force the device in standby mode (low power) if the pin floats.

The bus pins (CANH, CANL, and SPLIT) all have extremely low leakage currents when the device is unpowered so it does not load down the bus but be an *ideal passive* load to the bus. This is critical, especially if some nodes of the network are unpowered while the rest of the network remains in operation.

9.4 Device Functional Modes

Table 3 and Table 4 lists the functions of this device.

Table 3. Driver Function Table(1)

INPUTS		OUTPUTS		BUS STATE
TXD	STB	CANH	CANL	
L	L	H	L	Dominant
H	L	Z	Z	Recessive
Open	L	Z	Z	Recessive
X	H or Open	Y	Y	Recessive

(1) H = high level, L = low level, X = irrelevant, Y = weak pulldown to GND, ? = indeterminate, Z = high impedance

Table 4. Receiver Function Table

DIFFERENTIAL INPUTS V_{ID} = V(CANH) – V(CANL)	STB	OUTPUT RXD	BUS STATE
$V_{ID} \geq 0.9$ V	L	L	Dominant
$V_{ID} \geq 1.15$ V	H or Open	L	Dominant
0.5 V < V_{ID} < 0.9 V	X	?	?
$V_{ID} \leq 0.5$ V	X	H	Recessive
Open	X	H	Recessive

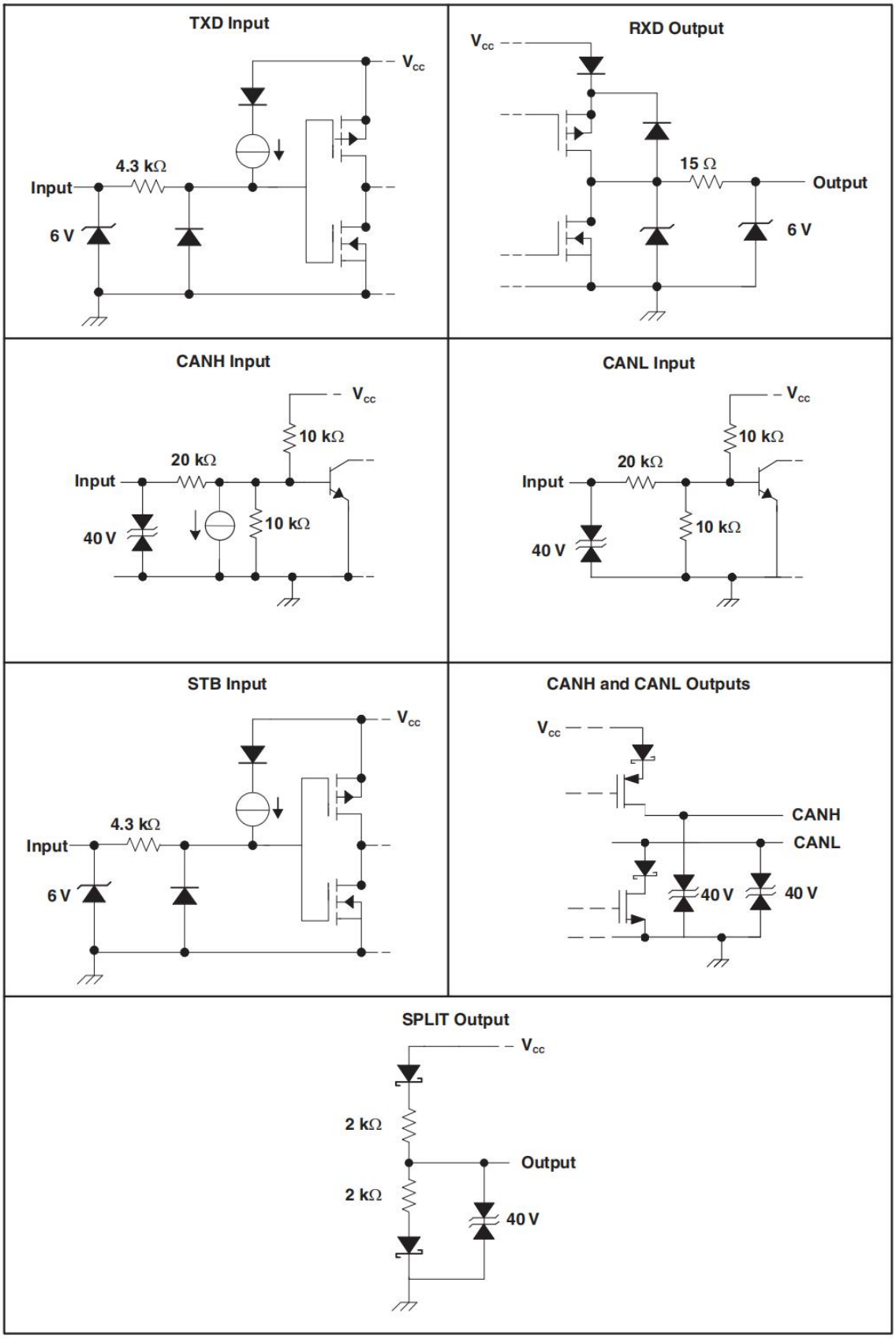
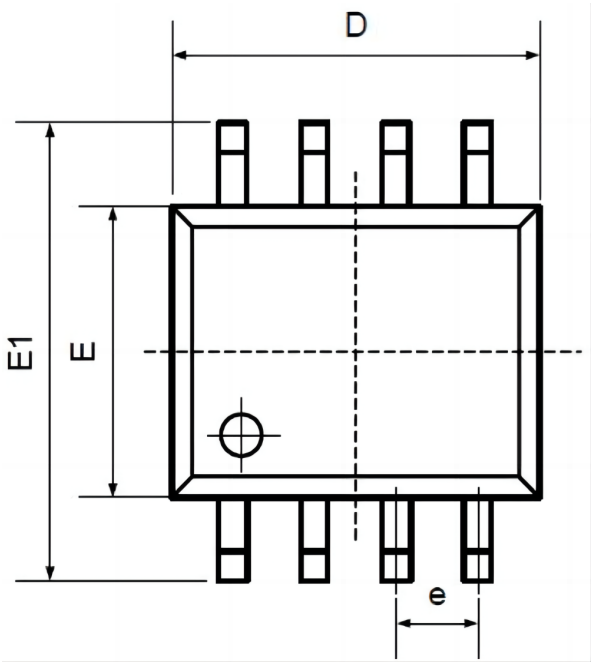


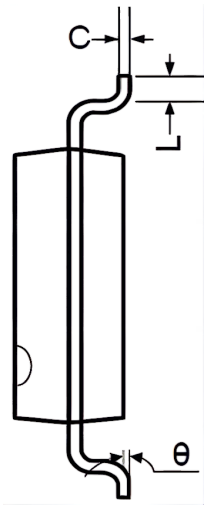
Figure 18. Equivalent Input and Output Schematic Diagrams

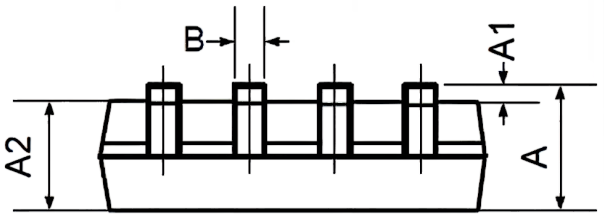
Order information

Order Number	Package	Package Quantity	Marking On The park
SN65HVD1040AQDRQ1-TUDI	SOP8	Tape,Reel,2500	SN65HVD1040AQDRQ1

Package SOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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