MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ C7

600V CoolMOS™ C7 Power Transistor
IPP60R180C7

Data Sheet

Rev. 2.0
Final

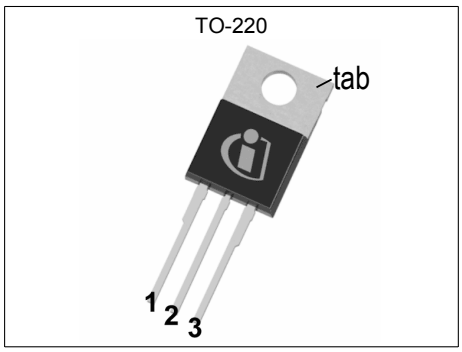
Power Management & Multimarket

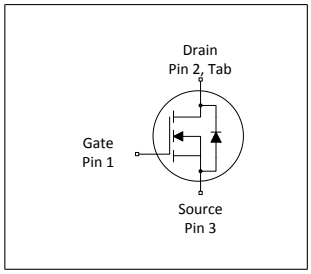
1 Description

CoolMOS™ C7 is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

600V CoolMOS™ C7 series combines the experience of the leading SJ MOSFET supplier with high class innovation.

The 600V C7 is the first technology ever with $R_{DS(on)}$*A below 1Ohm*mm².





Features

- Suitable for hard and soft switching (PFC and high performance LLC)
- Increased MOSFET dv/dt ruggedness to 120V/ns
- Increased efficiency due to best in class FOM $R_{DS(on)}$*E_{oss} and $R_{DS(on)}$*Q_g
- Best in class $R_{DS(on)}$ /package
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

Benefits

- Increased economies of scale by use in PFC and PWM topologies in the application
- Higher dv/dt limit enables faster switching leading to higher efficiency
- Enabling higher system efficiency by lower switching losses
- Increased power density solutions due to smaller packages
- Suitable for applications such as server, telecom and solar
- Higher switching frequencies possible without loss in efficiency due to low Eoss and Qg

Applications

PFC stages and PWM stages (TTF, LLC) for high power/performance SMPS e.g. Computing, Server, Telecom, UPS and Solar.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	180	mΩ
$Q_{g.typ}$	24	nC
$I_{D,pulse}$	45	A
$I_{D,continuous}$ @ T_j<150°C	22	A
E_{oss}@400V	2.7	µJ
Body diode di/dt	350	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPP60R180C7	PG-TO 220	60C7180	see Appendix A

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2 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	13 8	A	T_C=25°C T_C=100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	45	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	53	mJ	I_D=3.3A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.26	mJ	I_D=3.3A; V_{DD}=50V; see table 10
Avalanche current, single pulse	I_{AS}	-	-	3.3	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	68	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55	-	150	°C	-
Mounting torque	-	-	-	60	Ncm	M3 and M3.5 screws
Continuous diode forward current	I_S	-	-	13	A	T_C=25°C
Diode pulse current[2]	$I_{S,pulse}$	-	-	45	A	T_C=25°C
Reverse diode dv/dt[3]	dv/dt	-	-	20	V/ns	V_{DS}=0...400V, I_{SD}<=5.2A, T_j=25°C see table 8
Maximum diode commutation speed	di_f/dt	-	-	350	A/µs	V_{DS}=0...400V, I_{SD}<=5.2A, T_j=25°C see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C=25°C, t=1min

[1] Limited by $T_{j\,max}$.
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.832	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	leaded
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	°C/W	n.a.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

4 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	V_{DS}=V_{GS}, I_D=0.26mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=600, V_{GS}=0V, T_j=25°C V_{DS}=600, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.155 0.346	0.180 -	Ω	V_{GS}=10V, I_D=5.3A, T_j=25°C V_{GS}=10V, I_D=5.3A, T_j=150°C
Gate resistance	R_G	-	0.85	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1080	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}	-	18	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Effective output capacitance, energy related[1)]	$C_{o(er)}$	-	34	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[2)]	$C_{o(tr)}$	-	349	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	9.3	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=5.3A, R_G=10Ω; see table 9
Rise time	t_r	-	7	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=5.3A, R_G=10Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	50	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=5.3A, R_G=10Ω; see table 9
Fall time	t_f	-	6	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=5.3A, R_G=10Ω; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	5	-	nC	V_{DD}=400V, I_D=5.3A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	8	-	nC	V_{DD}=400V, I_D=5.3A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	24	-	nC	V_{DD}=400V, I_D=5.3A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.0	-	V	V_{DD}=400V, I_D=5.3A, V_{GS}=0 to 10V

[1)] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

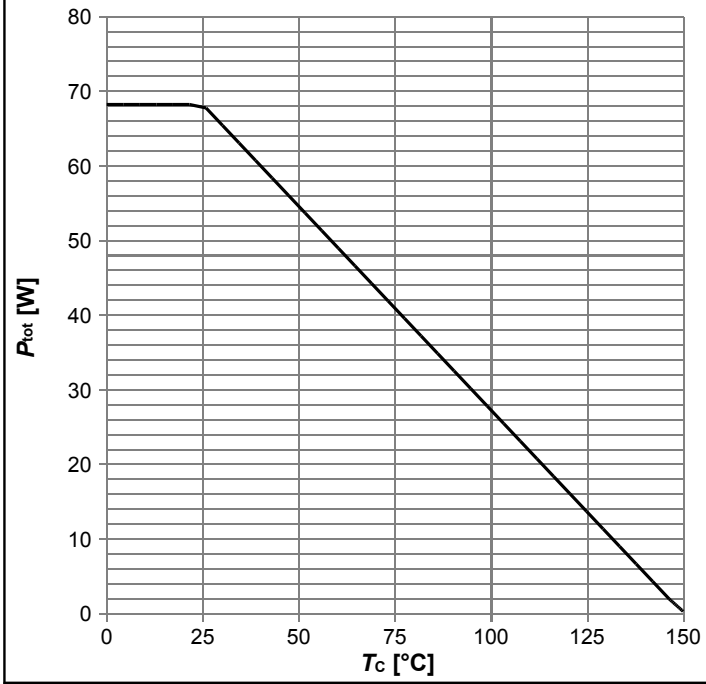
[2)] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=5.3A, T_j=25°C
Reverse recovery time	t_{rr}	-	280	-	ns	V_R=400V, I_F=5.3A, di_F/dt=100A/µs; see table 8
Reverse recovery charge	Q_{rr}	-	2.6	-	µC	V_R=400V, I_F=5.3A, di_F/dt=100A/µs; see table 8
Peak reverse recovery current	I_{rrm}	-	21	-	A	V_R=400V, I_F=5.3A, di_F/dt=100A/µs; see table 8

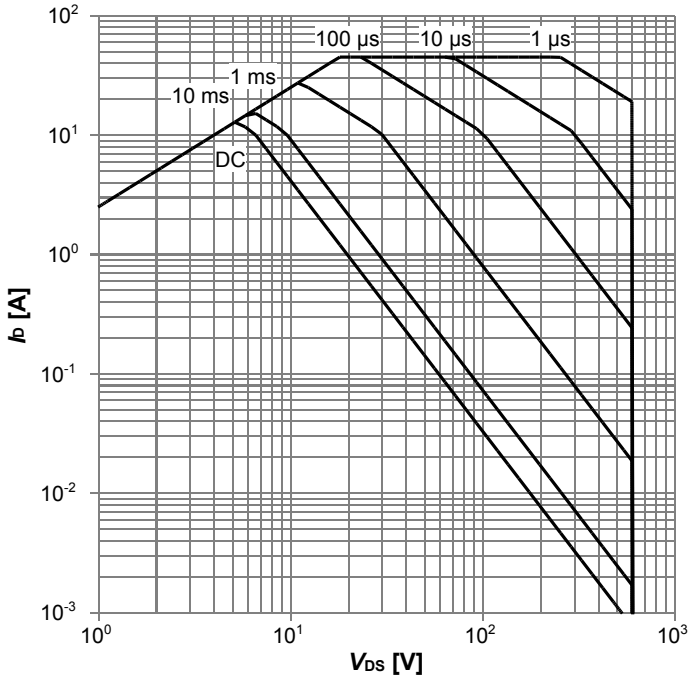
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



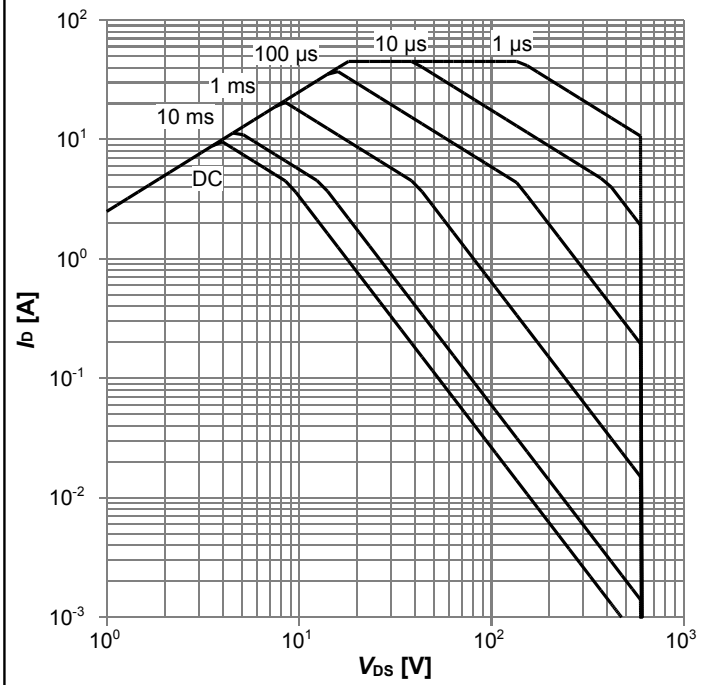
$P_{tot}=f(T_C)$

Diagram 2: Safe operating area



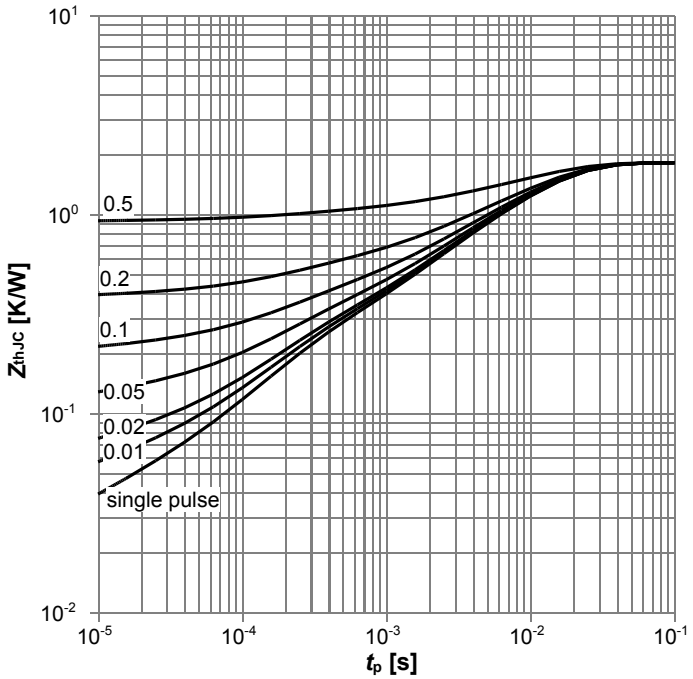
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 3: Safe operating area



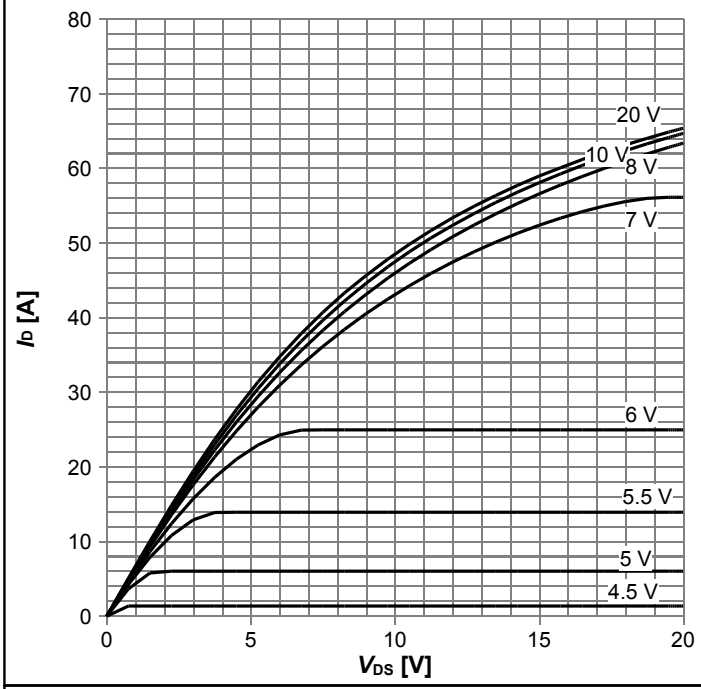
$I_D=f(V_{DS})$; $T_C=80$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



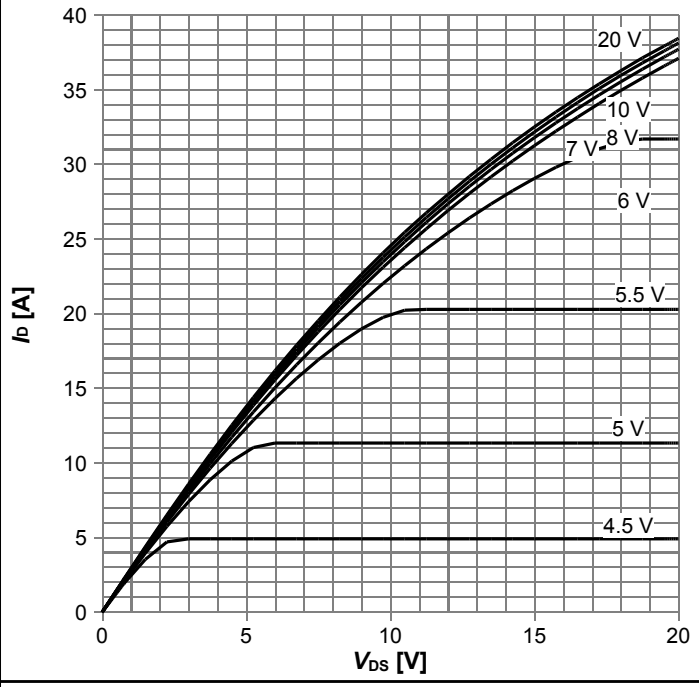
$Z_{thJC}=f(t_P)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



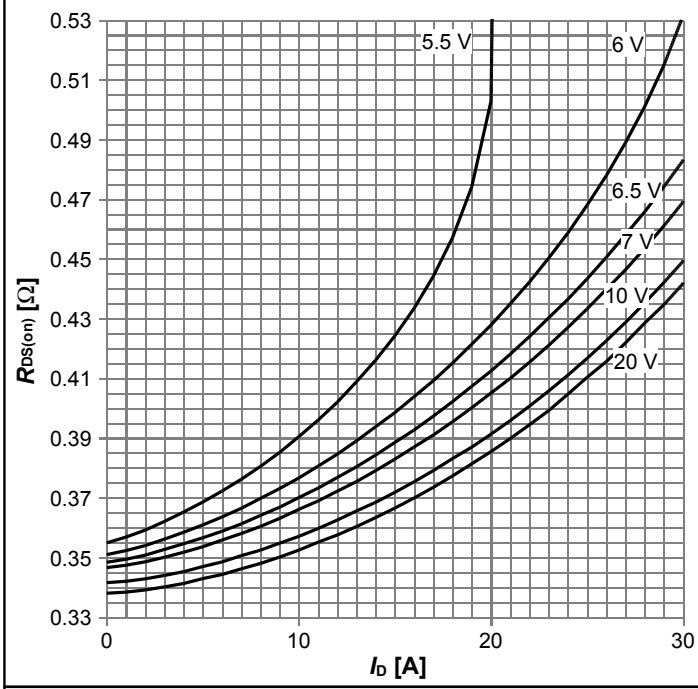
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



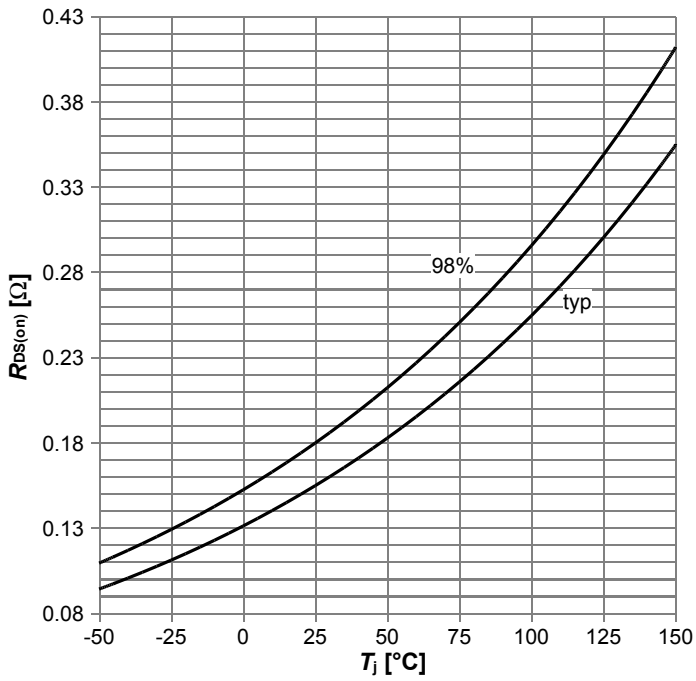
I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



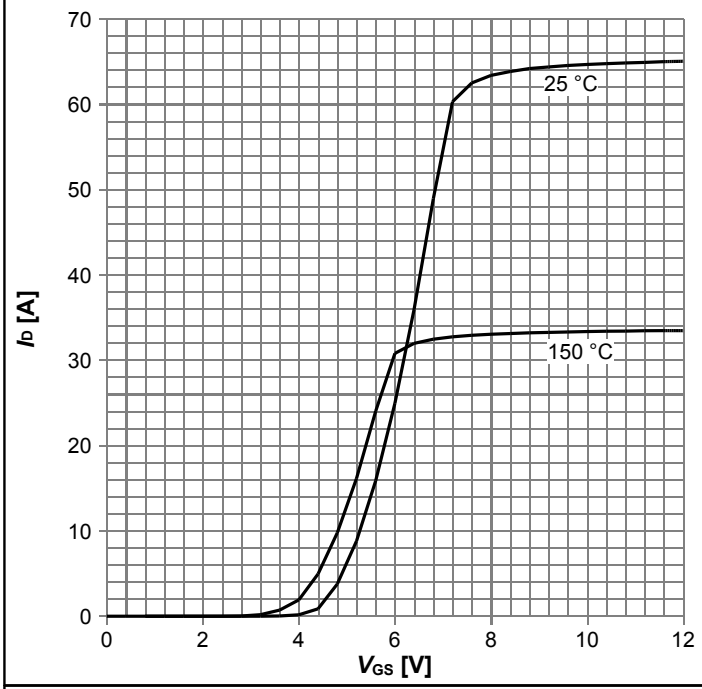
$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



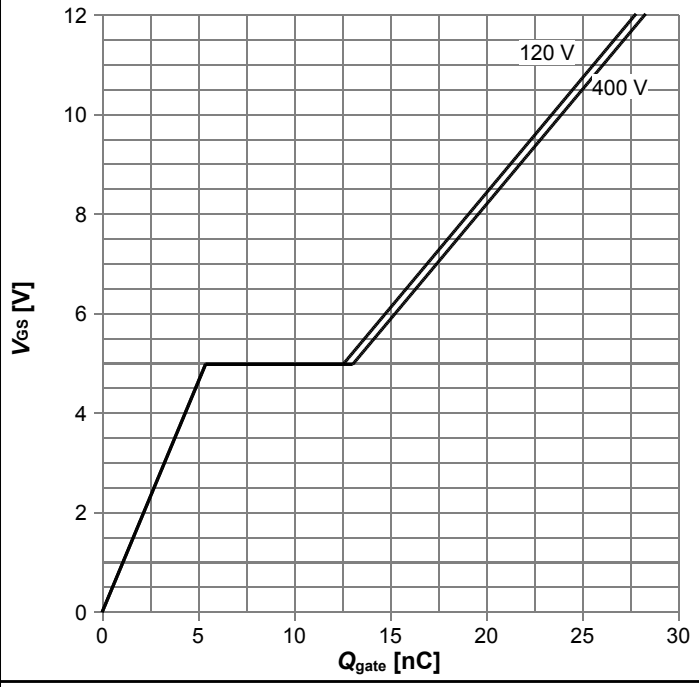
$R_{DS(on)}$=f(T_j); I_D=5.3 A; V_{GS}=10 V

Diagram 9: Typ. transfer characteristics



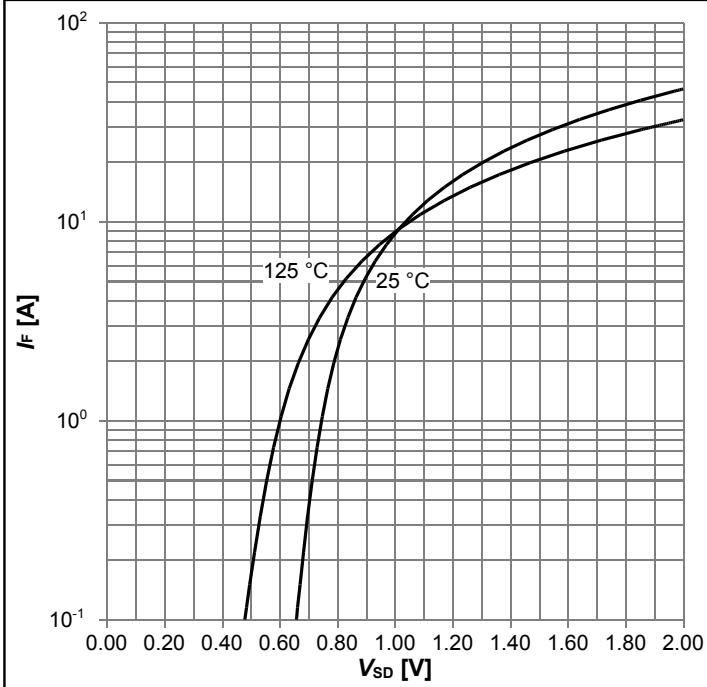
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



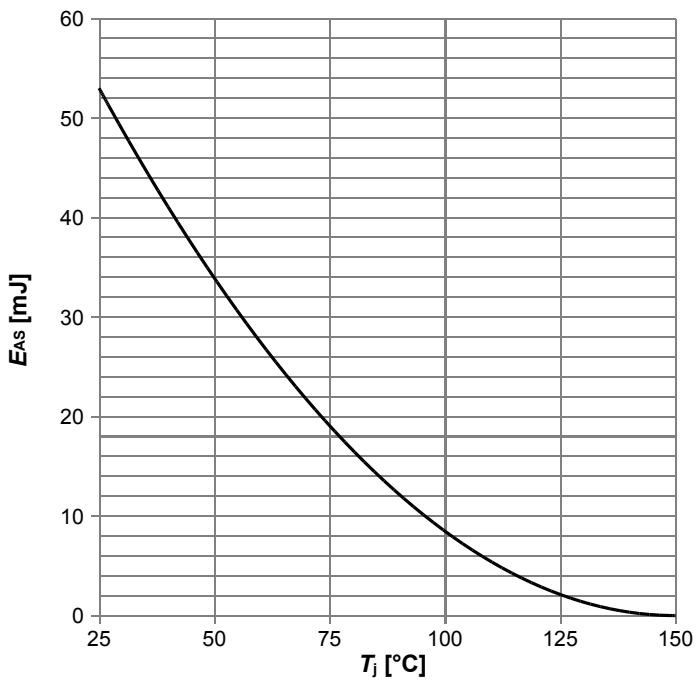
V_{GS}=f(Q_{gate}); I_D=5.3 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



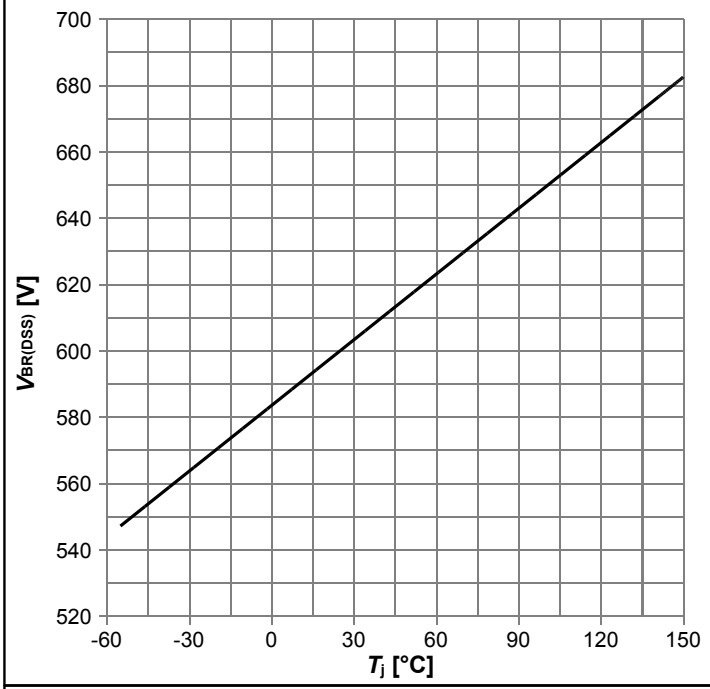
I_F=f(V_{SD}); parameter: T_j

Diagram 12: Avalanche energy



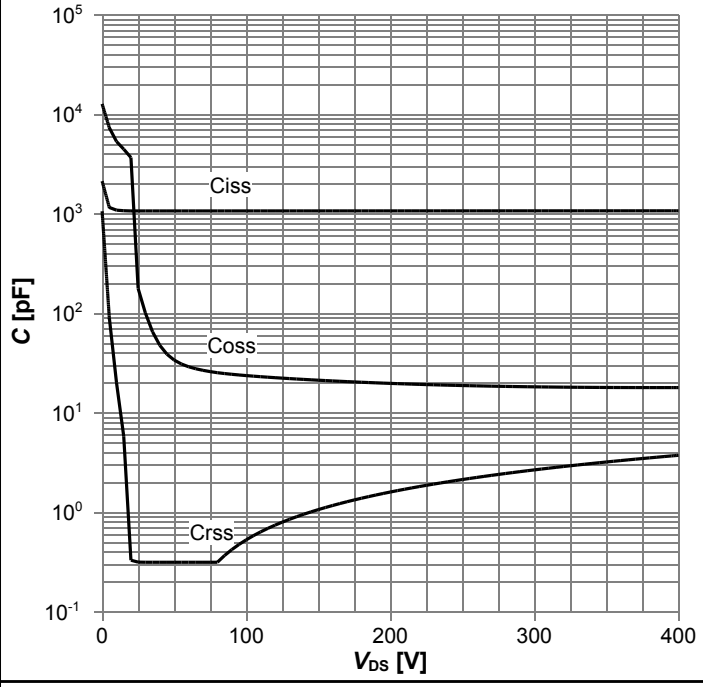
E_{AS}=f(T_j); I_D=3.3 A; V_{DD}=50 V

Diagram 13: Drain-source breakdown voltage



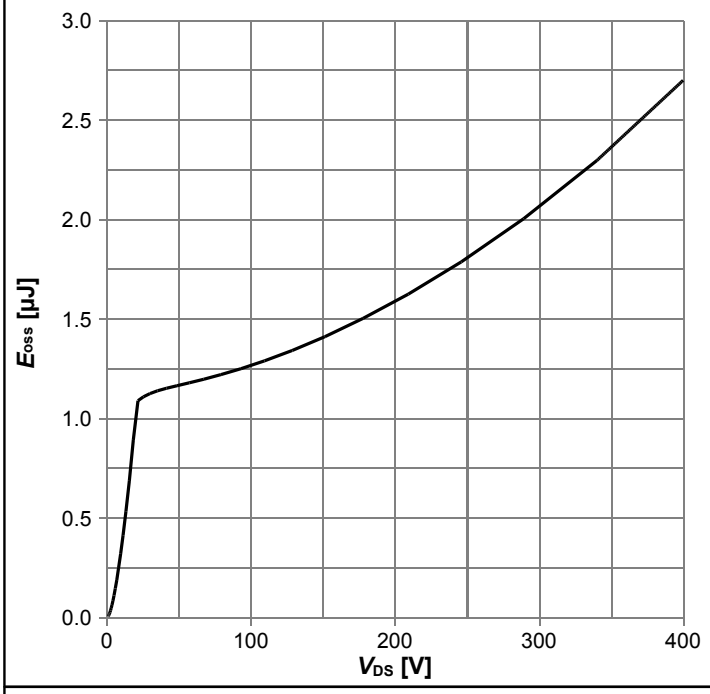
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy



E_{oss}=f(V_{DS})

6 Test Circuits

Table 8 Diode characteristics

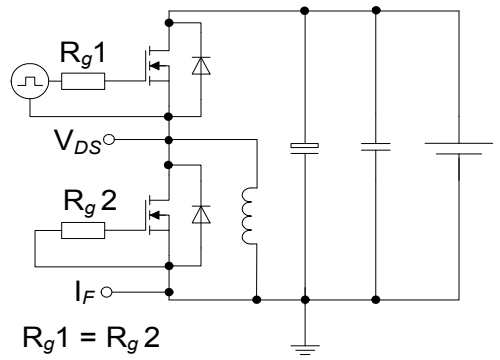
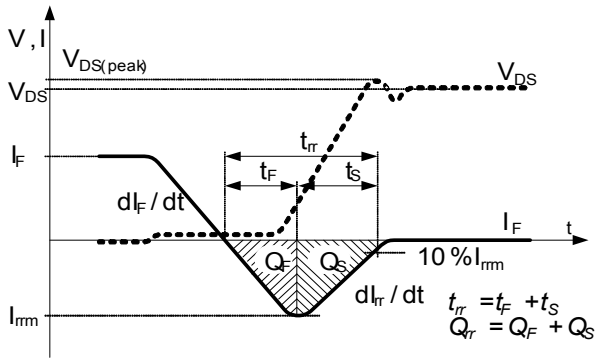
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

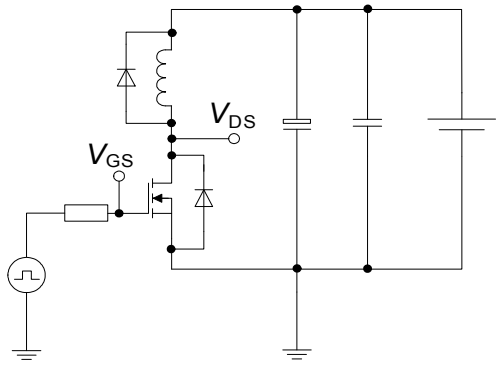
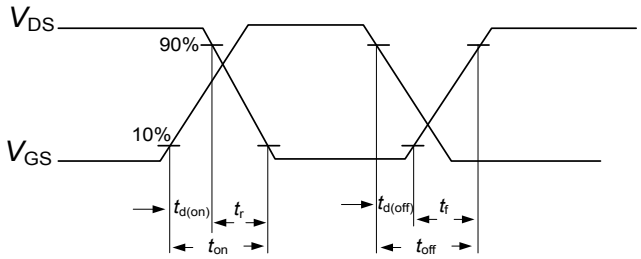
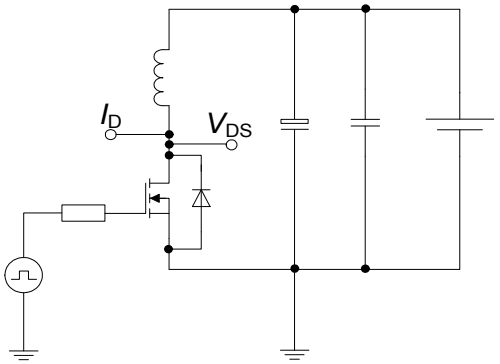
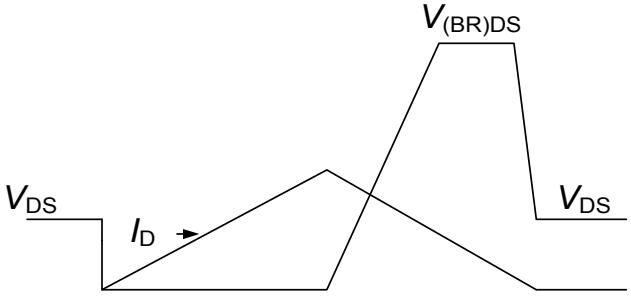
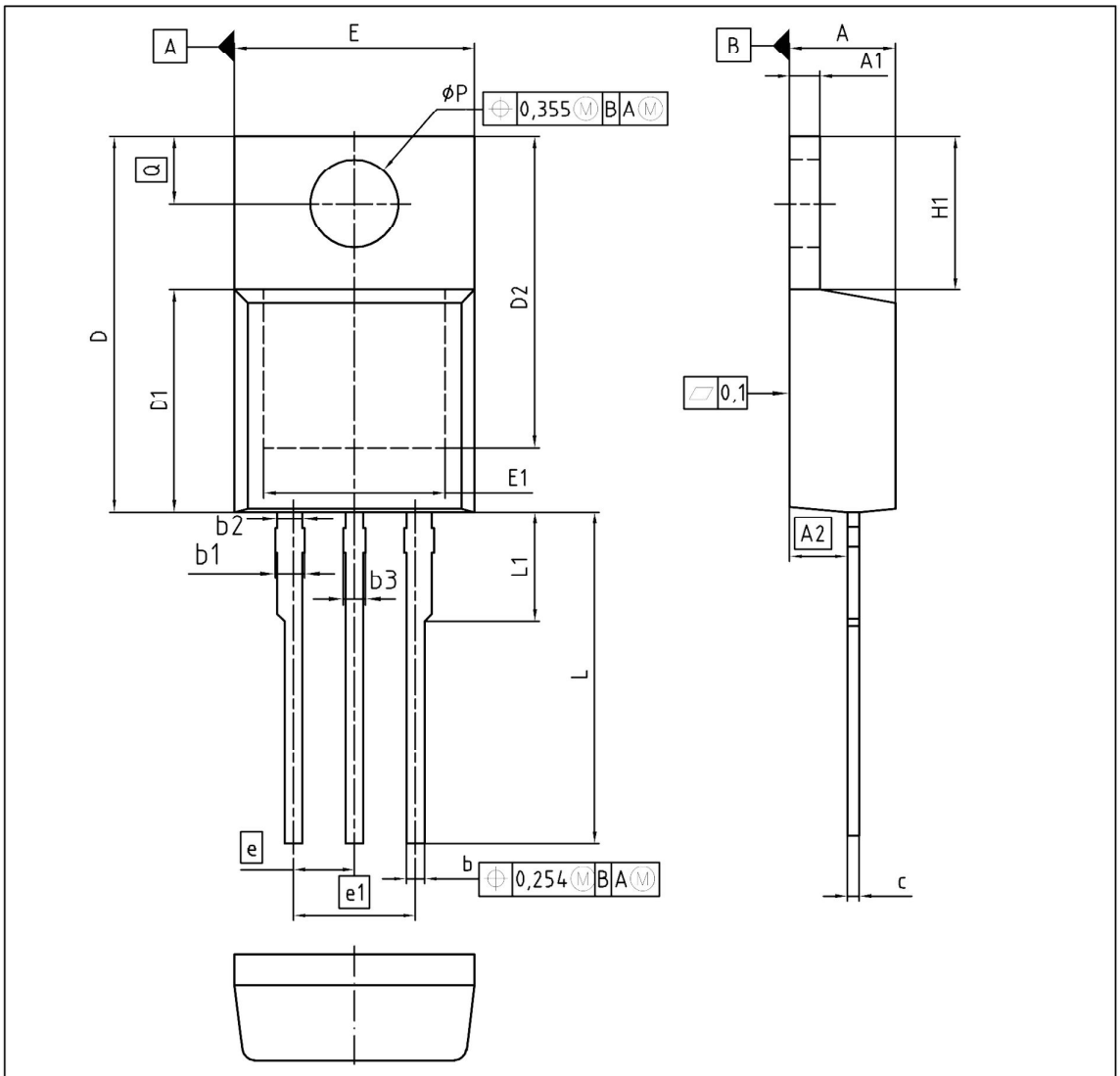
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

DOCUMENT NO.
Z8B00003318

SCALE 0 2.5 0 2.5 5mm

EUROPEAN PROJECTION

ISSUE DATE
30-07-2009

REVISION
06

Figure 1 Outline PG-TO 220, dimensions in mm/inches

8 Appendix A

Table 11 Related Links

- **IFX CoolMOS™ C7 Webpage:** www.infineon.com
- **IFX CoolMOS™ C7 application note:** www.infineon.com
- **IFX CoolMOS™ C7 simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPP60R180C7

Revision: 2015-05-08, Rev. 2.0

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2015-05-08	Release of final version

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