Voltage Supervisor with Microwire Serial CMOS EEPROM

HALOGEN FREE LEAD FREE™ RoHS Compliance

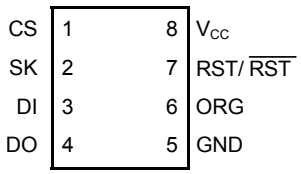
FEATURES

- **Precision Power Supply Voltage Monitor**
  - **5V, 3.3V, 3V & 2.5V systems**
  - **7 threshold voltage options**
- **Active High or Low Reset**
  - **Valid reset guaranteed at V_{CC} = 1 V**
- **High Speed Operation**
- **Selectable x8 or x16 memory organization**
- **Low power CMOS technology**
- **1,000,000 Program/Erase cycles**
- **100 year data retention**
- **Industrial temperature range**
- **RoHS-compliant 8-pin SOIC package**

For Ordering Information details, see page 13.

PIN CONFIGURATION

SOIC (W)



PIN FUNCTION

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
ORG	Memory Organization
RST/$\overline{RST}$	Reset Output
V_{CC}	Power Supply

Note:
When the ORG pin is connected to V_{CC}, the x16 organization is selected. When it is connected to ground, the x8 pin is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x16 organization.

DESCRIPTION

The CAT130xx (see table below) are memory and supervisory solutions for microcontroller based systems. A CMOS serial EEPROM memory and a system power supervisor with brown-out protection are integrated together. Memory interface is via Microwire serial protocol.

The CAT130xx provides a precision V_{CC} sense circuit with two reset output options: CMOS active low output or CMOS active high. The RESET output is active whenever V_{CC} is below the reset threshold or falls below the reset threshold voltage.

The power supply monitor and reset circuit protect system controllers during power up/down and against brownout conditions. Seven reset threshold voltages support 5V, 3.3V, 3V and 2.5V systems. If power supply voltages are out of tolerance reset signals become active, preventing the system microcontroller, ASIC or peripherals from operating. Reset signals become inactive typically 240ms after the supply voltage exceeds the reset threshold level.

MEMORY SIZE SELECTOR

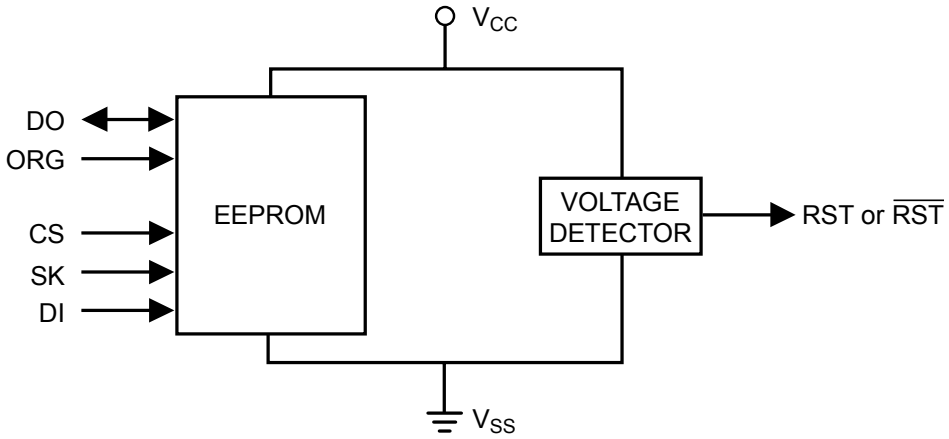
Product	Memory density
13001	1-Kbit
13004	4-Kbit
13008	8-Kbit
13016	16-Kbit

THRESHOLD SUFFIX SELECTOR

Nominal Threshold Voltage	Threshold Suffix Designation
4.63V	L
4.38V	M
4.00V	J
3.08V	T
2.93V	S
2.63V	R
2.32V	Z

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

Parameters	Ratings	Units
Storage Temperature	-65 to +150	°C
Voltage on Any Pin with Respect to Ground[2]	-0.5 to +6.5	V

RELIABILITY CHARACTERISTICS[3]

Symbol	Parameter	Min	Units
NEND[4]	Endurance	1,000,000	Program/ Erase Cycles
TDR	Data Retention	100	Years

D.C. OPERATING CHARACTERISTICS

V_{CC} = +2.5V to +5.5V unless otherwise specified.

Symbol	Parameter	Limits			Test Condition	Units
		Min.	Typ.	Max.		
I_{CC}	Supply Current			3	Read or Write at 1MHz	mA
I_{SB}	Standby Current		12	25	V_{CC} < 5.5V; All I/O Pins at V_{SS} or V_{CC}	µA
			10	20	V_{CC} < 3.6V; All I/O Pins at V_{SS} or V_{CC}	
I_L	I/O Pin Leakage			2	Pin at GND or V_{CC}	µA
V_{IL}	Input Low Voltage	-0.5		0.8		V
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.5		V
V_{OL}	Output Low Voltage			0.4	$V_{CC} \geq$ 2.5V, I_{OL} = 2.1mA	V
V_{OH}	Output High Voltage	2.4			$V_{CC} \geq$ 4.5V, I_{OH} = -0.4mA	V

Notes:

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

(2) The DC input voltage on any pin should not be lower than -0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

(3) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

(4) Block Mode, V_{CC} = 5 V, 25°C

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A.C. CHARACTERISTICS (MEMORY)[1]

V_{CC} = +2.5V to 5.5V, T_A = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Min	Max	Units
f_{SK}	Clock Frequency	DC	2000	kHz
t_{CSS}	CS Setup Time	50		ns
t_{CSH}	CS Hold Time	0		ns
t_{CSMIN}	Minimum CS Low Time	0.25		µs
t_{SKHI}	Minimum SK High Time	0.25		µs
t_{SKLOW}	Minimum SK Low Time	0.25		µs
t_{DIS}	DI Setup Time	100		ns
t_{DIH}	DI Hold Time	100		ns
t_{PD1}	Output Delay to 1		0.25	µs
t_{PD0}	Output Delay to 0		0.25	µs
t_{HZ}[1]	Output Delay to High-Z		100	ns
t_{SV}	Output Delay to Status Valid		0.25	µs
t_{EW}	Program/Erase Pulse Width		5	ms
t_{PU}[2], [3]	Power-up to Ready Mode		1	ms

Notes:

(1) Test conditions according to “A.C. Test Conditions” table.

(2) Tested initially and after a design or process change that affects this parameter.

(3) t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

A.C. TEST CONDITIONS

Input Rise and Fall Times	≤ 50 ns
Input Levels	0.4V to 2.4V (4.5V < V_{CC} < 5.5V)
Input Levels	0.2V_{CC} to 0.7V_{CC} (2.5V < V_{CC} < 4.5V)
Timing Reference Levels	0.8V, 2.0V (4.5V < V_{CC} < 5.5V)
Timing Reference Levels	0.5V_{CC} (2.5V < V_{CC} < 4.5V)
Output Load	Current Source: $I_{OL\ max}$ / $I_{OH\ max}$; C_L = 100pF

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ELECTRICAL CHARACTERISTICS (SUPERVISORY FUNCTION)

V_{CC} = Full range, T_A = -40ºC to +85ºC unless otherwise noted. Typical values at T_A = +25ºC and V_{CC} = 5V for L/M/J versions, V_{CC} = 3.3V for T/S versions, V_{CC} = 3V for R version and V_{CC} = 2.5V for Z version.

Symbol	Parameter	Threshold	Conditions	Min	Typ	Max	Units
V_{TH}	Reset Threshold Voltage	L	T_A = +25ºC	4.56	4.63	4.70	V
			T_A = -40ºC to +85ºC	4.50		4.75	
		M	T_A = +25ºC	4.31	4.38	4.45	
			T_A = -40ºC to +85ºC	4.25		4.50	
		J	T_A = +25ºC	3.93	4.00	4.06	
			T_A = -40ºC to +85ºC	3.89		4.10	
		T	T_A = +25ºC	3.04	3.08	3.11	
			T_A = -40ºC to +85ºC	3.00		3.15	
		S	T_A = +25ºC	2.89	2.93	2.96	
			T_A = -40ºC to +85ºC	2.85		3.00	
		R	T_A = +25ºC	2.59	2.63	2.66	
			T_A = -40ºC to +85ºC	2.55		2.70	
		Z	T_A = +25ºC	2.28	2.32	2.35	
			T_A = -40ºC to +85ºC	2.25		2.38	

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Units
	Reset Threshold Tempco			30		ppm/ºC
t_{RPD}	V_{CC} to Reset Delay[2]	V_{CC} = V_{TH} to (V_{TH} -100mV)		20		µs
t_{PURST}	Reset Active Timeout Period	T_A = -40ºC to +85ºC	140	240	460	ms
V_{OL}	$\overline{\text{RESET}}$ Output Voltage Low (Push-pull, active LOW, CAT130xx9)	V_{CC} = V_{TH} min, I_{SINK} = 1.2 mA R/S/T/Z			0.3	V
		V_{CC} = V_{TH} min, I_{SINK} = 3.2 mA J/L/M			0.4	
		V_{CC} > 1.0V, I_{SINK} = 50µA			0.3	
V_{OH}	$\overline{\text{RESET}}$ Output Voltage High (Push-pull, active LOW, CAT130xx9)	V_{CC} = V_{TH} max, I_{SOURCE} = -500µA R/S/T/Z	0.8V_{CC}			V
		V_{CC} = V_{TH} max, I_{SOURCE} = -800µA J/L/M	V_{CC} - 1.5			
V_{OL}	RESET Output Voltage Low (Push-pull, active HIGH, CAT130xx1)	V_{CC} > V_{TH} max, I_{SINK} = 1.2mA R/S/T/Z			0.3	V
		V_{CC} > V_{TH} max, I_{SINK} = 3.2mA J/L/M			0.4	
V_{OH}	RESET Output Voltage High (Push-pull, active HIGH, CAT130xx1)	1.8V < V_{CC} ≤ V_{TH} min, I_{SOURCE} = -150µA	0.8V_{CC}			V

Notes:

(1) Production testing done at T_A = +25ºC; limits over temperature guaranteed by design only.

(2) $\overline{\text{RESET}}$ output for the CAT130xx9; RESET output for the CAT130xx1.

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PIN DESCRIPTION

RESET/$\overline{\text{RESET}}$: The reset output is available in two versions: CMOS Active Low (CAT130xx9) and CMOS Active High (CAT130xx1). Both versions are push-pull outputs for high efficiency.

DI: The serial data input pin accepts op-codes, addresses and data. The input data is latched on the rising edge of the SK clock input.

DO: The serial data output pin is used to transfer data out of the device. The data is shifted out on the rising edge of the SK clock.

SK: The serial clock input pin accepts the clock provided by the host and used for synchronizing communication between host and CAT130xx device.

CS: The chip select input pin is used to enable/disable the CAT130xx. When CS is high, the device is selected and accepts op-codes, addresses and data. Upon receiving a Write or Erase instruction, the falling edge of CS will start the internal write cycle to the selected memory location.

ORG: The memory organization input selects the memory configuration as either register of 16 bits (ORG tied to V_{CC} or floating) or 8 bits (ORG connected to GND).

DEVICE OPERATION

The CAT130xx products combine the accurate voltage monitoring capabilities of a standalone voltage supervisor with the high quality and reliability of standard EEPROMs from Catalyst Semiconductor.

RESET CONTROLLER DESCRIPTION

The reset signal is asserted LOW for the CAT130xx9 and HIGH for the CAT130xx1 when the power supply voltage falls below the threshold trip voltage and remains asserted for at least 140ms (t_{PURST}) after the power supply voltage has risen above the threshold. Reset output timing is shown in Figure 1.

The CAT130xx devices protect µPs against brownout failure. Short duration V_{CC} transients of 4µsec or less and 100mV amplitude typically do not generate a Reset pulse.

Figure 2 shows the maximum pulse duration of negative-going V_{CC} transients that do not cause a reset condition. As the amplitude of the transient goes further below the threshold (increasing V_{TH} - V_{CC}), the maximum pulse duration decreases. In this test, the V_{CC} starts from an initial voltage of 0.5V above the threshold and drops below it by the amplitude of the overdrive voltage (V_{TH} - V_{CC}).

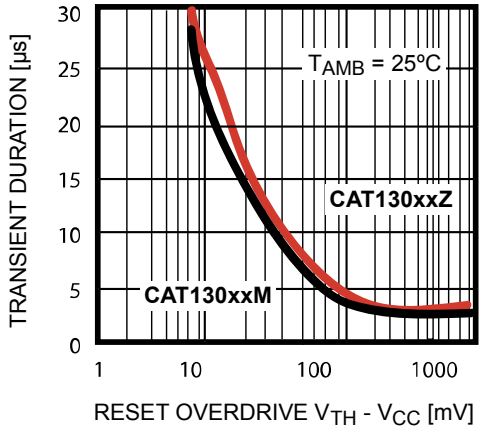


Figure 2. Maximum Transient Duration without Causing a Reset Pulse vs. Overdrive Voltage

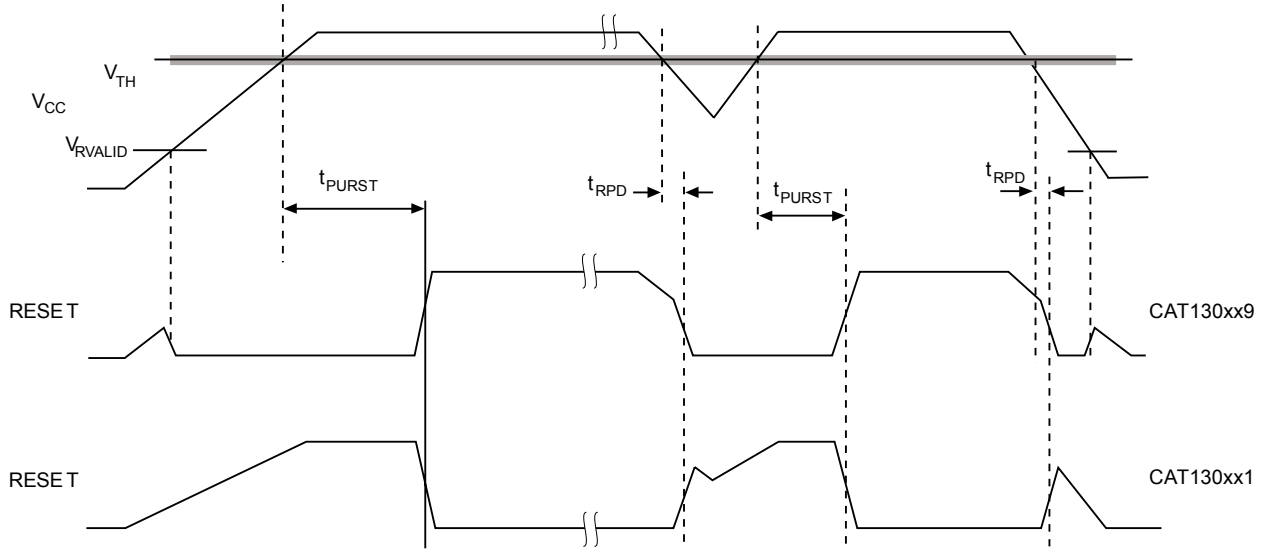


Figure 1. RESET Output Timing

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EMBEDDED EEPROM OPERATION

The CAT130xx has a nonvolatile embedded memory intended for use with industry standard micropro–cessors. The memory can be organized as either registers of 16 bits or 8 bits. The CAT130xx operates on a single power supply and will generate on chip the high voltage required during any write operation.

The format for all instructions sent to the device is a logical “1” start bit, a 2-bit (or 4-bit) opcode, 6-bit (13001) / 8-bit (13004) / 9-bit (13008) / 10-bit (13016) address (an additional bit when organized as x8) and for write operations a 16-bit data field (8-bit for x8 organization). The instruction format is shown in Instruction Set Table.

INSTRUCTION SET

Instruction	Device	Start Bit	Opcode	Address		Data		Comments
				x 8	x 16	x 8	x 16	
READ	13001	1	10	A6-A0	A5-A0			Read Address AN-A0
	13004	1	10	A8-A0	A7-A0			
	13008	1	10	A9-A0	A8-A0			
	13016	1	10	A10-A0	A9-A0			
ERASE	13001	1	11	A6-A0	A5-A0			Clear Address AN-A0
	13004	1	11	A8-A0	A7-A0			
	13008	1	11	A9-A0	A8-A0			
	13016	1	11	A10-A0	A9-A0			
WRITE	13001	1	01	A6-A0	A5-A0	D7-D0	D15-D0	Write Address AN-A0
	13004	1	01	A8-A0	A7-A0	D7-D0	D15-D0	
	13008	1	01	A9-A0	A8-A0	D7-D0	D15-D0	
	13016	1	01	A10-A0	A9-A0	D7-D0	D15-D0	
EWEN	13001	1	00	11xxxxx	11xxxx			Write Enable
	13004	1	00	11xxxxxxx	11xxxxxx			
	13008	1	00	11xxxxxxxx	11xxxxxxx			
	13016	1	00	11xxxxxxxxx	11xxxxxxxx			
EWDS	13001	1	00	00xxxxx	00xxxx			Write Disable
	13004	1	00	00xxxxxxx	00xxxxxx			
	13008	1	00	00xxxxxxxx	00xxxxxxx			
	13016	1	00	00xxxxxxxxx	00xxxxxxxx			
ERAL	13001	1	00	10xxxxx	10xxxx			Clear All Addresses
	13004	1	00	10xxxxxxx	10xxxxxx			
	13008	1	00	10xxxxxxxx	10xxxxxxx			
	13016	1	00	10xxxxxxxxx	10xxxxxxxx			
WRAL	13001	1	00	01xxxxx	01xxxx	D7-D0	D15-D0	Write All Addresses
	13004	1	00	01xxxxxxx	01xxxxxx	D7-D0	D15-D0	
	13008	1	00	01xxxxxxxx	01xxxxxxx	D7-D0	D15-D0	
	13016	1	00	01xxxxxxxxx	01xxxxxxxx	D7-D0	D15-D0	

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Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status during a write operation. The serial communication protocol follows the timing shown in Figure 3.

The ready/busy status can be determined after the start of internal write cycle by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the rising edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin. The Ready/Busy flag can be disabled only in Ready state; no change is allowed in Busy state.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT130xx will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}). The READ instruction timing is illustrated in Figure 4.

For the CAT13004/08/16, after the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches to the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data word is preceeded by a dummy zero bit. All subsequent data words will follow without a dummy zero bit.

Figure 3. Sychronous Data Timing

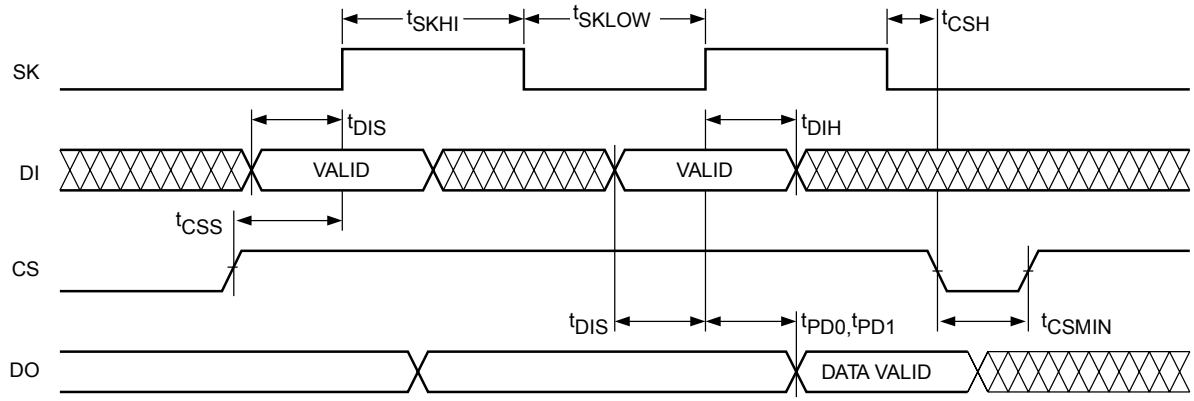
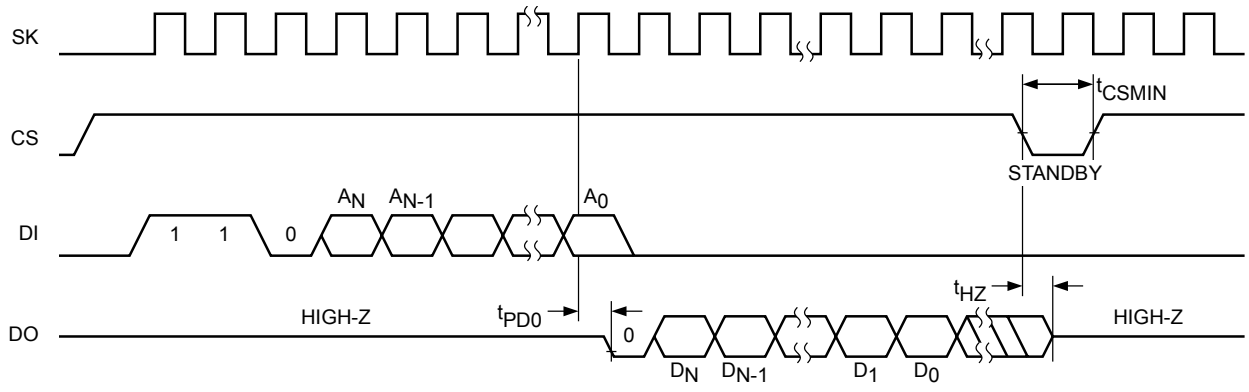


Figure 4. Read Instruction Timing



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Erase/Write Enable and Disable

The CAT130xx powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT130xx write and erase instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status. The EWEN and EWDS instructions timing is shown in Figure 5.

Write

After receiving a WRITE command (Figure 6), address and the data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking for auto-clear and data store cycles on the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT130xx can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before it is written into.

Figure 5. EWEN/EWDS Instruction Timing

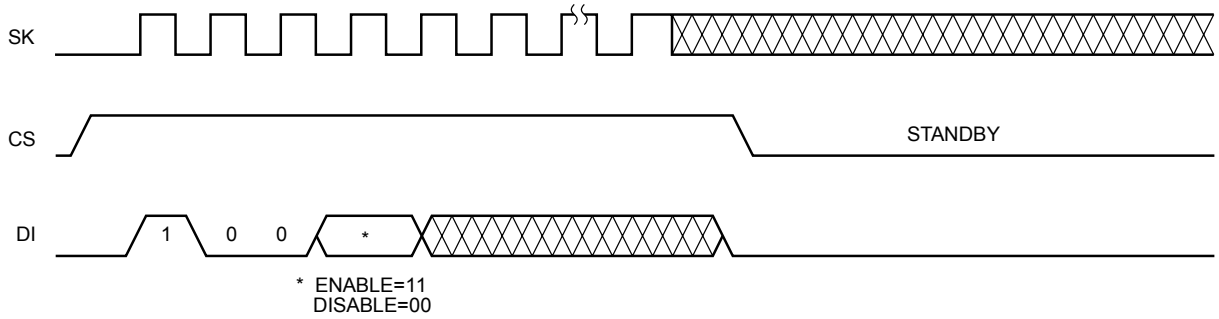
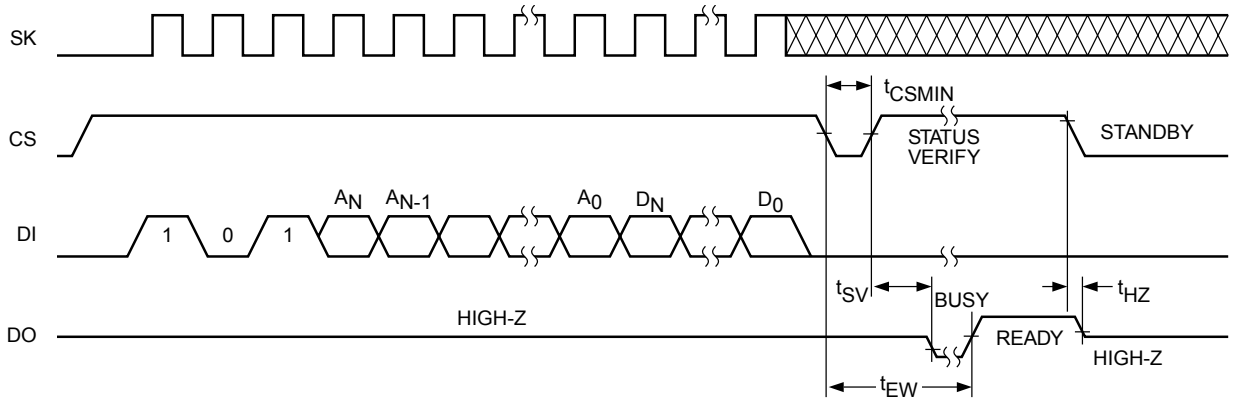


Figure 6. Write Instruction Timing



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Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of t_{CSMIN} (Figure 7). The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT130xx can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical “1” state.

Erase All

Upon receiving an ERAL command (Figure 8), the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT130xx can be determi–ned by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical “1” state.

Figure 7. Erase Instruction Timing

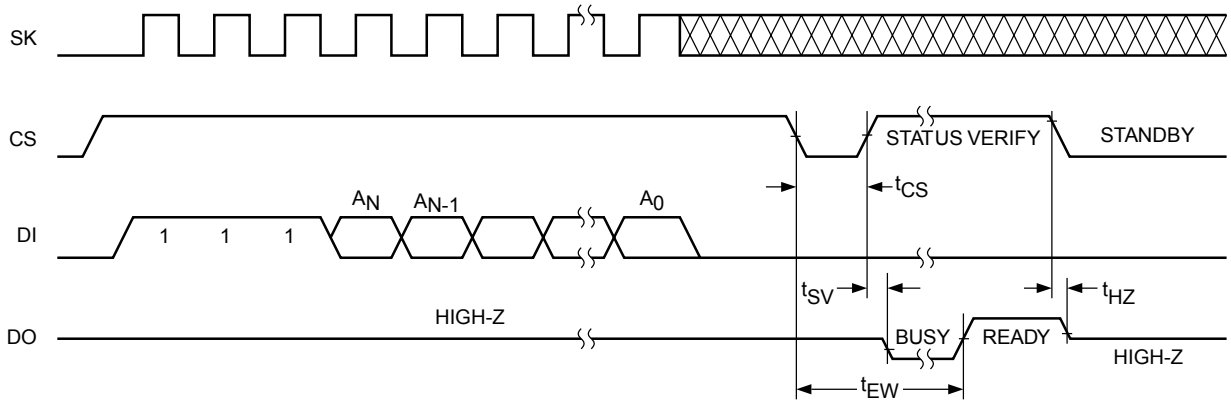
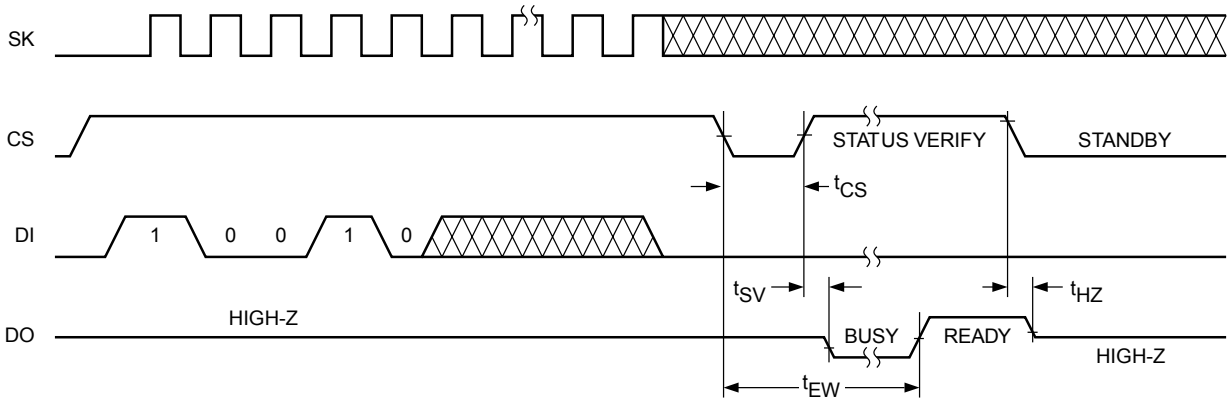


Figure 8. ERAL Instruction Timing



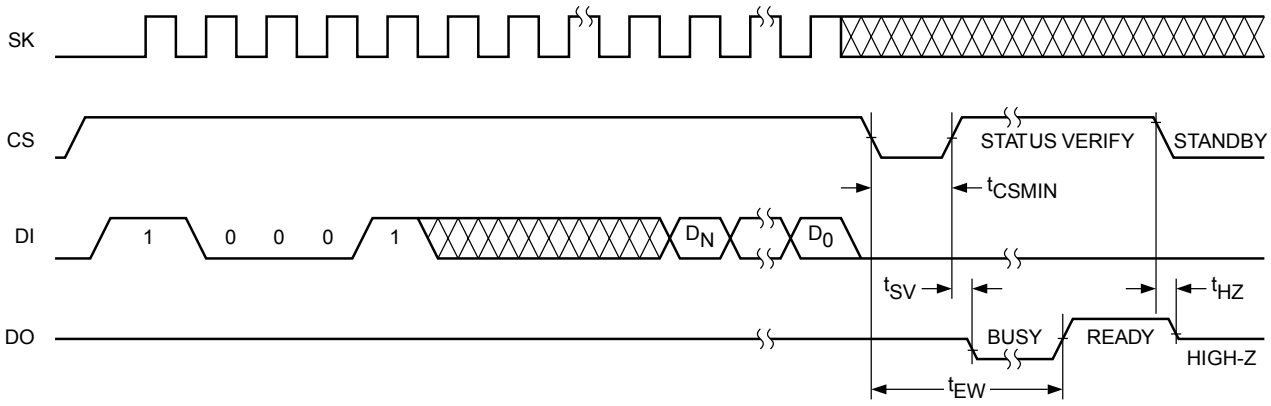
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Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN} (Figure 9). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode.

The ready/busy status of the CAT130xx can be deter–mined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

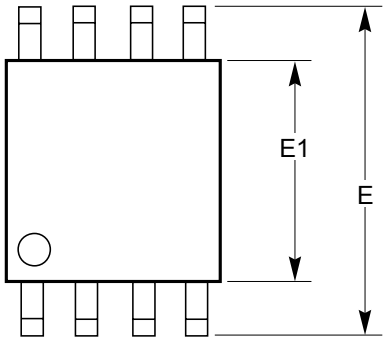
Figure 9. WRAL Instruction Timing

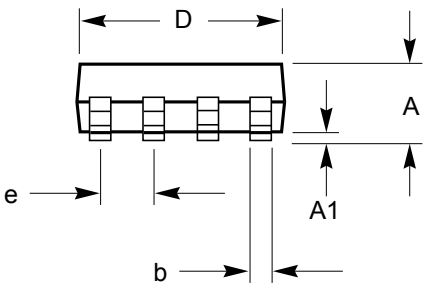


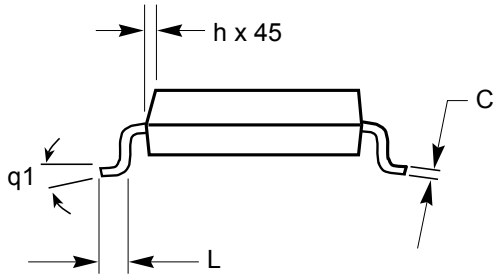
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PACKAGE OUTLINES

8-LEAD 150 MIL SOIC (W)







SYMBOL	MIN	NOM	MAX
A1	0.10		0.25
A	1.35		1.75
b	0.33		0.51
C	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
q1	0°		8°

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:

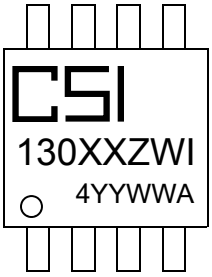
(1) All dimensions are in millimeters.

(2) Complies with JEDEC specification MS-012 dimensions.

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PACKAGE MARKING

8-LEAD SOIC



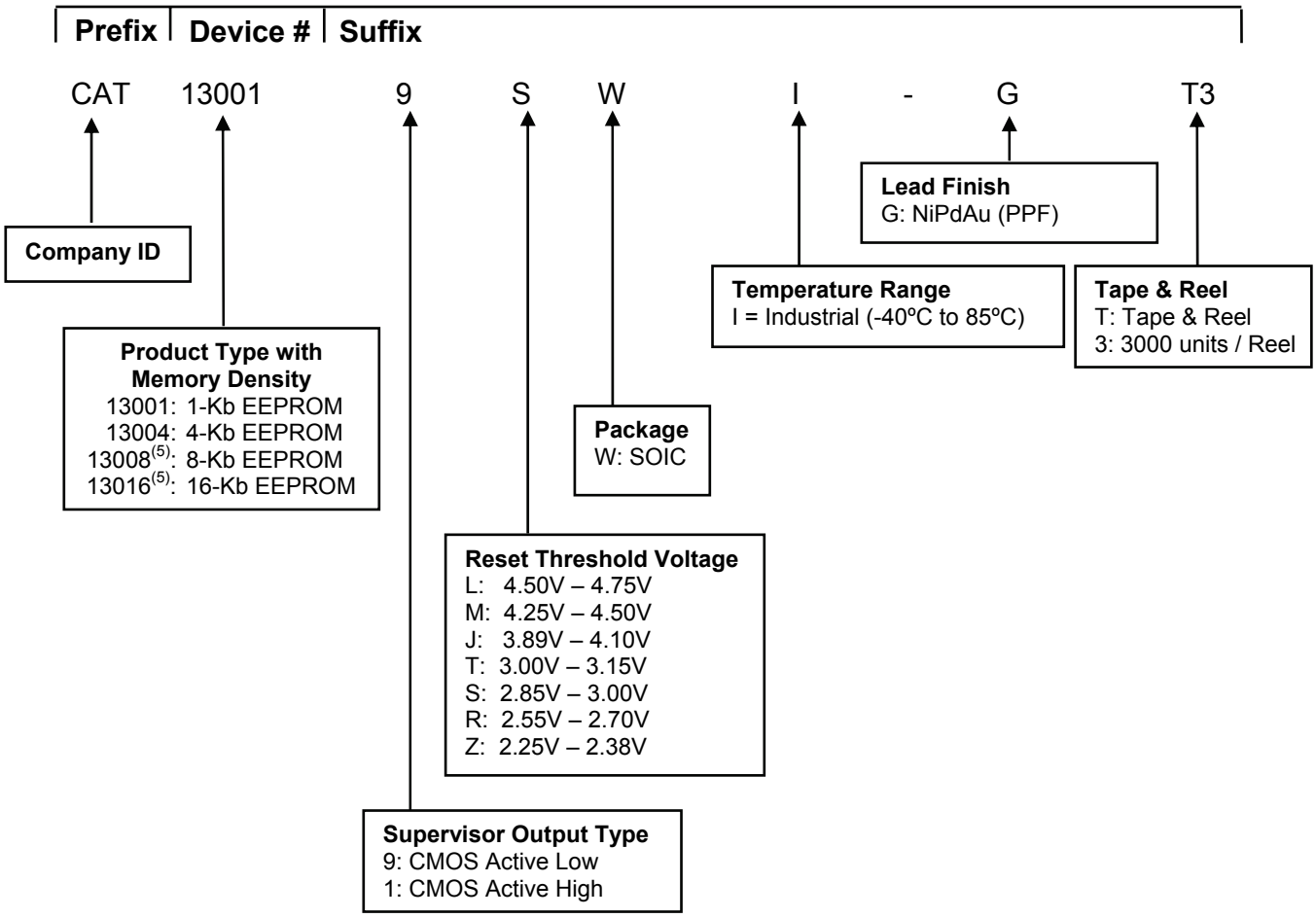
CSI = Catalyst Semiconductor, Inc.
XX = Device Code (see Marking Code table below)
Z = Supervisory Output Code (see Marking Code table below)
I = Temperature Range
YY = Production Year
WW = Production Week
A = Product Revision
4 = Lead Finish NiPdAu

	Device Marking Codes XX
13001	01
13004	04
13008	08
13016	16

	Supervisory Marking Codes Z
Output Active Low	9
Output Active High	1

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EXAMPLE OF ORDERING INFORMATION



Notes:

(1) All packages are RoHS-compliant (Lead-free, Halogen-free).

(2) The standard lead finish is NiPdAu pre-plated (PPF) lead frames.

(3) The device used in the above example is a CAT130019SWI-GT3 (1Kb EEPROM, with Active Low CMOS output, with a reset threshold between 2.85V - 3.00V, in an SOIC, Industrial Temperature, NiPdAu, Tape and Reel.

(4) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

(5) For 8-Kb and 16-Kb embedded EEPROM option availability please contact your nearest Catalyst Semiconductor Sales office.

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REVISION HISTORY

Date	Rev.	Reason
01/17/07	A	Initial Issue

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Catalyst Semiconductor, Inc.
Corporate Headquarters
2975 Stender Way
Santa Clara, CA 95054
Phone: 408.542.1000
Fax: 408.542.1200
www.catsemi.com

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CAV25M01YE-GT3 74ABT541CMTC MVMBF0201NLT1G BAS19LT3G QT7810X CAT823TTDI-GT3 RB751V40T1G SBAT54CWT1G-M02 NL17SZ126DFT2G NCV20072DR2G MC74LVX244DWR2G NCV431BSNT1G FDMC86261P FDMS86202 1N5344BRLG NCV7344AD10R2G FOD3120SDV 74LCX244WM NTS4101PT1G MMSZ5255BT1G MC7815CTG SVC704-TL-E 1N4749ATR MC14538BDTR2G FAN3229TMX-F085 LM2901MX MC34161DG NTS2101PT1G MMVL2101T1G ESD9X7.0ST5G