NUP4114 Series

ESD Protection Diode
Low Clamping Voltage

The NUP4114 ESD protection diode array is designed to protect high speed data lines from ESD. Ultra−low capacitance and high level of ESD protection make these devices well suited for use in USB 2.0 high speed applications.

Features

- Low Clamping Voltage
- Low Capacitance (<0.6 pF Typical, I/O to GND)
- Low Leakage
- Response Time is Typically < 1.0 ns
- IEC61000−4−2 Level 4 ESD Protection
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- LVDS
- USB 2.0 High Speed Data Line and Power Line Protection
- Digital Video Interface (DVI) and HDMI
- Gigabit Ethernet
- Monitors and Flat Panel Displays
- Notebook Computers

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

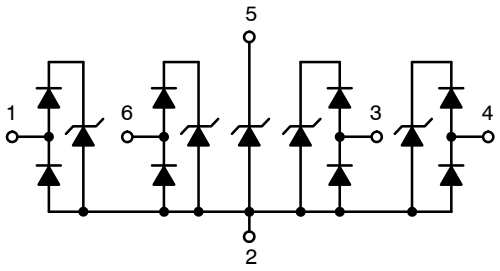
Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
IEC 61000−4−2 Contact IEC 61000−4−2 Air ISO 10605 330 pF / 330 Ω Contact ISO 10605 330 pF / 2 kΩ Contact ISO 10605 150 pF / 2 kΩ Contact	ESD	±8 ±15 ±10 ±21 ±30	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

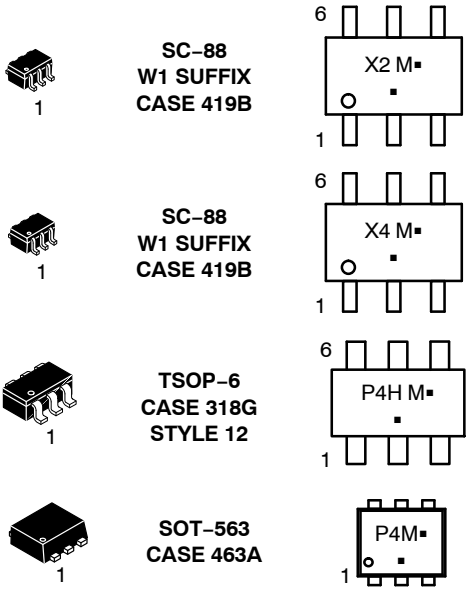
See Application Note AND8308/D for further description of survivability specs.

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MARKING DIAGRAMS



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

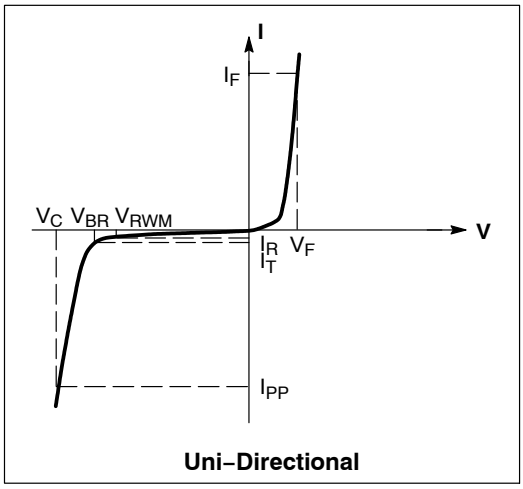
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ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Capacitance @ V_R = 0 and f = 1.0 MHz

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Uni−Directional

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}				5.5	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, (Note 1)	5.5	6.5		V
Reverse Leakage Current	I_R	V_{RWM} = 5.5 V			1.0	μA
Clamping Voltage	V_C	I_{PP} = 1 A (Note 2)		8.3	10	V
		I_{PP} = 5 A (Note 3)		8.5	9.0	V
		I_{PP} = 8 A (Note 3)		9.2	10	V
ESD Clamping Voltage	V_C	Per IEC61000−4−2 (Note 4)	See Figures 1 & 2			
Maximum Peak Pulse Current	I_{PP}	8/20 μs Waveform (Note 3)			12	A
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND			0.6	pF
		V_R = 0 V, f = 1 MHz between I/O Pins			0.3	pF

1. V_{BR} is measured at pulse test current I_T.
2. Nonrepetitive current pulse (I/O to GND).
3. Nonrepetitive current pulse (Pin 5 to Pin 2)
4. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

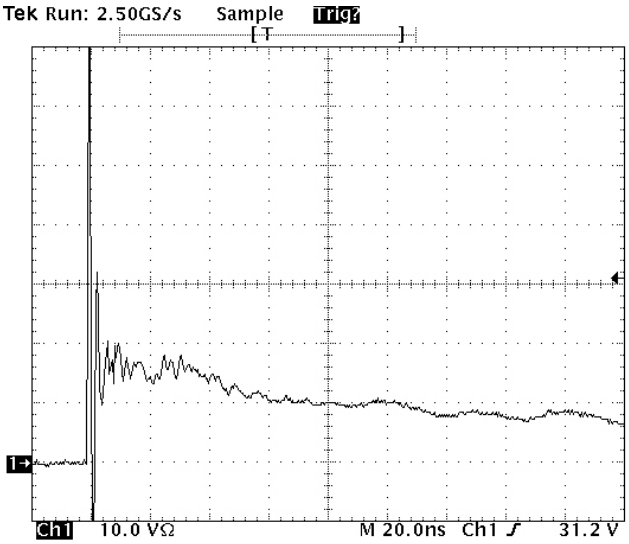


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

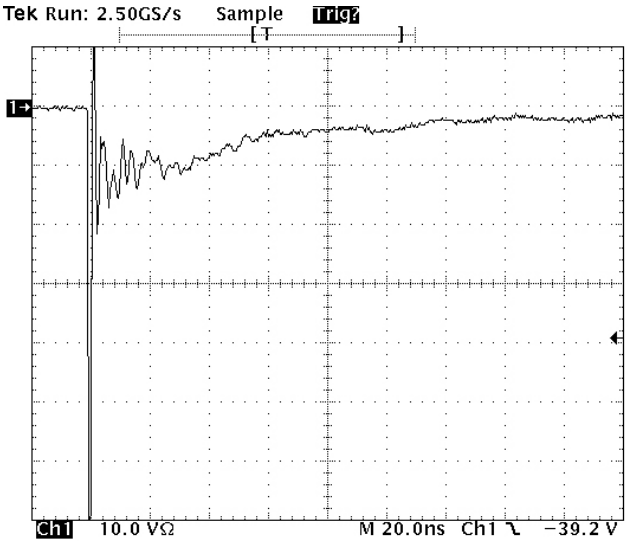


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

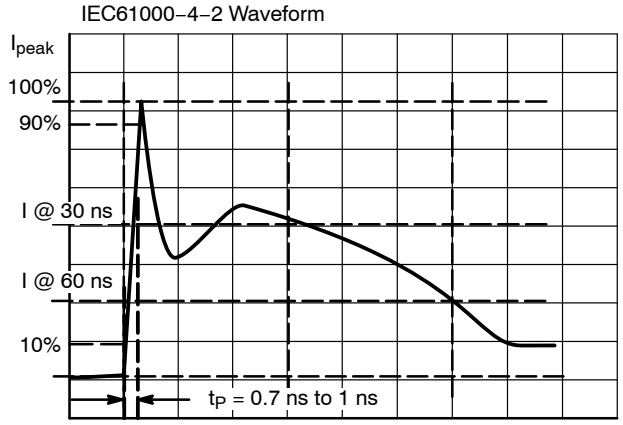


Figure 3. IEC61000−4−2 Spec

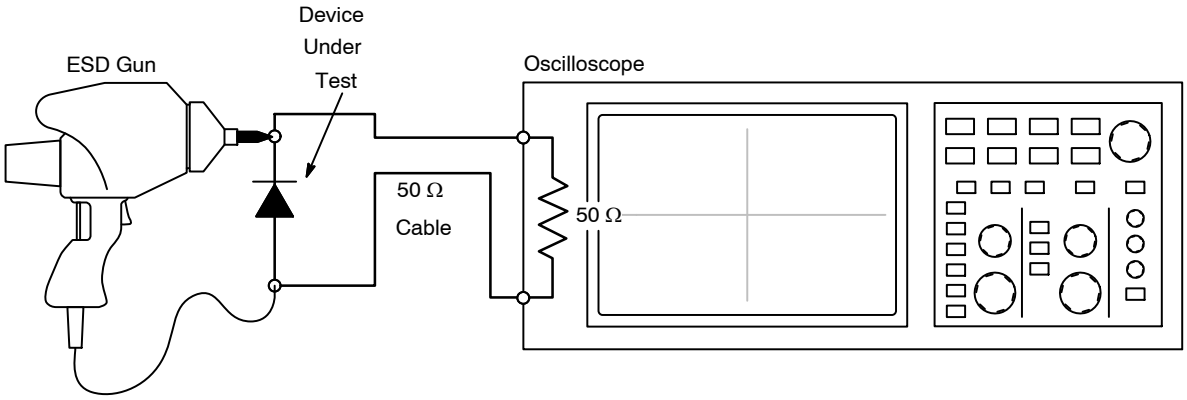


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

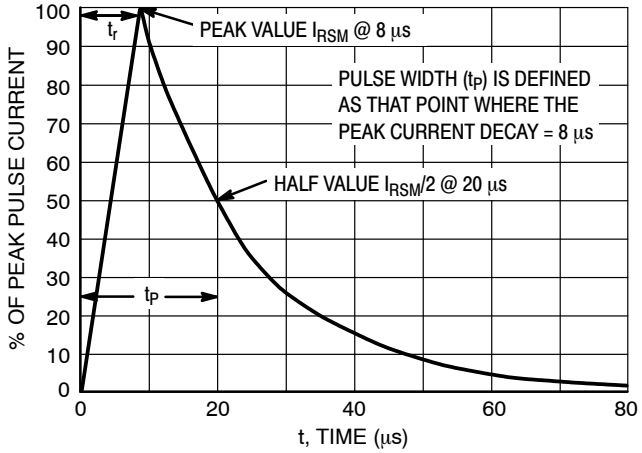


Figure 5. 8/20 μs Pulse Waveform

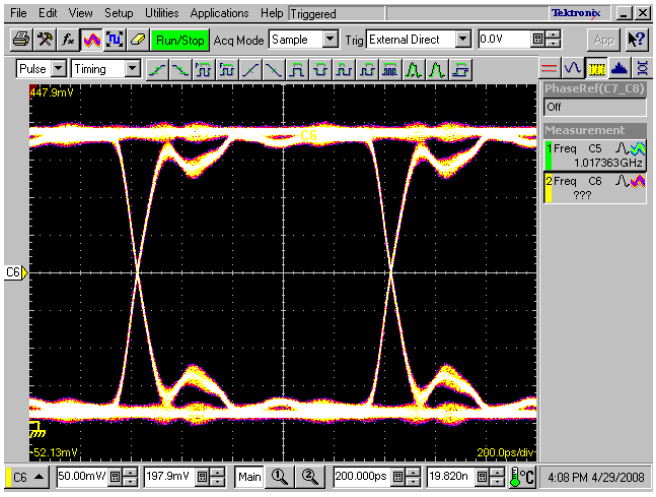


Figure 6. 500 MHz Data Pattern

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NUP4114UCLW1T1G	X2	SC−88 (Pb−Free)	3000 / Tape & Reel
NUP4114UCLW1T2G	X2		
SZNUP4114UCLW1T2G	X2		
NUP4114UCW1T2G	X4		
NUP4114UPXV6T1G	P4	SOT−563 (Pb−Free)	4000 / Tape & Reel
NUP4114UPXV6T2G			
NUP4114HMR6T1G	P4H	TSOP−6 (Pb−Free)	3000 / Tape & Reel
SZNUP4114HMR6T1G	P4H		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

APPLICATIONS INFORMATION

The new NUP4114 is a low capacitance ESD diode array designed to protect sensitive electronics such as communications systems, computers, and computer peripherals against damage due to ESD events or transient overvoltage conditions. Because of its low capacitance, it can be used in high speed I/O data lines. The integrated design of the NUP4114 offers low capacitance steering diodes and an ESD diode integrated in a single package (TSOP−6). If a transient condition occurs, the steering diodes will drive the transient to the positive rail of the power supply or to ground. This device protects the power line against overvoltage conditions to avoid damage to the power supply and any downstream components.

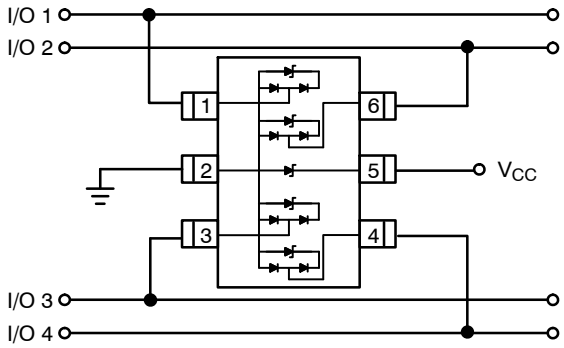
NUP4114 Configuration Options

The NUP4114 is able to protect up to four data lines against transient overvoltage conditions by driving them to a fixed reference point for clamping purposes. The steering diodes will be forward biased whenever the voltage on the protected line exceeds the reference voltage (V_f or $V_{CC} + V_f$). The diodes will force the transient current to bypass the sensitive circuit.

Data lines are connected at pins 1, 3, 4 and 6. The negative reference is connected at pin 2. This pin must be connected directly to ground by using a ground plane to minimize the PCB's ground inductance. It is very important to reduce the PCB trace lengths as much as possible to minimize parasitic inductances.

Option 1

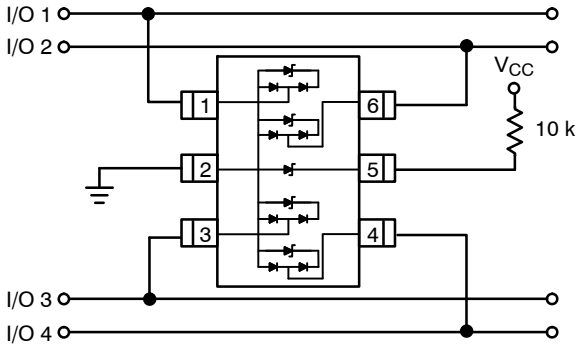
Protection of four data lines and the power supply using V_{CC} as reference.



For this configuration, connect pin 5 directly to the positive supply rail (V_{CC}), the data lines are referenced to the supply voltage. The internal ESD diode prevents overvoltage on the supply rail. Biasing of the steering diodes reduces their capacitance.

Option 2

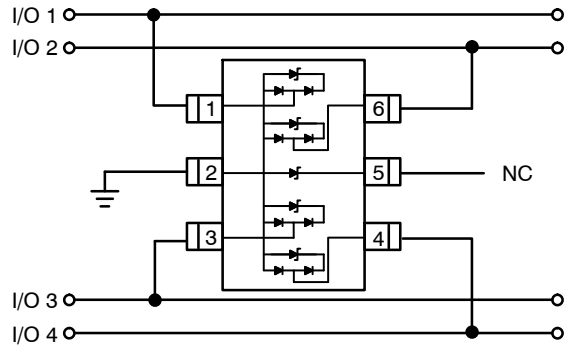
Protection of four data lines with bias and power supply isolation resistor.



The NUP4114 can be isolated from the power supply by connecting a series resistor between pin 5 and V_{CC}. A 10 kΩ resistor is recommended for this application. This will maintain a bias on the internal ESD and steering diodes, reducing their capacitance.

Option 3

Protection of four data lines using the internal ESD diode as reference.

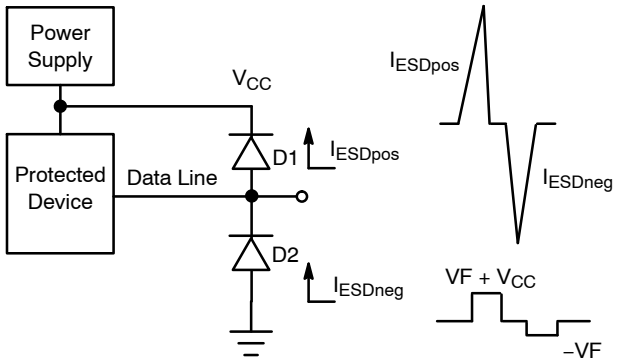


In applications lacking a positive supply reference or those cases in which a fully isolated power supply is required, the internal ESD can be used as the reference. For these applications, pin 5 is not connected. In this configuration, the steering diodes will conduct whenever the voltage on the protected line exceeds the working voltage of the ESD plus one diode drop ($V_C = V_f + V_{ESD}$).

ESD Protection of Power Supply Lines

When using diodes for data line protection, referencing to a supply rail provides advantages. Biasing the diodes reduces their capacitance and minimizes signal distortion.

Implementing this topology with discrete devices does have disadvantages. This configuration is shown below:



Looking at the figure above, it can be seen that when a positive ESD condition occurs, diode D1 will be forward biased while diode D2 will be forward biased when a negative ESD condition occurs. For slower transient conditions, this system may be approximated as follows:

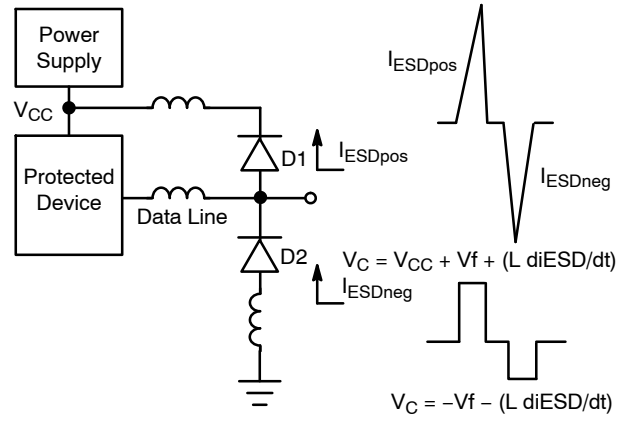
For positive pulse conditions:

$V_c = V_{CC} + V_{fD1}$

For negative pulse conditions:

$V_c = -V_{fD2}$

ESD events can have rise times on the order of some number of nanoseconds. Under these conditions, the effect of parasitic inductance must be considered. A pictorial representation of this is shown below.



An approximation of the clamping voltage for these fast transients would be:

For positive pulse conditions:

$V_c = V_{CC} + Vf + (L\ di_{ESD}/dt)$

For negative pulse conditions:

$V_c = -V_f - (L\ di_{ESD}/dt)$

As shown in the formulas, the clamping voltage (V_c) not only depends on the Vf of the steering diodes but also on the L di_{ESD}/dt factor. A relatively small trace inductance can result in hundreds of volts appearing on the supply rail. This endangers both the power supply and anything attached to that rail. This highlights the importance of good board layout. Taking care to minimize the effects of parasitic inductance will provide significant benefits in transient immunity.

Even with good board layout, some disadvantages are still present when discrete diodes are used to suppress ESD events across datalines and the supply rail. Discrete diodes with good transient power capability will have larger die and therefore higher capacitance. This capacitance becomes problematic as transmission frequencies increase. Reducing capacitance generally requires reducing die size. These small die will have higher forward voltage characteristics at typical ESD transient current levels. This voltage combined with the smaller die can result in device failure.

The ON Semiconductor NUP4114 was developed to overcome the disadvantages encountered when using discrete diodes for ESD protection. This device integrates an ESD diode within a network of steering diodes.

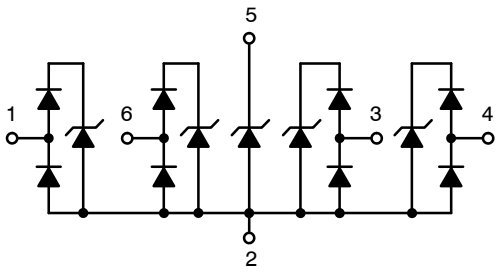
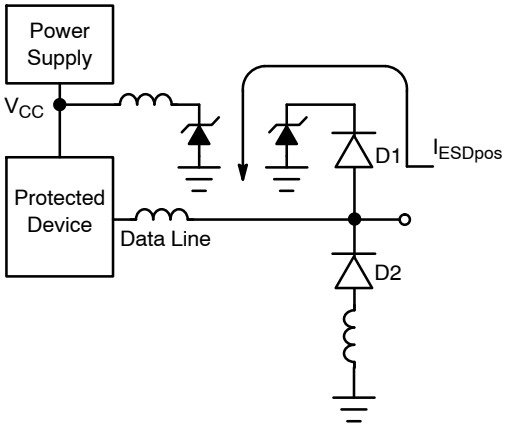


Figure 7. NUP4114 Equivalent Circuit

During an ESD condition, the ESD current will be driven to ground through the ESD diode as shown below.



The resulting clamping voltage on the protected IC will be:

$V_c = V_F + V_{ESD}$.

The clamping voltage of the ESD diode depends on the magnitude of the ESD current. The steering diodes are fast switching devices with unique forward voltage and low capacitance characteristics.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

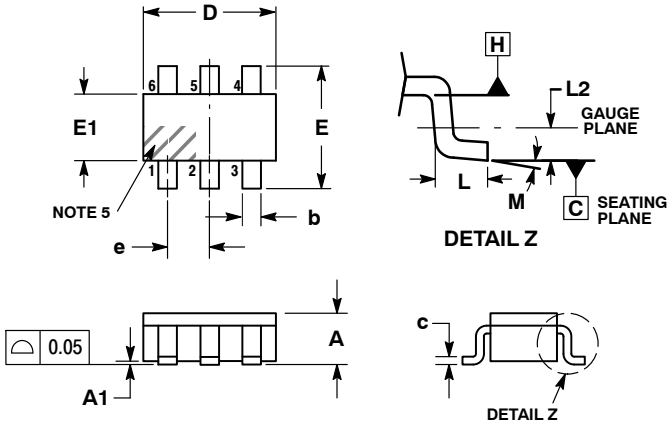
ON Semiconductor®



SCALE 2:1

TSOP−6
CASE 318G−02
ISSUE V

DATE 12 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	–	10°

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

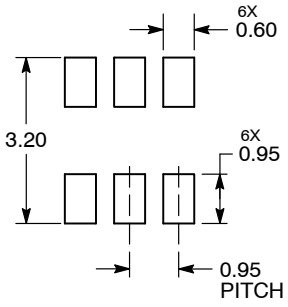
STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

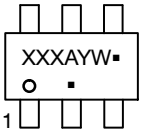
RECOMMENDED SOLDERING FOOTPRINT*



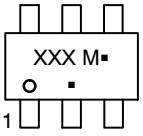
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC



STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present.

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STATUS:	ON SEMICONDUCTOR STANDARD		
NEW STANDARD:			
DESCRIPTION:	TSOP−6		PAGE 1 OF 2

ISSUE	REVISION	DATE
B	ADDED STYLE 2. REQ.BY A. PATEL.	05 MAY 1997
C	ADDED STYLE 3. REQ.BY D. BOLDT, ADDED STYLE 4. REQ.BY UKO.	14 APR 1998
D	ADDED STYLE 5. REQ.BY D. BOLDT.	13 MAY 1998
E	ADDED STYLE 6. REQ.BY M. ATANOVICH.	17 NOV 1999
F	MOTOROLA WAS NOT REMOVED FROM (STATUS) PAGES. PAGES NOT NUMBERED CORRECTLY. REV PAGE WAS MISSING. REQ.BY F. BLAKLEY.	22 NOV 1999
G	ADDED STYLE 7. REQ.BY M. ATANOVICH.	15 DEC 1999
H	ADDED STYLE 8. REQ.BY D. TRUHITTE.	11 MAY 2001
J	ADDED NOTE 4. REQ. BY S. RIGGS.	26 JUN 2003
K	ADDED STYLE 9. REQ.BY S. BACHMAN.	09 SEP 2003
L	ADDED STYLE 10. REQ. BY A. TAM.	25 FEB 2004
M	ADDED STYLE 11 AND 12. REQ. BY L. ROBINSON.	07 JUN 2004
N	CORRECTED STYLE 11, PIN 4 SOURCE 2. REQ. BY C. CHENG .	03 FEB 2005
P	ADDED NOMINAL VALUES AND UPDATED GENERIC MARKING DIAGRAM. REQ. BY HONG XIAO.	27 MAY 2005
R	ADDED STYLE 13. REQ. BY J. CARTER.	09 MAR 2006
S	ADDED STYLE 14. REQ. BY A. SAM.	22 MAR 2006
T	ADDED STYLE 15. REQ. BY S. WINSTON.	06 FEB 2008
U	ADDED DETAIL Z, REMOVED INCH VALUES, ADDED L2, ADDED NOTE 5. REQ. BY J. LETTERMAN.	14 JAN 2010
V	ADDED STYLES 16 & 17. REQ. BY Y. KALDERON.	12 JUN 2012

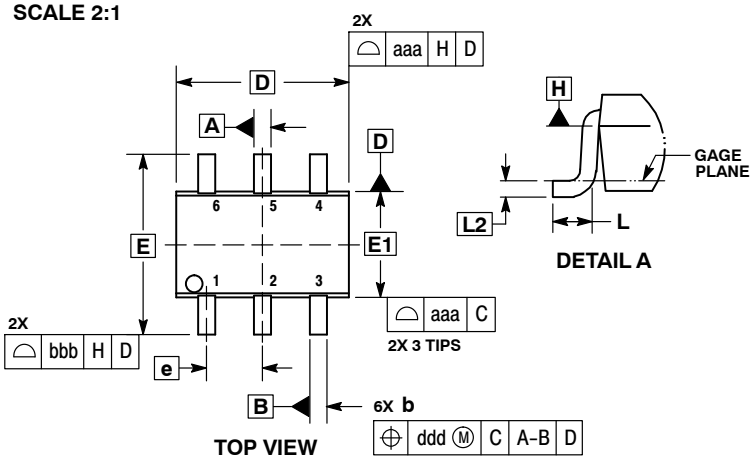
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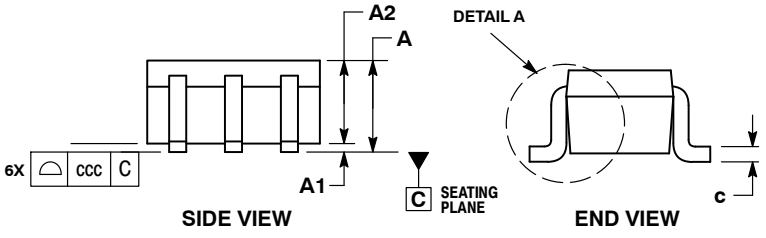
SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012



1
SCALE 2:1

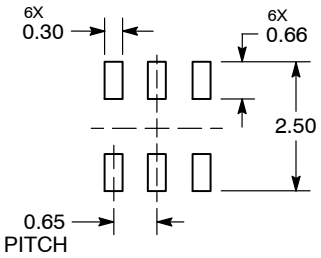




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	−−−	−−−	1.10	−−−	−−−	0.043
A1	0.00	−−−	0.10	0.000	−−−	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

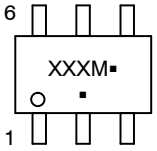
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

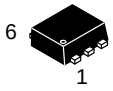
STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

ISSUE	REVISION	DATE
H	REVISION TO CHANGE LEGAL OWNER OF DOCUMENT FROM MOTOROLA TO ON SEMICONDUCTOR. DELETED DIM “V” WAS 0.3 MM–0.4 MM/0.012–0.016 IN. REQ BY G KWONG	14 JUN 01
J	ADDED STYLE 20. REQ BY M. ATANOVICH.	11 OCT 01
K	UPDATED STYLE 15 WAS PIN 1, 2 AND 3: ANODE. PIN 4, 5, AND 6 CATHODE. ADDED STYLE 21. REQ BY M. ATANOVICH	03 APR 02
L	ADDED STYLE 22. REQ BY S. CHANG	25 OCT 02
M	ADDED STYLE 23. REQ BY B. BLACKMON	04 DEC 02
N	ADDED STYLE 24. REQ BY B. BLACKMON	09 JAN 03
P	ADDED STYLE 25. REQ BY S. CHANG	09 MAY 03
R	REMOVED THE “1” AFTER EMITTER. REQ BY S. CHANG	03 JUN 03
S	ADDED STYLE 26. REQ BY A. BINEYARD	18 AUG 03
T	ADDED STYLE 27. REQ. BY M. SWEADOR	23 OCT 2003
U	ADDED STYLES 28 AND 29. REQ. BY A. BINEYARD AND S. BACHMAN	22 JAN 2004
V	ADDED NOM VALUES AND CHANGED DIMS TO INDUSTRY STANDARD. REQ. BY D. TRUHITTE	31 JAN 2005
W	ADDED STYLE 30. REQ. BY L. DELUCA.	26 JAN 2006
Y	UPDATED & REDREW TO JEDEC STANDARDS. REQ. BY D. TRUHITTE.	11 DEC 2012

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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

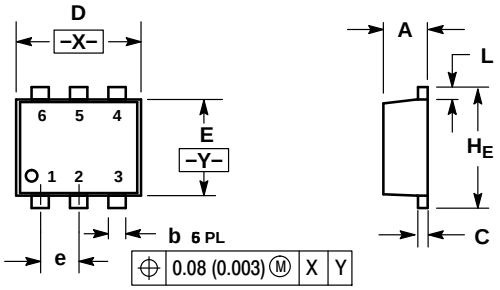
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SCALE 4:1

SOT−563, 6 LEAD
CASE 463A
ISSUE G

DATE 23 SEP 2015



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.021	0.023
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.08	0.12	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.062	0.066
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.5 BSC			0.02 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	1.50	1.60	1.70	0.059	0.062	0.066

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

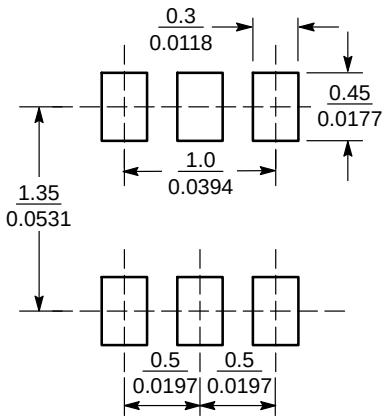
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



SCALE 20:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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STATUS:	**ON SEMICONDUCTOR STANDARD**		
NEW STANDARD:			
DESCRIPTION:	**SOT−563, 6 LEAD**		**PAGE 1 OF 2**

ISSUE	REVISION	DATE
A	ADDED STYLE 5. REQ. BY D. BARLOW.	03 NOV 2003
B	ADDED STYLE 6. REQ. BY M. ATANOVICH.	03 MAR 2004
C	ADDED SYTLE 7. REQ. BY A. TAM.	19 MAR 2004
D	ADDED STYLE 8 AND 9. REQ. K. VAN TYNE.	30 APR 2004
E	ADDED NOM VALUES AND CHANGED DIMS TO INDUSTRY STANDARD. REQ. BY D. TRUHITTE	31 JAN 2005
F	ADDED STYLE 10. REQ. BY M. DEWITT.	28 APR 2005
G	REMOVED −01 FROM CASE CODE VARIANT. REQ. BY N. CALZADA.	23 SEP 2015

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