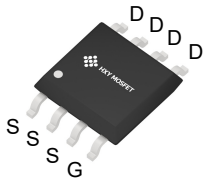
Description

The IRF9335 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

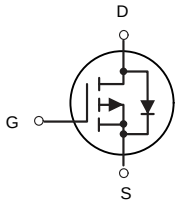


SOP-8
(SOIC-8)

General Features

V_{DS} =-30V I_D = -5.8A

$R_{DS(ON)}$ < 55mΩ @ V_{GS}=10V



P-Channel MOSFET

Application

Battery protection

Load switch

Uninterruptible power supply

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
IRF9335	SOP-8(SOIC-8)	HXY MOSFET	3000

Absolute Maximum Ratings (Tc=25℃ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	- 30	V
VGS	Gate-Source Voltage	±20	V
I_D@T_A=25℃	Drain Current[3], V_{GS} @ 10V	-5.8	A
IDM	Pulsed Drain Current[1]	-20	A
P_D@T_A=25℃	Total Power Dissipation	2.5	W
	Linear Derating Factor	0.02	W/℃
TSTG	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	50	℃/W

Electrical Characteristics (T_A=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-30	-33	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-24V,V_{GS}=0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1	-1.6	-3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-5.1A	-	43	55	mΩ
		V_{GS}=-4.5V, I_D=-4.2A	-	62	90	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-15V,I_D=-4.5A	4	7	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=-15V,V_{GS}=0V, F=1.0MHz	-	520	-	PF
Output Capacitance	C_{oss}		-	130	-	PF
Reverse Transfer Capacitance	C_{rss}		-	70	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-15V, ID=-1A, V_{GS}=-10V,R_{GEN}=6Ω	-	7	-	nS
Turn-on Rise Time	t_r		-	13	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	14	-	nS
Turn-Off Fall Time	t_f		-	9	-	nS
Total Gate Charge	Q_g	V_{DS}=-15V,I_D=-5.1A,V_{GS}=-10V	-	11	-	nC
Gate-Source Charge	Q_{gs}		-	2.2	-	nC
Gate-Drain Charge	Q_{gd}		-	3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-5.1A	-	-	-1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics

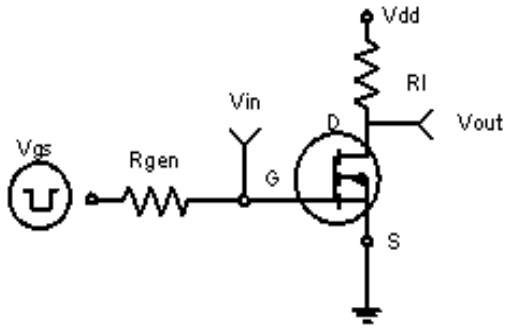


Figure 1:Switching Test Circuit

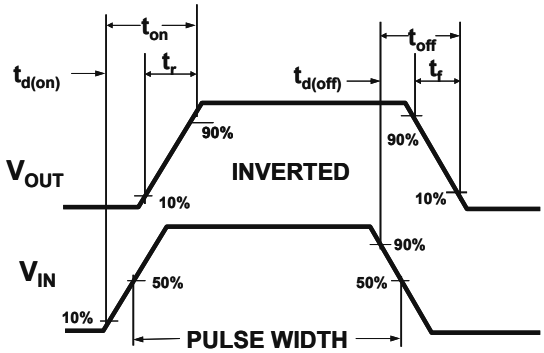


Figure 2:Switching Waveforms

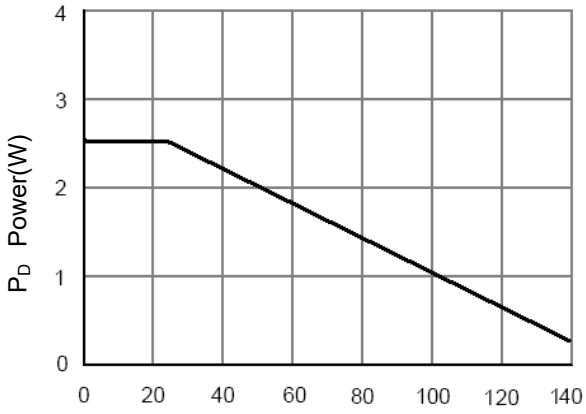


Figure 3 Power Dissipation

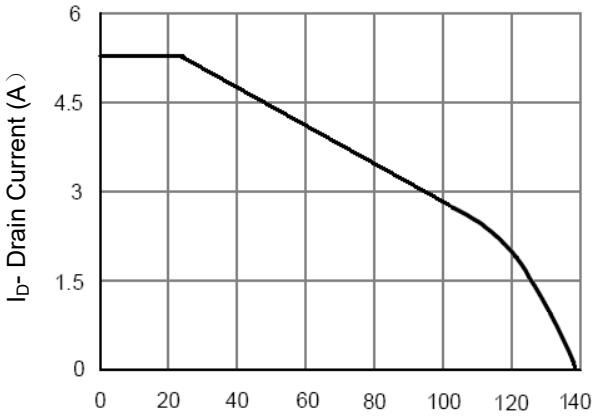


Figure 4 Drain Current

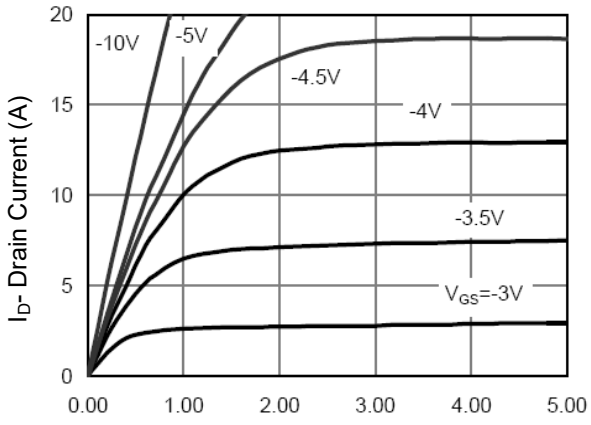


Figure 5 Output Characteristics

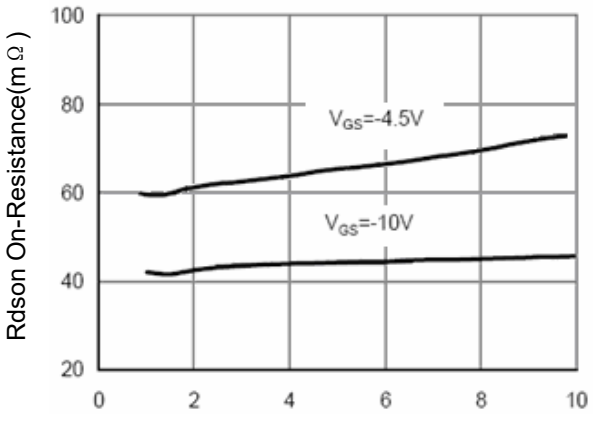
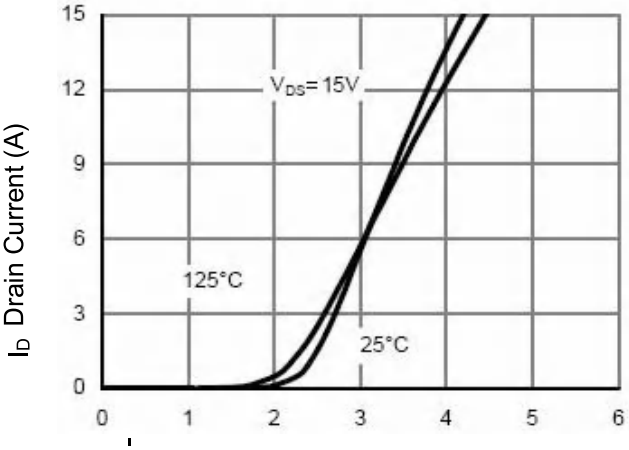


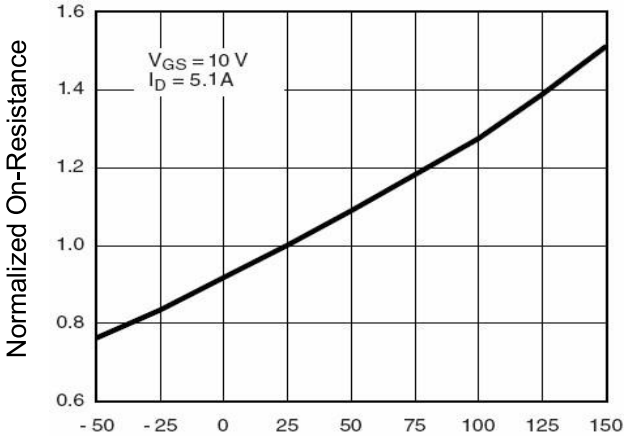
Figure 6 Drain-Source On-Resistance

Figure 5 Output Characteristics



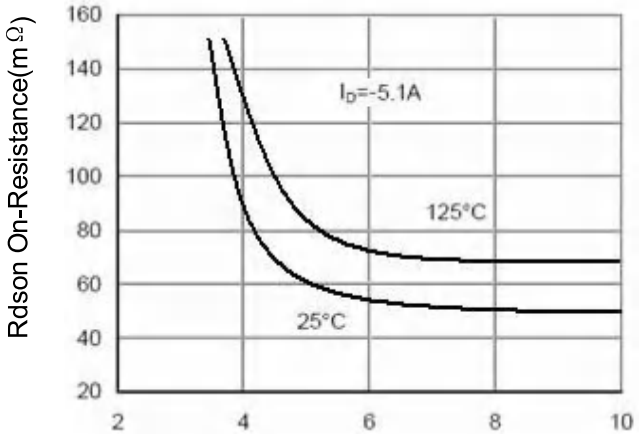
Vgs Gate-Source Voltage (V)

Figure 7 Transfer Characteristics



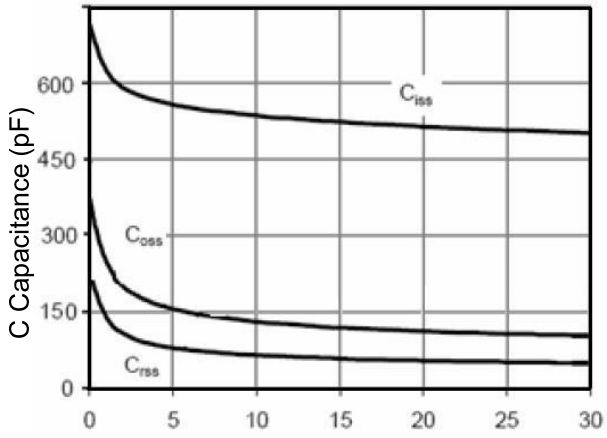
T_J-Junction Temperature(℃)

Figure 8 Drain-Source On-Resistance



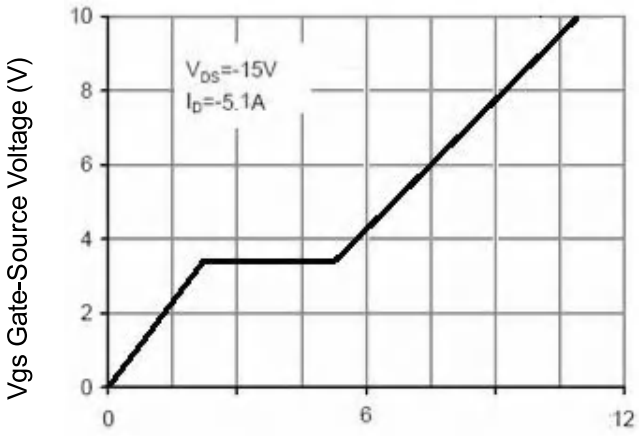
Vgs Gate-Source Voltage (V)

Figure 9 Rdson vs Vgs



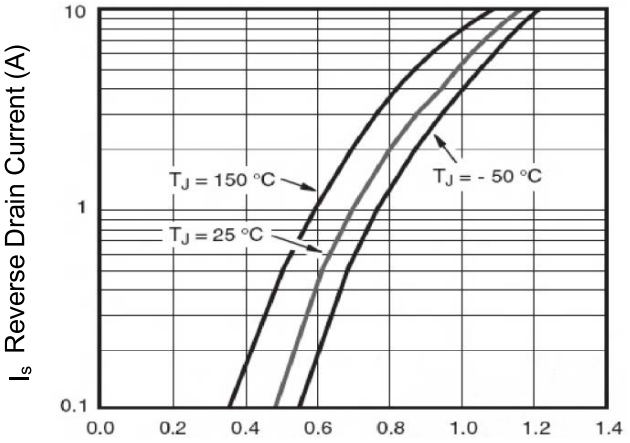
Vds Drain-Source Voltage (V)

Figure 10 Capacitance vs Vds



Qg Gate Charge (nC)

Figure 11 Gate Charge



Vsd Source-Drain Voltage (V)

Figure 12 Source- Drain Diode Forward

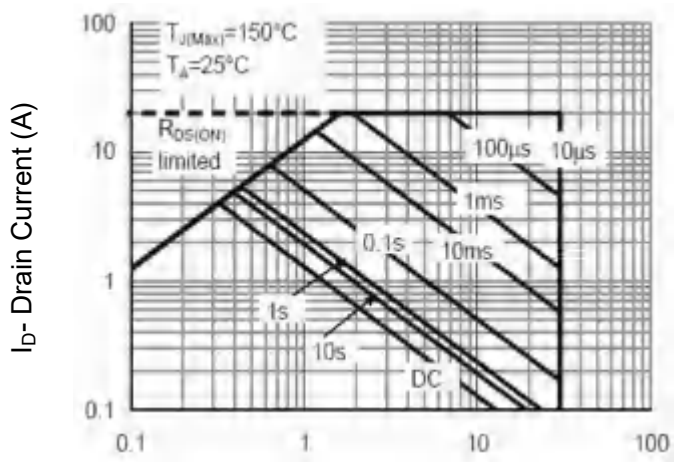


Figure 13 Safe Operation Area

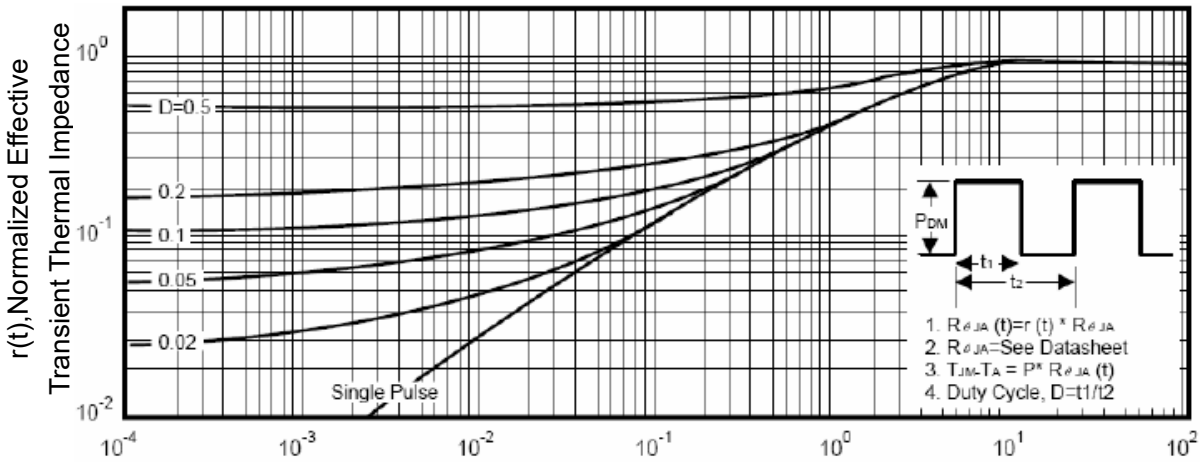
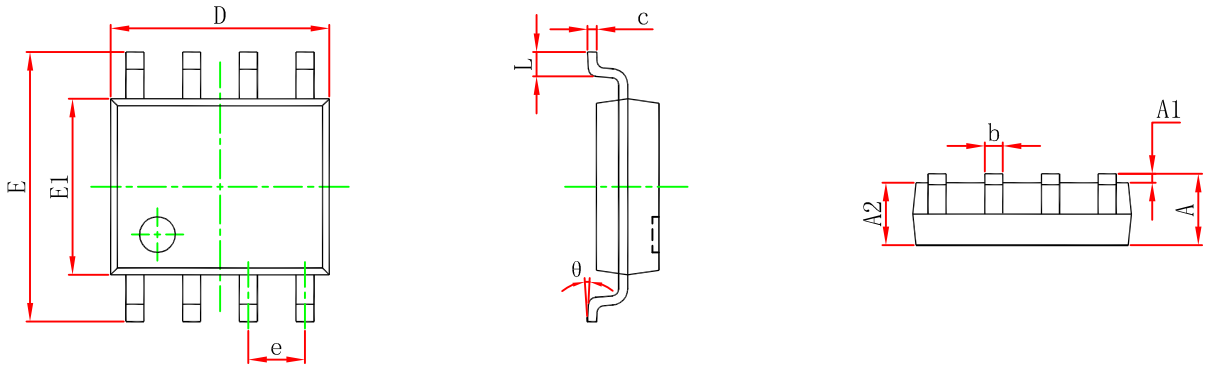
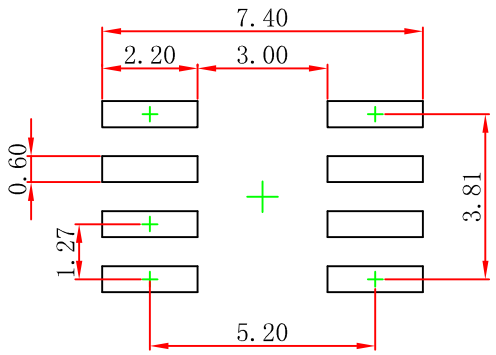


Figure 14 Normalized Maximum Transient Thermal Impedance

SOP-8(SOIC-8) Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

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