LM5066I 10 to 80 V, Hotswap Controller With I/V/P Monitoring and PMBus™ Interface

1 Features

- 10- to 80-V Operation
- 100-V Continuous Absolute Max
- 26 mV or 50 mV ILIM Threshold (±10%)
- Programmable FET SOA Protection
- Programable UV, OV, t_{FAULT} Thresholds
- External FET Temperature Sensing
- Failed FET Detection
- I^2C / SMBus Interface
- PMBus™ and Node Manager 2.0 and 3.0 Compliant Command Structure
- Precision V_{IN}, V_{OUT}, I_{IN}, P_{IN}, V_{AUX} Monitoring
  - V (±1.25%); I (±1.75%); P (±2.5%)
- Supports Energy Monitoring via Read_EIN Command
- Programable I/V/P Averaging Interval
- 12-bit ADC with 1-kHz Sampling Rate
- –40°C < T_J < 125°C Operation

2 Applications

- 48-V Servers
- Base Station Power Distribution
- Networking Routers and Switchers
- PLC Power Management
- 24- to 28-V Industrial Systems

3 Description

LM5066I provides robust protection and precision monitoring for 10- to 80-V systems. Programmable UV, OV, I_{LIMIT}, and fast-short circuit protection allow for customized protection for any application. Programmable FET SOA protection sets the maximum power the FET is allowed to dissipate under any condition. The programmable fault timer (t_{FAULT}) is set to avoid nuisance trips, ensure start-up, and limit the duration of over load events.

In addition to circuit protection, the LM5066I supplies real-time power, voltage, current, temperature, and fault data to the system management host through the I^2C / SMBus interface. PMBus compliant command structure makes it easy to program the device. Precision telemetry enables intelligent power management functions such as efficiency optimization and early fault detection. LM5066I also supports advanced features such as I/V/P averaging and peak power measurment to improve system diagnostics.

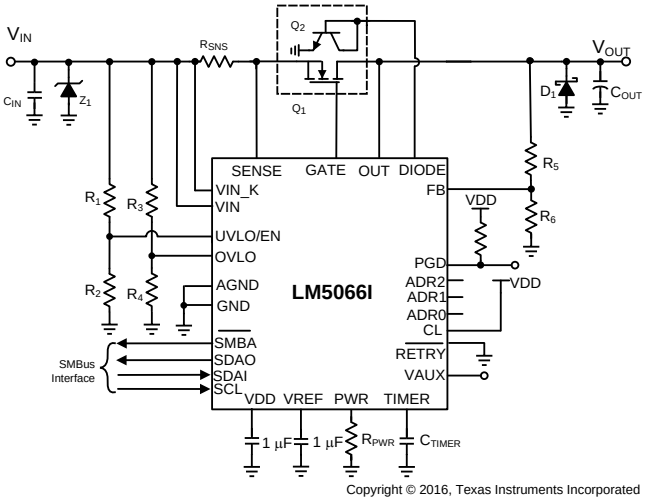
LM5066I is pin-to-pin compatible with the LM5066 and offers improved telemetry accuracy and supports the Read_Ein command to monitor energy. See Table 1 for a detailed comparison.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5066I	PWP (28)	9.70 × 4.40 mm²

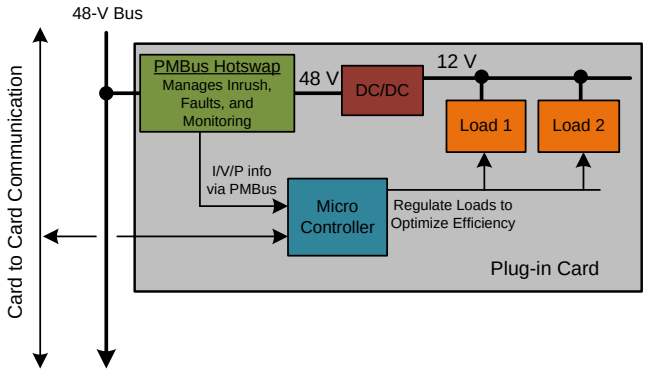
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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LM5066I in a Plug-in Card



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2015) to Revision C — **Page**

- Changed V_{GATEZ} MIN value from "15 V" to "12 V" ... 7

Changes from Revision A (May 2014) to Revision B — **Page**

- Added Absolute Maximum Ratings table. ... 5
- Changed title of Handling Ratings table to ESD Ratings table ... 5

Changes from Original (April 2014) to Revision A — **Page**

- Added new sections ... 1

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5 Device Comparison Table

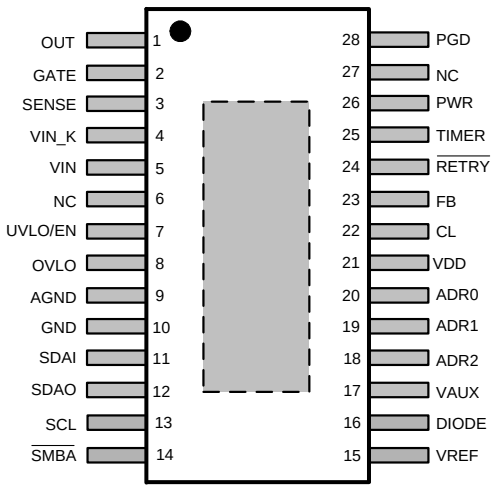
Table 1 summarizes the differences between the LM5066 and the LM5066I. Note that the current monitoring accuracy of the LM5066I is much better at the ILIM = 26 mV setting, but is comparable at the 50-mV setting. For many applications with lower power, using the LM5066 at the 50-mV setting is a great option. However, for higher power applications upgrading to LM5066I and using the ILIM = 26 mV setting will lead to significant power savings (approximately 24 mV × I_{LOAD}). In addition, the higher accuracy and energy monitoring capability can enable further improvements in system efficiency, which is critical in high power applications.

Table 1. LM5066 vs LM5066I

KEY PARAMETERS	LM5066	LM5066I
Voltage monitoring	±2.7%	±1.25%
Current monitoring (ILIM = 26 mV)	±4.25%	±1.75%
Power monitoring (ILIM = 26 mV)	±4.5%	±.2.5%
Current monitoring (ILIM = 50 mV)	±3%	±3.5%
Power monitoring (ILIM = 50 mV)	±4.5%	±4.5%
Supports Energy Monitoring via Read_EIN command	No	Yes

6 Pin Configuration and Functions

PWP Package
28-Pin
Top View



Solder exposed pad to ground.

Pin Functions

PIN		DESCRIPTION
NAME	NO.	
Exposed Pad	Pad	Exposed pad of TSSOP package Solder to the ground plane to reduce thermal resistance
OUT	1	Output feedback Connect to the output rail (external MOSFET source). Internally used to determine the MOSFET V_{DS} voltage for power limiting and to monitor the output voltage.
GATE	2	Gate drive output Connect to the external MOSFET's gate.
SENSE	3	Current sense input The voltage across the current sense resistor (R_{SNS}) is measured from VIN_K to this pin. If the voltage across R_{SNS} reaches overcurrent threshold the load current is limited and the fault timer activates.

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Pin Functions (continued)

PIN		DESCRIPTION
NAME	NO.	
VIN_K	4	Positive supply Kelvin pin The input voltage is measured on this pin.
VIN	5	Positive supply input This pin is the input supply connection for the device.
N/C	6	No connection
UVLO/EN	7	Undervoltage lockout An external resistor divider from the system input voltage sets the undervoltage turn-on threshold. An internal 20-µA current source provides hysteresis. The enable threshold at the pin is nominally 2.48 V. This pin can also be used for remote shutdown control.
OVLO	8	Overvoltage lockout An external resistor divider from the system input voltage sets the overvoltage turn-off threshold. An internal 21-µA current source provides hysteresis. The disable threshold at the pin is 2.46 V.
AGND	9	Circuit ground Analog device ground. Connect to GND at the pin.
GND	10	Circuit ground
SDAI	11	SMBus data input pin Data input pin for SMBus. Connect to SDAO if the application does not require unidirectional isolation devices.
SDAO	12	SMBus data output pin Data output pin for SMBus. Connect to SDAI if the application does not require unidirectional isolation devices.
SCL	13	SMBus clock Clock pin for SMBus
$\overline{\text{SMBA}}$	14	SMBus alert line Alert pin for SMBus, active low
VREF	15	Internal reference Internally generated precision reference used for analog-to-digital conversion. Connect a 1-µF capacitor on this pin to ground for bypassing.
DIODE	16	External diode Connect this to a diode-configured MMBT3904 NPN transistor for temperature monitoring.
VAUX	17	Auxiliary voltage input Auxiliary pin allows voltage telemetry from an external source. Full-scale input of 2.97 V.
ADR2	18	SMBUS address line 2 Tri-state address line. Should be connected to GND, VDD, or left floating.
ADR1	19	SMBUS address line 1 Tri-state address line. Should be connected to GND, VDD, or left floating.
ADR0	20	SMBUS address line 0 Tri-state address line. Should be connected to GND, VDD, or left floating.
VDD	21	Internal sub-regulator output Internally sub-regulated 4.85-V bias supply. Connect a 1-µF capacitor on this pin to ground for bypassing.
CL	22	Current limit range Connect this pin to GND or leave floating to set the nominal over-current threshold at 50 mV. Connecting CL to VDD sets the overcurrent threshold to be 26 mV.
FB	23	Power Good feedback An external resistor divider from the output sets the output voltage at which the PGD pin switches. The threshold at the pin is nominally 2.46 V. An internal 20-µA current source provides hysteresis.
$\overline{\text{RETRY}}$	24	Fault retry input This pin configures the power up fault retry behavior. When this pin is connected to GND or left floating, the device will continually try to engage power during a fault. If the pin is connected to VDD, the device will latch off during a fault.
TIMER	25	Timing capacitor An external capacitor connected to this pin sets insertion time delay, fault timeout period, and restart timing.
PWR	26	Power limit set An external resistor connected to this pin, in conjunction with the current sense resistor (R_{SNS}), sets the maximum power dissipation allowed in the external series pass MOSFET.
N/C	27	No connection

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Pin Functions (continued)

PIN		DESCRIPTION
NAME	NO.	
PGD	28	Power Good indicator An open-drain output. This output is high when the voltage at the FB pin is above V_{FBTH} (nominally 2.46 V) and the input supply is within its undervoltage and overvoltage thresholds. Connect to the output rail (external MOSFET source) or any other voltage to be monitored.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN, VIN_K, GATE, UVLO/EN, SENSE, PGD to GND (2)	–0.3	100	V
	OVLO, FB, TIMER, PWR to GND	–0.3	7	
	OUT to GND	–0.3	100	
	SCL, SDAI, SDAO, CL, ADR0, ADR1, ADR2, VDD, VAUX, DIODE, $\overline{\text{RETRY}}$ to GND	–0.3	6	
	SENSE to VIN_K, VIN to VIN_K, AGND to GND	–0.3	0.3	
Junction temperature			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The GATE pin voltage is typically 13.6 V above VIN when the LM5066I is enabled. Therefore, the Absolute Maximum Rating for VIN applies only when the LM5066I is disabled, or for a momentary surge to that voltage because the Absolute Maximum Rating for the GATE pin is also 100 V.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD} (1)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins except GATE(2)	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(3)	±500	V

(1) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. 2-kV rating for all pins except GATE which is rated for 1 kV.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VIN, SENSE, OUT voltage	10		80	V
Junction temperature	–40		125	°C

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7.4 Thermal Information

THERMAL METRIC[1]		LM5066I PWP 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	35.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance[3]	19.9	
$R_{\theta JB}$	Junction-to-board thermal resistance[4]	16.8	
ψ_{JT}	Junction-to-top characterization parameter[5]	0.5	
ψ_{JB}	Junction-to-board characterization parameter[6]	16.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance[7]	2.9	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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7.5 Electrical Characteristics

Unless otherwise stated, the following conditions apply: V_{VIN} = 48 V, –40°C < T_J < 125°C, V_{UVLO} = 3 V , V_{OVLO} = 0 V, R_{PWR}= 20 kΩ. See (1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT (VIN PIN)						
I_{IN-EN}	Input current, enabled	V_{UVLO} = 3 V and V_{OVLO} = 2 V		5.6	7	mA
POR_{IT}	Power-on reset threshold at V_{VIN} to trigger insertion timer	V_{VIN} increasing		7.8	9.0	V
POR_{EN}	Power-on reset threshold at V_{VIN} to enable all functions	V_{VIN} increasing		8.6	9.9	V
POR_{HYS}	POR_{EN} hysteresis	V_{VIN} decreasing		100		mV
VDD REGULATOR (VDD PIN)						
V_{DD}		I_{VDD} = 0 mA	4.60	4.90	5.15	V
		I_{VDD} = 10 mA	4.60	4.85	5.15	V
V_{DDILIM}	V_{VDD} current limit		–50	–30	–15	mA
V_{DDPOR}	V_{VDD} voltage reset threshold	V_{VDD} rising		4.1		V
UVLO/EN, OVLO PINS						
$UVLO_{TH}$	UVLO threshold	V_{UVLO} falling	2.41	2.48	2.55	V
$UVLO_{HYS}$	UVLO hysteresis current	V_{UVLO} = 1 V	16	20	24	µA
$UVLO_{BIAS}$	UVLO bias current	V_{UVLO} = 3 V			1	µA
$OVLO_{TH}$	OVLO threshold	V_{OVLO} rising	2.39	2.46	2.53	V
$OVLO_{HYS}$	OVLO hysteresis current	V_{OVLO}= 1 V	–24	–21	–16	µA
$OVLO_{BIAS}$	OVLO bias current	V_{OVLO} = 1 V			1	µA
POWER GOOD (PGD PIN)						
PGD_{VOL}	Output low voltage	I_{SINK} = 2 mA		100	400	mV
PGD_{IOH}	Off leakage current	V_{PGD} = 80 V			1	µA
FB PIN						
FB_{TH}	FB threshold	V_{UVLO} = 3 V and V_{OVLO} = 2 V	2.41	2.46	2.52	V
FB_{HYS}	FB hysteresis current		–25	–20	–15	µA
FB_{LEAK}	Off leakage current	V_{FB} = 2.3 V			1	µA
POWER LIMIT (PWR PIN)						
	Power limit sense voltage (V_{VIN_K} – V_{SENSE})	V_{SENSE} – V_{OUT} = 48 V, R_{PWR} = 60 kΩ	7.4	9.4	11.4	mV
		V_{SENSE} – V_{OUT} = 48 V, R_{PWR} = 20 kΩ	1.5	3.5	5.7	mV
		V_{SENSE} – V_{OUT} = 48 V, R_{PWR} = 20 kΩ, T_J = 0°C to 85°C	1.85	3.5	5.02	mV
		V_{SENSE} – V_{OUT} = 24 V, R_{PWR} = 60 kΩ	15	18.75	22.5	mV
		V_{SENSE} – V_{OUT} = 24 V, R_{PWR} = 20 kΩ	5	7.23	10	mV
I_{PWR}	PWR pin current	V_{PWR} = 2.5 V		-20		µA
$R_{SAT(PWR)}$	PWR pin impedance when disabled	V_{UVLO} = 2 V		120		Ω
GATE CONTROL (GATE PIN)						
I_{GATE}	Source current	Normal operation	–40	–20	–7.5	µA
	Fault sink current	V_{UVLO} = 2 V	3.4	4.2	5.3	mA
	POR circuit breaker sink current	V_{VIN_K} – V_{SENSE} = 60 mV or V_{VIN} < POR_{IT}, V_{GATE} = 5 V, OUT = 0 V, CB/CL ratio bit = 0, CL = 1	90	160	230	mA
V_{GATEZ}	Reverse-bias voltage of GATE to OUT Zener diode, I_Z = –100 µA	V_{GATE}– V_{OUT}	12	16.5	18	V
V_{GATECP}	Peak charge pump voltage in normal operation (V_{IN} = V_{OUT})	V_{GATE}– V_{OUT}	11	13	15	V
OUT PIN						
I_{OUT-EN}	OUT bias current, enabled	V_{IN} = V_{OUT}, normal operation	60	80	100	µA
$I_{OUT-DIS}$	OUT bias current, disabled (2)	Disabled, OUT = 0 V, V_{VIN_K} = V_{SENSE}	–65	–50	–35	µA

(1) Current out of a pin is indicated as a negative value.
(2) OUT bias current (disabled) due to leakage current through an internal 1-MΩ resistance from SENSE to VOUT.

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Electrical Characteristics (continued)

Unless otherwise stated, the following conditions apply: V_{VIN} = 48 V, –40°C < T_J < 125°C, V_{UVLO} = 3 V , V_{OVLO} = 0 V, R_{PWR}= 20 kΩ. See (1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
V_{CL}	Current limit threshold voltage (V_{VIN_K} – V_{SENSE})	CL = VDD	23.4	26	28.6	mV
		CL = GND	45	50	55	
I_{SENSE}	SENSE input current	Enabled, SENSE = OUT	20	25	35	µA
		Disabled, OUT = 0 V		66		
		Enabled, OUT = 0 V	190	220	250	
CIRCUIT BREAKER						
RT_{CB}	Circuit breaker to current limit ratio: (V_{VIN_K} – V_{SENSE})$_{CB}$/V_{CL}	CB/CL ratio bit = 0, ILIM = 50 mV	1.64	1.94	2.23	V/V
		CB/CL ratio bit = 1, ILIM = 50 mV	3.28	3.87	4.45	
		CB/CL ratio bit = 0, ILIM = 26 mV	1.5	1.88	2.3	
		CB/CL ratio bit = 1, ILIM = 26 mV	3.1	3.75	4.45	
V_{CB}	Circuit breaker threshold voltage: (V_{VIN_K} – V_{SENSE})	CB/CL ratio bit = 0, ILIM = 50 mV	76	96	116	mV
		CB/CL ratio bit = 1, ILIM = 50 mV	155	193	235	
		CB/CL ratio bit = 0, ILIM = 26 mV	38	48	58	
		CB/CL ratio bit = 1, ILIM = 26 mV	76	96	116	
TIMER (TIMER PIN)						
V_{TMRH}	Upper threshold		3.74	3.9	4.07	V
V_{TMRL}	Lower threshold	Restart cycles	1	1.2	1.4	V
		End of eighth cycle re-enable threshold		0.3		V
I_{TIMER}	Insertion time current	TIMER pin = 2 V	–5.9	–4.8	–3.3	µA
	Sink current, end of insertion time		0.9	1.5	2.1	mA
	Fault detection current		–90	–75	–60	µA
	Fault sink current		1.7	2.5	3.2	µA
DC_{FAULT}	Fault restart duty cycle			0.5%		
INTERNAL REFERENCE						
V_{REF}	Reference voltage		2.93	2.97	3.02	V
ADC AND MUX						
	Resolution			12		Bits
INL	Integral non-linearity	ADC only		±4		LSB
$t_{ACQUIRE}$	Acquisition + conversion time	Any channel		100		µs
t_{RR}	Acquisition round robin time	Cycle all channels		1		ms
TELEMETRY ACCURACY						
I_{INFSR}	Current input full-scale range	CL = GND	50	54.4	58	mV
		CL = VDD	26	27.0	29	mV
I_{INLSB}	Current input LSB	CL = GND		13.30		µV
		CL = VDD		6.70		µV
V_{AUXFSR}	VAUX input full-scale range		2.93	2.97	3.01	V
V_{AUXLSB}	VAUX input LSB			725		µV
V_{INFSR}	Input voltage full-scale range		86	88.9	91	V
V_{INLSB}	Input voltage LSB			21.7		mV
V_{OUTFSR}	Output voltage full-scale range		86	88.9	91	V
V_{OUTLSB}	Output voltage LSB			21.7		mV
I_{INACC}	Input current absolute accuracy	V_{VIN_K} – V_{SENSE} = 22 mV (80% I_{INFSR}), CL = VDD	–1.75	%	+1.75	
		V_{VIN_K} – V_{SENSE} = 5 mV (19% I_{INFSR}), CL = VDD	–6.0	%	+6.0	
		V_{VIN_K} – V_{SENSE} = 44 mV (80% I_{INFSR}), CL = GND	–3.5	%	+3.5	

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Electrical Characteristics (continued)

Unless otherwise stated, the following conditions apply: V_{VIN} = 48 V, –40°C < T_J < 125°C, V_{UVLO} = 3 V , V_{OVLO} = 0 V, R_{PWR}= 20 kΩ. See (1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ACC}	VIN, VOUT absolute accuracy	V_{VIN}, V_{VOUT} = 48, 80 V	–1.25	%	+1.25	
		V_{VIN}, V_{VOUT} = 10 V	–2.5	%	+2.5	
	VAUX absolute accuracy	V_{AUX} = 2.8 V	–1.25	%	+1.25	
P_{INACC}	Input power accuracy	V_{VIN} = 48 V, V_{VIN_K} – V_{SENSE} = 22 mV (80% I_{INFSR}), CL = VDD	–2.5	%	+2.5	
		V_{VIN} = 48 V, V_{VIN_K} – V_{SENSE} = 5 mV (19% I_{INFSR}), CL = VDD	–6.5	%	+6.5	
		V_{VIN} = 48V , V_{VIN_K} – V_{SENSE}= 44 mV (80% I_{INFSR}), CL = GND	–4.5	%	+4.5	
REMOTE DIODE TEMPERATURE SENSOR						
T_{ACC}	Temperature accuracy using local diode	T_A = 25°C to 85°C		2	10	°C
	Remote diode resolution			9		bits
I_{DIODE}	External diode current source	High level		250	325	µA
		Low level		9.4		µA
	Diode current ratio			25.9		µA
PMBus PIN THRESHOLDS ($\overline{SMBA}$, SDA, SCL)						
V_{IL}	Data, clock input low voltage				0.9	V
V_{IH}	Data, clock input high voltage		2.1		5.5	V
V_{OL}	Data output low voltage	I_{SINK} = 3 mA	0		0.4	V
I_{LEAK}	Input leakage current	SDAI,$\overline{SMBA}$,SCL = 5 V			1	µA
CONFIGURATION PIN THRESHOLDS (CL, $\overline{RETRY}$)						
V_{IH}	Threshold voltage		3			V
I_{LEAK}	Input leakage current	CL, $\overline{RETRY}$ = 5 V		5		µA

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7.6 SMBus Communications Timing Requirements and Definitions

PARAMETER		MIN	MAX	UNIT
f_{SMB}	SMBus operating frequency	10	400	kHz
t_{BUF}	Bus free time between stop and start condition	1.3		µs
$t_{HD:STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated.	0.6		µs
$t_{SU:STA}$	Repeated start condition setup time	0.6		µs
$t_{SU:STO}$	Stop condition setup time	0.6		µs
$t_{HD:DAT}$	Data hold time	85		ns
$t_{SU:DAT}$	Data setup time	100		ns
$t_{TIMEOUT}$	Clock low time-out (1)	25	35	ms
t_{LOW}	Clock low period	1.5		µs
t_{HIGH}	Clock high period (2)	0.6		µs
$t_{LOW:SEXT}$	Cumulative clock low extend time (slave device) (3)		25	ms
$t_{LOW:MEXT}$	Cumulative low extend time (master device) (4)		10	ms
t_F	Clock or data fall time (5)	20	300	ns
t_R	Clock or data rise time (5)	20	300	ns

(1) Devices participating in a transfer will timeout when any clock low exceeds the value of $t_{TIMEOUT,MIN}$ of 25 ms. Devices that have detected a timeout condition must reset the communication no later than $t_{TIMEOUT,MAX}$ of 35 ms. The maximum value must be adhered to by both a master and a slave as it incorporates the cumulative stretch limit for both a master (10 ms) and a slave (25 ms).
(2) $t_{HIGH\ MAX}$ provides a simple method for devices to detect bus idle conditions.
(3) $t_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to the stop. If a slave exceeds this time, it is expected to release both its clock and data lines and reset itself.
(4) $t_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from start-to-ack, ack-to-ack, or ack-to-stop.
(5) Rise and fall time is defined as follows: t_R = (V_{ILMAX} – 0.15) to (V_{IHMIN} + 0.15); t_F = 0.9 VDD to (V_{ILMAX} – 0.15)

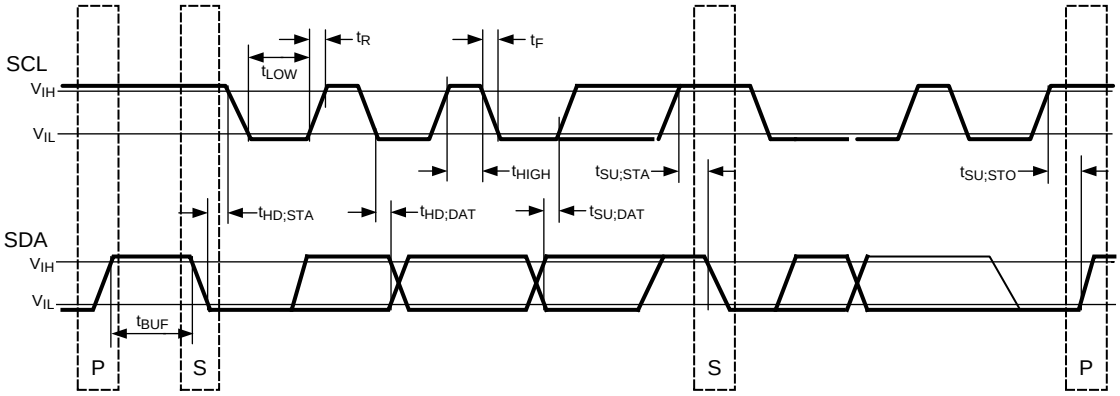


Figure 1. SMBus Timing Diagram

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7.7 Switching Characteristics

Unless otherwise stated, the following conditions apply: V_{VIN} = 48 V, –40°C < T_J < 125°C, V_{UVLO} = 3 V , V_{OVLO} = 0 V, R_{PWR}= 20 kΩ.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
UVLO/EN, OVLO PINS						
$UVLO_{DEL}$	UVLO delay	Delay to GATE high	7	9.6	12.2	µs
		Delay to GATE low	6	8.5	11	
$OVLO_{DEL}$	OVLO delay	Delay to GATE high	7	9.6	12.2	µs
		Delay to GATE low	6	8.5	11	
FB PIN						
FB_{DEL}	FB Delay	Delay to PGD high	5	7.6	10	µs
		Delay to PGD low	7	9.2	12.5	
CURRENT LIMIT						
t_{CL}	Response time	VIN-SENSE stepped from 0 to 80 mV; CL = GND		30	50	µs
CIRCUIT BREAKER						
t_{CB}	Response time	VIN-SENSE stepped from 0 to 150 mV, time to GATE low, no load		0.36	0.8	µs
TIMER (TIMER PIN)						
t_{FAULT_DELAY}	Fault to GATE low delay	TIMER pin reaches the upper threshold		12		µs

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7.8 Typical Characteristics

Unless otherwise specified, the following conditions apply: T_J = 25°C, V_{IN} = 48 V. All graphs show junction temperature.

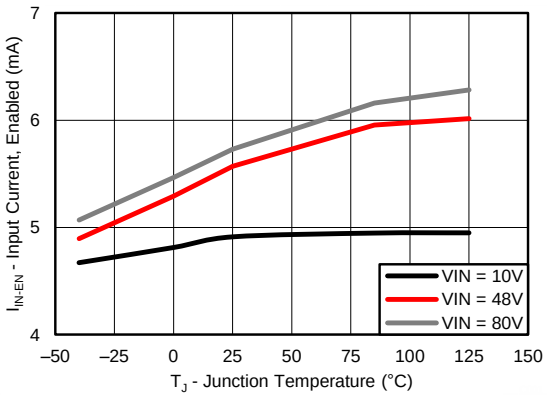


Figure 2. Input Current vs VIN and T_J

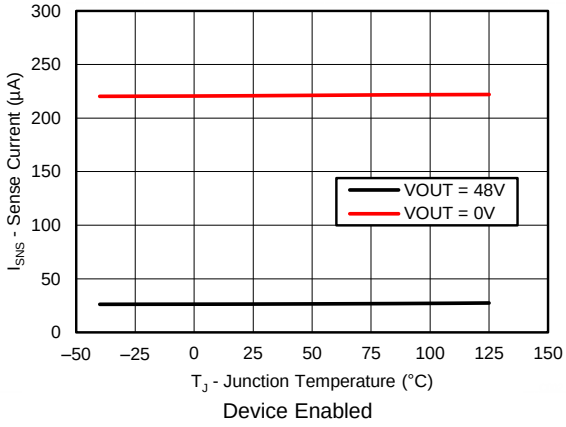


Figure 3. Sense Current vs VOUT and T_J

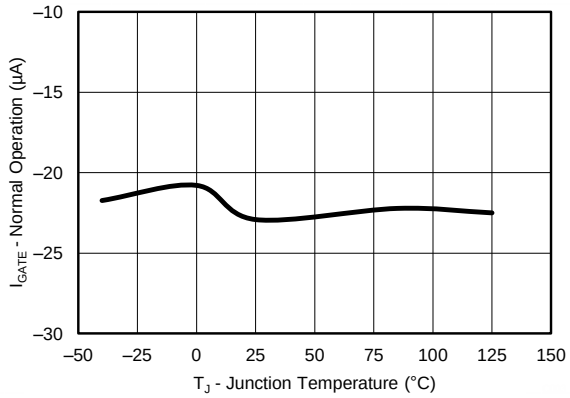


Figure 4. Gate Sourcing Current vs T_J

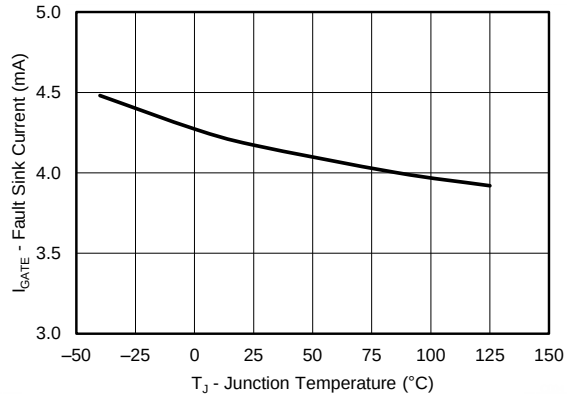


Figure 5. Gate Sinking Current vs T_J

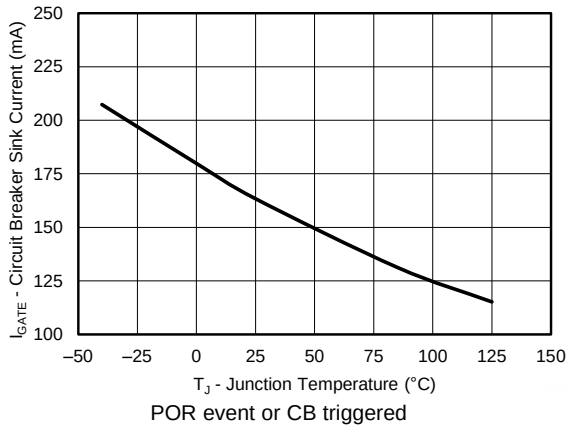


Figure 6. Gate Sinking Current vs T_J

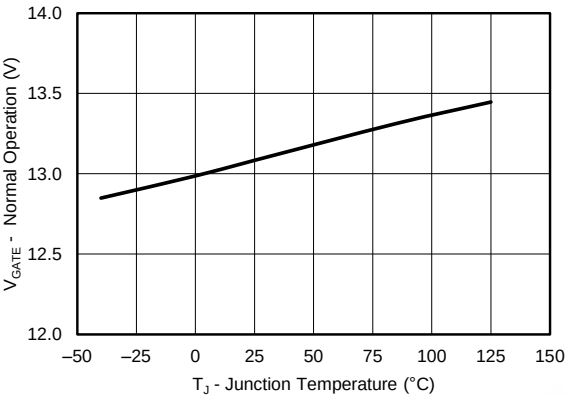
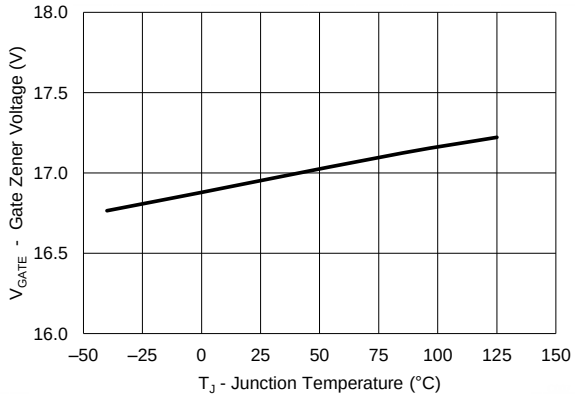


Figure 7. Gate Voltage vs T_J

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: T_J = 25°C, V_{IN} = 48 V. All graphs show junction temperature.



Inject 100 µA into gate node. Measure GATE-SOURCE

Figure 8. Gate Clamping Voltage vs T_J

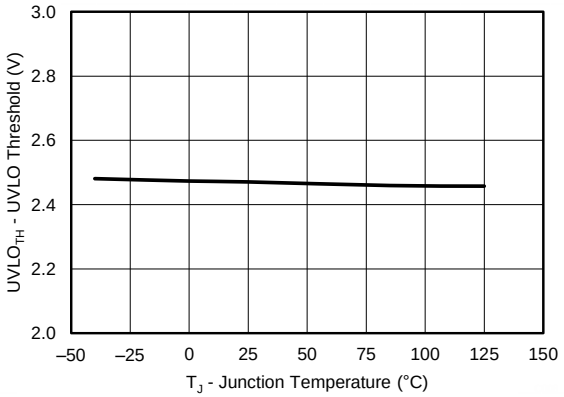


Figure 9. UVLO/EN Threshold vs T_J

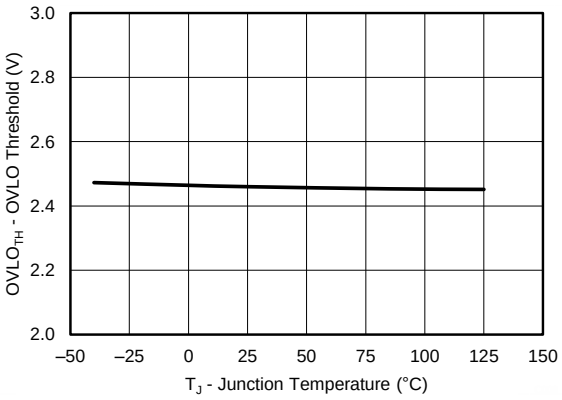


Figure 10. OVLO Threshold vs T_J

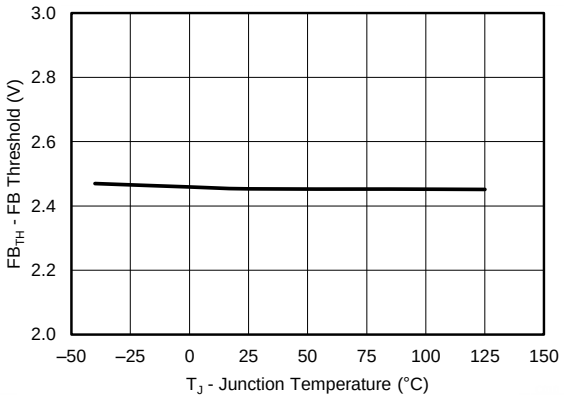


Figure 11. Power Good Feedback Threshold vs T_J

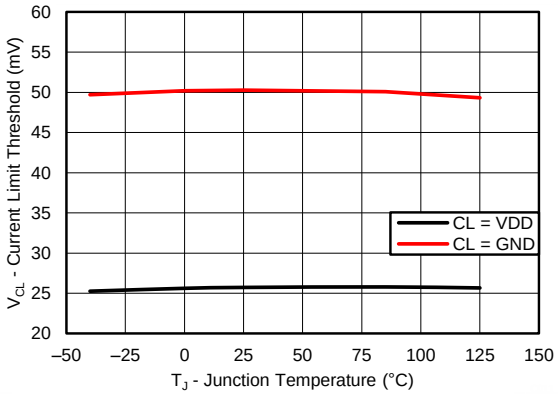


Figure 12. Current Limit Threshold vs T_J

8 Detailed Description

8.1 Overview

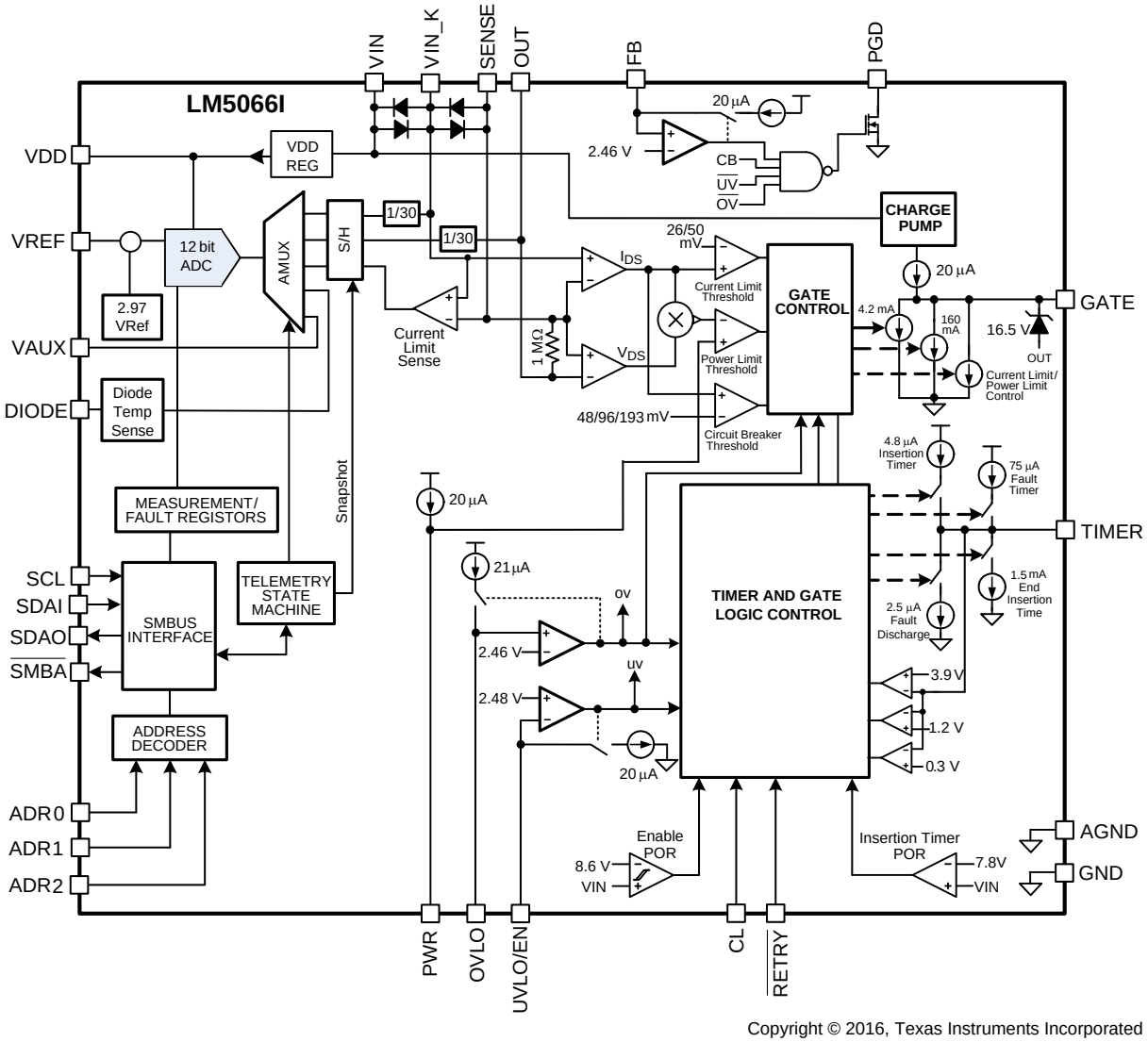
The inline protection functionality of the LM5066I is designed to control the in-rush current to the load after insertion of a circuit card into a live backplane or other “hot” power source, thereby limiting the voltage sag on the backplane’s supply voltage and the dV/dt of the voltage applied to the load. The effects on other circuits in the system are minimized by preventing possible unintended resets. When the circuit card is removed, a controlled shutdown can be implemented using the LM5066I.

In addition to a programmable current limit, the LM5066I monitors and limits the maximum power dissipation in the series-pass device to maintain operation within the device safe operating area (SOA). Either current limiting or power limiting for an extended period of time results in the shutdown of the series-pass device. In this event, the LM5066I can latch off or repetitively retry based on the hardware setting of the $\overline{\text{RETRY}}$ pin. When started, the number of retries can be set to none, 1, 2, 4, 8, 16, or infinite. The circuit breaker function quickly switches off the series-pass device upon detection of a severe overcurrent condition. Programmable undervoltage lockout (UVLO) and overvoltage lockout (OVLO) circuits shut down the LM5066I when the system input voltage is outside the desired operating range.

The telemetry capability of the LM5066I provides intelligent monitoring of the input voltage, output voltage, input current, input power, temperature, and an auxiliary input. The LM5066I also provides a peak capture of the input power and programmable hardware averaging of the input voltage, current, power, and output voltage. Warning thresholds which trigger the $\overline{\text{SMBA}}$ pin may be programmed for input and output voltage, current, power, and temperature through the PMBus interface. Additionally, the LM5066I is capable of detecting damage to the external MOSFET, Q_1.

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8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Current Limit

The current limit threshold is reached when the voltage across the sense resistor R_{SNS} (VIN_K to SENSE) exceeds the ILIM threshold (26 mV if CL = VDD and 50 mV if CL = GND). In the current limiting condition, the GATE voltage is controlled to limit the current in MOSFET Q_1. While the current limit circuit is active, the fault timer is active as described in the *Fault Timer and Restart* section. If the load current falls below the current limit threshold before the end of the Fault Timeout Period, the LM5066I resumes usual operation. If the current limit condition persists for longer than the Fault Timeout Period set by C_T, the IIN OC Fault bit in the STATUS_INPUT (7Ch) register, the INPUT bit in the STATUS_WORD (79h) register, and IIN_OC/PFET_OP_FAULT bit in the DIAGNOSTIC_WORD (E1h) register is toggled high and $\overline{SMBA}$ pin is asserted. $\overline{SMBA}$ toggling can be disabled using the ALERT_MASK (D8h) register. For proper operation, the R_{SNS} resistor value should be no higher than 200 mΩ. Higher values may create instability in the current limit control loop. The current limit threshold pin value may be overridden by setting appropriate bits in the DEVICE_SETUP register (D9h).

Feature Description (continued)

8.3.2 Circuit Breaker

If the load current increases rapidly (for example, the load is short circuited), the current in the sense resistor (R_S) may exceed the current limit threshold before the current limit control loop is able to respond. If the current exceeds 1.94x or 3.87x (CL = GND) the current limit threshold, Q_1 is quickly switched off by the 160-mA pulldown current at the GATE pin and a Fault Timeout Period begins. When the voltage across R_{SNS} falls below the circuit breaker (CB) threshold, the 160-mA pulldown current at the GATE pin is switched off, and the gate voltage of Q_1 is then determined by the current limit or the power limit functions. If the TIMER pin reaches 3.9 V before the current limiting or power limiting condition ceases, Q_1 is switched off by the 4.2-mA pulldown current at the GATE pin as described in the *Fault Timer and Restart* section. A circuit breaker event causes the CIRCUIT BREAKER FAULT bit in the STATUS_OTHER (7Fh), STATUS_MFR_SPECIFIC (80h), and DIAGNOSTIC_WORD (E1h) registers to be toggled high and SMBA pin are asserted unless this feature is disabled using the ALERT_MASK (D8h) register. The circuit breaker pin configuration may be overridden by setting appropriate bits in the DEVICE_SETUP (D9h) register.

8.3.3 Power Limit

An important feature of the LM5066I is the MOSFET power limiting. The Power Limit function can be used to maintain the maximum power dissipation of MOSFET Q_1 within the device SOA rating. The LM5066I determines the power dissipation in Q_1 by monitoring its drain-source voltage (SENSE to OUT), and the drain current through the R_{SNS} (VIN_K to SENSE). The product of the current and voltage is compared to the power limit threshold programmed by the resistor at the PWR pin. If the power dissipation reaches the limiting threshold, the GATE voltage is modulated to regulate the current in Q_1. While the power limiting circuit is active, the fault timer is active as described in the *Fault Timer and Restart* section. If the power limit condition persists for longer than the Fault Timeout Period set by the timer capacitor, C_T, the IIN OC Fault bit in the STATUS_INPUT (7Ch) register, the INPUT bit in the STATUS_WORD (79h) register, and the IIN_OC/PFET_OP_FAULT bit in the DIAGNOSTIC_WORD (E1h) register is toggled high and SMBA pin is asserted unless this feature is disabled using the ALERT_MASK (D8h) register.

8.3.4 UVLO

The series-pass MOSFET (Q_1) is enabled when the input supply voltage (V_{IN}) is within the operating range defined by the programmable UVLO and OVLO levels. Typically the UVLO level at V_{IN} is set with a resistor divider. Referring to the *Functional Block Diagram* when V_{IN} is below the UVLO level, the internal 20-µA current source at UVLO is enabled, the current source at OVLO is off, and Q_1 is held off by the 4.2-mA pulldown current at the GATE pin. As V_{IN} is increased, raising the voltage at UVLO above its threshold the 20 µA current source at UVLO is switched off, increasing the voltage at UVLO, providing hysteresis for this threshold. With the UVLO/EN pin above its threshold, Q_1 is switched on by the 20-µA current source at the GATE pin if the insertion time delay has expired.

See the *Application and Implementation* section for a procedure to calculate the values of the threshold setting resistors. The minimum possible UVLO level at V_{IN} can be set by connecting the UVLO/EN pin to VIN. In this case, Q_1 is enabled after the insertion time when the voltage at VIN reaches the POR threshold. After power-up, an UVLO condition causes the INPUT bit in the STATUS_WORD (79h) register, the VIN_UV_FAULT bit in the STATUS_INPUT (7Ch) register, and the VIN_UNDERVOLTAGE_FAULT bit in the DIAGNOSTIC_WORD (E1h) registers to be toggled high and SMBA pin is pulled low unless this feature is disabled using the ALERT_MASK (D8h) register.

8.3.5 OVLO

The series-pass MOSFET (Q_1) is enabled when the input supply voltage (V_{IN}) is within the operating range defined by the programmable UVLO and OVLO levels. If V_{IN} raises the OVLO pin voltage above its threshold, Q_1 is switched off by the 4.2-mA pulldown current at the GATE pin, denying power to the load. When the OVLO pin is above its threshold, the internal 21-µA current source at OVLO is switched on, raising the voltage at OVLO to provide threshold hysteresis. When V_{IN} is reduced below the OVLO level Q_1 is re-enabled. An OVLO condition toggles the VIN_OV_FAULT bit in the STATUS_INPUT (7Ch) register, the INPUT bit in the STATUS_WORD (79h) register and the VIN_OVERVOLTAGE_FAULT bit in the DIAGNOSTIC_WORD (E1h) register. The SMBA pin is pulled low unless this feature is disabled using the ALERT_MASK (D8h) register.

See the *Application and Implementation* section for a procedure to calculate the threshold setting resistor values.

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Feature Description (continued)

8.3.6 Power Good Pin

The Power Good indicator pin (PGD) is connected to the drain of an internal N-channel MOSFET capable of sustaining 80 V in the off-state, and transients up to 100 V. An external pullup resistor is required at PGD to an appropriate voltage to indicate the status to downstream circuitry. The off-state voltage at the PGD pin can be higher or lower than the voltages at VIN and OUT. PGD is switched high when the voltage at the FB pin exceeds the PGD threshold voltage. Typically, the output voltage threshold is set with a resistor divider from output to feedback, although the monitored voltage need not be the output voltage. Any other voltage can be monitored as long as the voltage at the FB pin does not exceed its maximum rating. Referring to the *Functional Block Diagram*, when the voltage at the FB pin is below its threshold, the 20-µA current source at FB is disabled. As the output voltage increases, taking FB above its threshold, the current source is enabled, sourcing current out of the pin, raising the voltage at FB to provide threshold hysteresis. The PGD output is forced low when either the UVLO/EN pin is below its threshold or the OVLO pin is above its threshold. The status of the PGD pin can be read through the PMBus interface in either the STATUS_WORD (79h) or DIAGNOSTIC_WORD (E1h) registers.

8.3.7 VDD Sub-Regulator

The LM5066I contains an internal linear sub-regulator, which steps down the input voltage to generate a 4.9-V rail used for powering low voltage circuitry. The VDD sub-regulator should be used as the pullup supply for the CL, RETRY, ADR2, ADR1, and ADR0 pins if they are to be tied high. It may also be used as the pullup supply for the PGD and the SMBus signals (SDA, SCL, and SMBA). The VDD sub-regulator is not designed to drive high currents and should not be loaded with other integrated circuits. The VDD pin is current limited to 30 mA in order to protect the LM5066I in the event of a short. The sub-regulator requires a ceramic bypass capacitance having a value of 1 µF or greater to be placed as close to the VDD pin as the PCB layout allows.

8.3.8 Remote Temperature Sensing

The LM5066I is designed to measure temperature remotely using an MMBT3904 NPN transistor. The base and collector of the MMBT3904 should be connected to the DIODE pin and the emitter to the LM5066I ground. Place the MMBT3904 near the device that requires temperature sensing. If the temperature of the hot swap pass MOSFET, Q_1, is to be measured, the MMBT3904 should be placed as close to Q_1 as the layout allows. The temperature is measured by means of a change in the diode voltage in response to a step in current supplied by the DIODE pin. The DIODE pin sources a constant 9.4 µA, but pulses 250 µA once every millisecond to measure the diode temperature. Take care in the PCB layout to keep the parasitic resistance between the DIODE pin and the MMBT3904 low so as not to degrade the measurement. In addition it is recommended to make a Kelvin connection from the emitter of the MMBT3904 to the GND of the part to ensure an accurate measurement. Additionally, a small 1000-pF bypass capacitor should be placed in parallel with the MMBT3904 to reduce the effects of noise. The temperature can be read using the READ_TEMPERATURE_1 PMBus command (8Dh). By default, the temperature fault and warning thresholds of the LM5066I are set to 256°C and are effectively disabled. These thresholds can be reprogrammed through the PMBus interface using the OT_WARN_LIMIT (51h) and OT_FAULT_LIMIT (4Fh) commands. If the temperature measurement and protection capability of the LM5066I are not used, the DIODE pin should be grounded.

Erroneous temperature measurements may result when the device input voltage is below the minimum operating voltage (10 V), due to VREF dropping out below the nominal voltage (2.97 V). At higher ambient temperatures, this measurement could read a value higher than the OT_FAULT_LIMIT, and trigger a fault, disabling Q_1. In this case, the faults should be removed and the device reset by writing a 0h, followed by an 80h to the OPERATION (03h) register.

8.3.9 Damaged MOSFET Detection

The LM5066I is able to detect whether the external MOSFET, Q_1, is damaged under certain conditions. If the voltage across the sense resistor exceeds 4 mV while the GATE voltage is low or the internal logic indicates that the GATE should be low, the EXT_MOSFET_SHORTED bit in the STATUS_MFR_SPECIFIC (80h) and DIAGNOSTIC_WORD (E1h) registers are toggled high and the SMBA pin is asserted unless this feature is disabled using the ALERT_MASK register (D8h). This method effectively determines whether Q_1 is shorted because of damage present between the drain and gate and/or drain and source.

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8.4 Device Functional Modes

8.4.1 Power-Up Sequence

The VIN operating range of the LM5066I is 10 to 80 V, with a transient capability to 100 V. Referring to the and Figure 13, as the voltage at VIN initially increases, the external N-channel MOSFET (Q_1) is held off by an internal 160-mA pulldown current at the GATE pin. The strong pulldown current at the GATE pin prevents an inadvertent turn-on as the gate-to-drain (Miller) capacitance of the MOSFET is charged. Additionally, the TIMER pin is initially held at ground. When the V_{IN} voltage reaches the POR threshold the insertion time begins. During the insertion time, the capacitor at the TIMER pin (C_T) is charged by a 4.8-µA current source, and Q_1 is held off by a 4.2-mA pulldown current at the GATE pin regardless of the input voltage. The insertion time delay allows ringing and transients at V_{IN} to settle before Q_1 is enabled. The insertion time ends when the TIMER pin voltage reaches 3.9 V. C_T is then quickly discharged by an internal 1.5-mA pulldown current. The GATE pin then switches on Q_1 when V_{IN} exceeds the UVLO threshold. If V_{IN} is above the UVLO threshold at the end of the insertion time, Q_1 the GATE pin charge pump sources 20 µA to charge the gate capacitance of Q_1. The maximum voltage from the gate to source of the Q_1 is limited by an internal 16.5-V Zener diode.

As the voltage at the OUT pin increases, the LM5066I monitors the drain current and power dissipation of MOSFET Q_1. In-rush current limiting or power limiting circuits, or both, actively control the current delivered to the load. During the in-rush limiting interval (t_2 in Figure 13), an internal 75-µA fault timer current source charges C_T. If Q_1's power dissipation and the input current reduce below their respective limiting thresholds before the TIMER pin reaches 3.9 V, the 75-µA current source is switched off, and C_T is discharged by the internal 2.5-µA current sink (t_3 in Figure 13). The in-rush limiting no longer engages unless a current-limit condition occurs.

If the TIMER pin voltage reaches 3.9 V before in-rush current limiting or power limiting ceases during t_2, a fault is declared and Q_1 is turned off. See the *Fault Timer and Restart* section for a complete description of the fault mode.

The LM5066I asserts the $\overline{\text{SMBA}}$ pin after the input voltage has exceeded its POR threshold to indicate that the volatile memory and device settings are in their default state. The CONFIG_PRESET bit within the STATUS_MFR_SPECIFIC register (80h) indicates default configuration of warning thresholds and device operation and remains high until a CLEAR_FAULTS command is received.

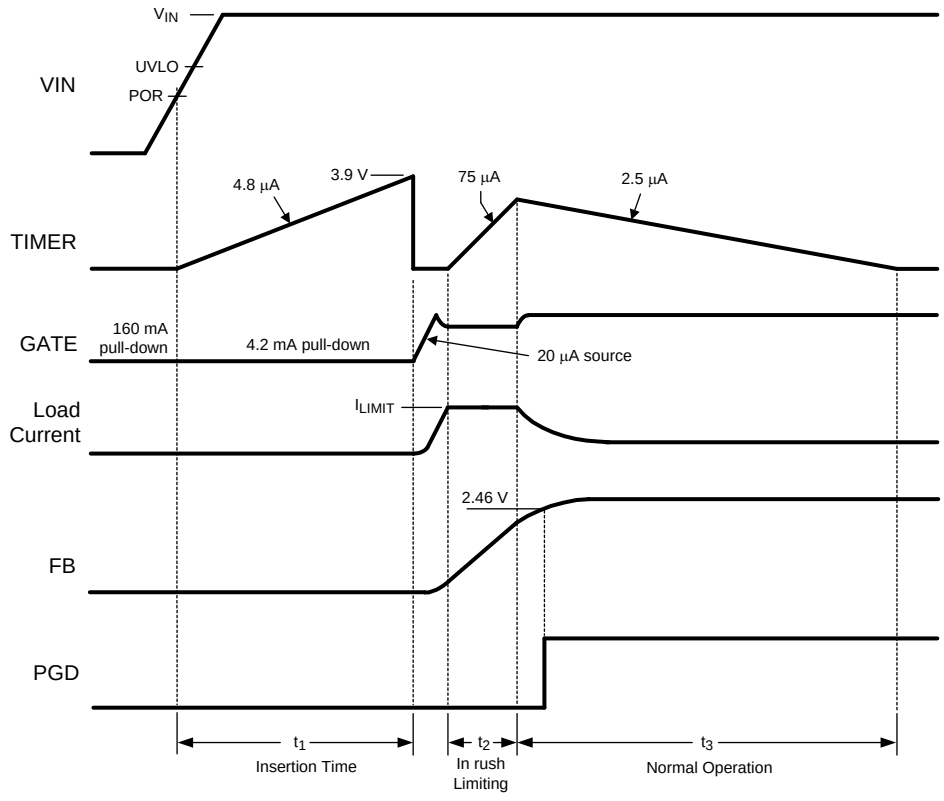


Figure 13. Power-Up Sequence (Current Limit Only)

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Device Functional Modes (continued)

8.4.2 Gate Control

A charge pump provides the voltage at the GATE pin to enhance the N-channel MOSFET's gate (Q_1). During normal operating conditions (t_3 in Figure 13), the gate of Q_1 is held charged by an internal 20-µA current source. The charge pump peak voltage is roughly 13.5 V, which forces a V_{GS} across Q1 of 13.5 V under normal operation. When the system voltage is initially applied, the GATE pin is held low by a 160-mA pulldown current. This helps prevent an inadvertent turn-on of Q_1 through its drain-gate capacitance as the applied system voltage increases.

During the insertion time (t_1 in Figure 13) the GATE pin is held low by a 4.2-mA pulldown current. This maintains Q_1 in the off-state until the end of t_1, regardless of the voltage at VIN or UVLO. Following the insertion time, during t_2 in Figure 13 the gate voltage of Q_1 is modulated to keep the current or power dissipation level from exceeding the programmed levels. While in the current or power limiting mode, the TIMER pin capacitor is charging. If the current and power limiting cease before the TIMER pin reaches 3.9 V, the TIMER pin capacitor then discharges, and the circuit begins normal operation. If the in-rush limiting condition persists such that the TIMER pin reached 3.9 V during t_2, the GATE pin is then pulled low by the 4.2-mA pulldown current. The GATE pin is then held low until either a power-up sequence is initiated ($\overline{\text{RETRY}}$ pin to VDD), or an automatic retry is attempted ($\overline{\text{RETRY}}$ pin to GROUND or floating). See the *Fault Timer and Restart* section. If the system input voltage falls below the UVLO threshold, or rises above the OVLO threshold, the GATE pin is pulled low by the 4.2-mA pulldown current to switch off Q_1.

8.4.3 Fault Timer and Restart

When the current limit or power limit threshold is reached during turn-on, or as a result of a fault condition, the gate-to-source voltage of Q_1 is modulated to regulate the load current and power dissipation in Q_1. When either limiting function is active, a 75-µA fault timer current source charges the external capacitor (C_T) at the TIMER pin as shown in Figure 13 (fault timeout period). If the fault condition subsides during the fault timeout period before the TIMER pin reaches 3.9 V, the LM5066I returns to the normal operating mode and C_T is discharged by the 1.5-mA current sink. If the TIMER pin reaches 3.9 V during the fault timeout period, Q_1 is switched off by a 4.2-mA pulldown current at the GATE pin. The subsequent restart procedure then depends on the selected retry configuration.

If the $\overline{\text{RETRY}}$ pin is high, the LM5066I latches the GATE pin low at the end of the fault timeout period. C_T is then discharged to ground by the 2.5-µA fault current sink. The GATE pin is held low by the 4.2-mA pulldown current until a power-up sequence is externally initiated by cycling the input voltage (V_{IN}), or momentarily pulling the UVLO/EN pin below its threshold with an open-collector or open-drain device as shown in Figure 14. The voltage at the TIMER pin must be <0.3 V for the restart procedure to be effective. The TIMER_LATCHED_OFF bit in the DIAGNOSTIC_WORD (E1h) register remains high while the latched off condition persists.

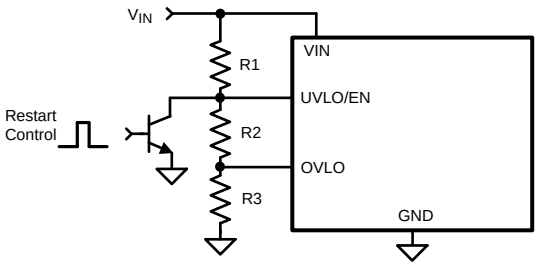


Figure 14. Latched Fault Restart Control

The LM5066I provides an automatic restart sequence which consists of the TIMER pin cycling between 3.9 and 1.2 V seven times after the fault timeout period, as shown in Figure 15. The period of each cycle is determined by the 75-µA charging current, the 2.5-µA discharge current, and the value of the capacitor, C_T. When the TIMER pin reaches 0.3 V during the eighth high-to-low ramp, the 20-µA current source at the GATE pin turns on Q_1. If the fault condition is still present, the fault timeout period and the restart sequence repeat. The $\overline{\text{RETRY}}$ pin allows selecting no retries or infinite retries. Finer control of the retry behavior can be achieved through the DEVICE_SETUP (D9h) register. Retry counts of 0, 1, 2, 4, 8, 16, or infinite may be selected by setting the appropriate bits in the DEVICE_SETUP (D9h) register.

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Device Functional Modes (continued)

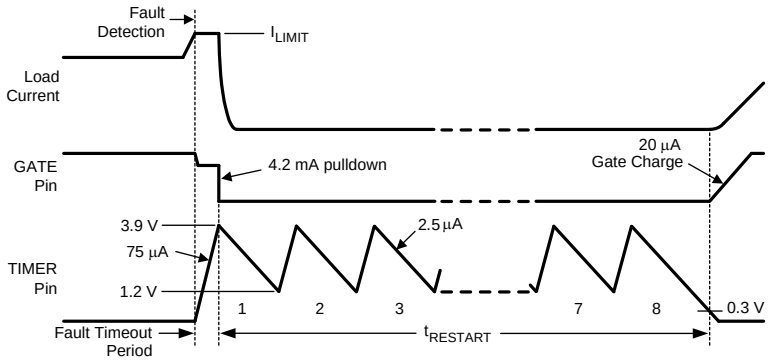


Figure 15. Restart Sequence

8.4.4 Shutdown Control

The load current can be remotely switched off by taking the UVLO/EN pin below its threshold with an open collector or open-drain device, as shown in Figure 16. When UVLO/EN pin is released, the LM5066I switches on the FET with in-rush current and power limiting.

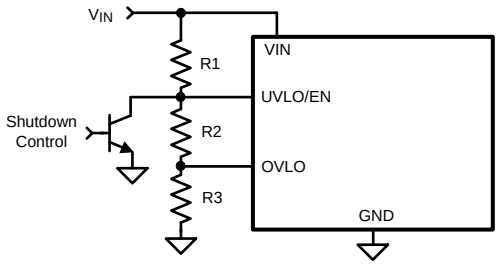


Figure 16. Shutdown Control

8.4.5 Enabling/Disabling and Resetting

The output can be disabled at during normal operation by either pulling the UVLO/EN pin to below its threshold or the OVLO pin above its threshold. This will cause the GATE voltage to be forced low with a pulldown strength of 4.2 mA. Toggling the UVLO/EN pin also resets the LM5066I from a latched-off state due to an overcurrent or over-power limit condition that caused the maximum allowed number of retries to be exceeded. While the UVLO/EN or OVLO pins can be used to disable the output, they have no effect on the volatile memory or address location of the LM5066I. User-stored values for address, device operation, and warning and fault levels programmed through the SMBus are preserved while the LM5066I is powered regardless of the state of the UVLO/EN and OVLO pins. The output may also be enabled or disabled by writing 80h or 0h to the OPERATION (03h) register. To re-enable after a fault, the fault condition should be cleared by programing the OPERATION (03h) register with 0h and then 80h.

The SMBus address of the LM5066I is captured based-on the states of the ADR0, ADR1, and ADR2 pins (GND, NC, and VDD) during turn on and is latched into a volatile register after VDD has exceeded its POR threshold of 4.1 V. Reassigning or postponing the address capture is accomplished by holding the VREF pin to ground. Pulling the VREF pin low also resets the logic and erases the volatile memory of the LM5066I. When released, the VREF pin charges up to its final value and the address is latched into a volatile register when the voltage at the VREF exceeds 2.55 V.

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8.5 Programming

8.5.1 PMBus Command Support

The device features an SMBus interface that allows the use of PMBus commands to set warn levels, error masks, and get telemetry on V_{IN}, V_{OUT}, I_{IN}, V_{AUX}, and P_{IN}. The supported PMBus commands are shown in Table 2.

Table 2. Supported PMBus Commands

CODE	NAME	FUNCTION	R/W	NUMBER OF DATA BYTES	DEFAULT VALUE
01h	OPERATION	Retrieves or stores the operation status	R/W	1	80h
03h	CLEAR_FAULTS	Clears the status registers and re-arms the black box registers for updating	Send byte	0	
19h	CAPABILITY	Retrieves the device capability	R	1	B0h
43h	VOUT_UV_WARN_LIMIT	Retrieves or stores output undervoltage warn limit threshold	R/W	2	0000h
4Fh	OT_FAULT_LIMIT	Retrieves or stores over temperature fault limit threshold	R/W	2	0FFFh (256°C)
51h	OT_WARN_LIMIT	Retrieves or stores over temperature warn limit threshold	R/W	2	0FFFh (256°C)
57h	VIN_OV_WARN_LIMIT	Retrieves or stores input overvoltage warn limit threshold	R/W	2	0FFFh
58h	VIN_UV_WARN_LIMIT	Retrieves or stores input undervoltage warn limit threshold	R/W	2	0000h
5Dh	IIN_OC_WARN_LIMIT	Retrieves or stores input current warn limit threshold (mirror at D3h)	R/W	2	0FFFh
78h	STATUS_BYTE	Retrieves information about the parts operating status	R	1	01h
79h	STATUS_WORD	Retrieves information about the parts operating status	R	2	0801h
7Ah	STATUS_VOUT	Retrieves information about output voltage status	R	1	00h
7Ch	STATUS_INPUT	Retrieves information about input status	R	1	10h
7Dh	STATUS_TEMPERATURE	Retrieves information about temperature status	R	1	00h
7Eh	STATUS_CML	Retrieves information about communications status	R	1	00h
7Fh	STATUS_OTHER	Retrieves other status information	R	1	00h
80h	STATUS_MFR_SPECIFIC	Retrieves information about circuit breaker and MOSFET shorted status	R	1	10h
86h	READ_EIN	Retrieves energy meter measurement	R	6	00h 00h 00h 00h 00h 00h
88h	READ_VIN	Retrieves input voltage measurement	R	2	0000h
89h	READ_IIN	Retrieves input current measurement (Mirrors at D1h)	R	2	0000h
8Bh	READ_VOUT	Retrieves output voltage measurement	R	2	0000h
8Dh	READ_TEMPERATURE_1	Retrieves temperature measurement	R	2	0190h
97h	READ_PIN	Retrieves averaged input power measurement (mirror at DFh).	R	2	0000h
99h	MFR_ID	Retrieves manufacturer ID in ASCII characters (TI)	R	3	54h 49h 0h
9Ah	MFR_MODEL	Retrieves part number in ASCII characters. (LM5066I)	R	8	4Ch 4Dh 35h 30h 36h 36h 49h 0h
9Bh	MFR_REVISION	Retrieves part revision letter or number in ASCII (for example, AA)	R	2	41h 41h
D0h	MFR_SPECIFIC_00 READ_VAUX	Retrieves auxiliary voltage measurement	R	2	0000h
D1h	MFR_SPECIFIC_01 MFR_READ_IIN	Retrieves input current measurement (Mirror at 89h)	R	2	0000h
D2h	MFR_SPECIFIC_02 MFR_READ_PIN	Retrieves input power measurement	R	2	0000h
D3h	MFR_SPECIFIC_03 MFR_IIN_OC_WARN_LIMIT	Retrieves or stores input current limit warn threshold (Mirror at 5Dh)	R/W	2	0FFFh

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Programming (continued)

Table 2. Supported PMBus Commands (continued)

CODE	NAME	FUNCTION	R/W	NUMBER OF DATA BYTES	DEFAULT VALUE
D4h	MFR_SPECIFIC_04 MFR_PIN_OP_WARN_LIMIT	Retrieves or stores input power limit warn threshold	R/W	2	0FFFh
D5h	MFR_SPECIFIC_05 READ_PIN_PEAK	Retrieves measured peak input power measurement	R	2	0000h
D6h	MFR_SPECIFIC_06 CLEAR_PIN_PEAK	Resets the contents of the peak input power register to 0	Send byte	0	
D7h	MFR_SPECIFIC_07 GATE_MASK	Allows the user to disable MOSFET gate shutdown for various fault conditions	R/W	1	0000h
D8h	MFR_SPECIFIC_08 ALERT_MASK	Retrieves or stores user $\overline{\text{SMBA}}$ fault mask	R/W	2	FD04h
D9h	MFR_SPECIFIC_09 DEVICE_SETUP	Retrieves or stores information about number of retry attempts	R/W	1	0000h
DAh	MFR_SPECIFIC_10 BLOCK_READ	Retrieves most recent diagnostic and telemetry information in a single transaction	R	12	0880h 0000h 0000h 0000h 0000h 0000h
DBh	MFR_SPECIFIC_11 SAMPLES_FOR_AVG	Exponent value AVGN for number of samples to be averaged (N = 2^{AVGN}), range = 00h to 0Ch	R/W	1	08h
DCh	MFR_SPECIFIC_12 READ_AVG_VIN	Retrieves averaged input voltage measurement	R	2	0000h
DDh	MFR_SPECIFIC_13 READ_AVG_VOUT	Retrieves averaged output voltage measurement	R	2	0000h
DEh	MFR_SPECIFIC_14 READ_AVG_IIN	Retrieves averaged input current measurement	R	2	0000h
DFh	MFR_SPECIFIC_15 READ_AVG_PIN	Retrieves averaged input power measurement	R	2	0000h
E0h	MFR_SPECIFIC_16 BLACK_BOX_READ	Captures diagnostic and telemetry information, which are latched when the first $\overline{\text{SMBA}}$ event occurs after faults are cleared	R	12	0880h 0000h 0000h 0000h 0000h 0000h
E1h	MFR_SPECIFIC_17 DIAGNOSTIC_WORD_READ	Manufacturer-specific parallel of the STATUS_WORD to convey all FAULT/WARN data in a single transaction	R	2	0880h
E2h	MFR_SPECIFIC_18 AVG_BLOCK_READ	Retrieves most recent average telemetry and diagnostic information in a single transaction	R	12	0880h 0000h 0000h 0000h 0000h 0000h

8.5.2 Standard PMBus Commands

8.5.2.1 OPERATION (01h)

The OPERATION command is a standard PMBus command that controls the MOSFET switch. This command can be used to switch the MOSFET on and off under host control. It is also used to re-enable the MOSFET after a fault triggered shutdown. Writing an OFF command, followed by an ON command, clears all faults and re-enables the device. Writing only an ON after a fault-triggered shutdown does not clear the fault registers or re-enable the device. The OPERATION command is issued with the write byte protocol.

Table 3. Recognized OPERATION Command Values

VALUE	MEANING	DEFAULT
80h	Switch ON	80h
00h	Switch OFF	N/A

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8.5.2.2 CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is a standard PMBus command that resets all stored warning and fault flags and the SMBA signal. If a fault or warning condition still exists when the CLEAR_FAULTS command is issued, the SMBA signal may not clear or re-asserts almost immediately. Issuing a CLEAR_FAULTS command does not cause the MOSFET to switch back on in the event of a fault turnoff; that must be done by issuing an OPERATION command after the fault condition is cleared. This command uses the PMBus send byte protocol.

8.5.2.3 CAPABILITY (19h)

The CAPABILITY command is a standard PMBus command that returns information about the PMBus functions supported by the LM5066I. This command is read with the PMBus read byte protocol.

Table 4. CAPABILITY Register

VALUE	MEANING	DEFAULT
B0h	Supports packet error check, 400 Kb/s, supports SMBus alert	B0h

8.5.2.4 VOUT_UV_WARN_LIMIT (43h)

The VOUT_UV_WARN_LIMIT command is a standard PMBus command that allows configuring or reading the threshold for the VOUT undervoltage warning detection. Reading and writing to this register should use the coefficients shown in Table 47. Accesses to this command should use the PMBus read or write word protocol. If the measured value of VOUT falls below the value in this register, VOUT UV warn flags are set and the SMBA signal is asserted.

Table 5. VOUT_UV_WARN_LIMIT Register

VALUE	MEANING	DEFAULT
0001h to 0FFFh	VOUT undervoltage warning detection threshold	0000h (disabled)
0000h	VOUT undervoltage warning disabled	N/A

8.5.2.5 OT_FAULT_LIMIT (4Fh)

The OT_FAULT_LIMIT command is a standard PMBus command that allows configuring or reading the threshold for the overtemperature fault detection. Reading and writing to this register should use the coefficients shown in Table 47. Accesses to this command should use the PMBus read or write word protocol. If the measured temperature exceeds this value, an overtemperature fault is triggered and the MOSFET is switched off, OT FAULT flags set, and the SMBA signal asserted. After the measured temperature falls below the value in this register, the MOSFET may be switched back on with the OPERATION command. A single temperature measurement is an average of 16 round-robin cycles; therefore, the minimum temperature fault detection time is 16 ms.

Table 6. OT_FAULT_LIMIT Register

VALUE	MEANING	DEFAULT
0000h to 0FFEh	Over-temperature fault threshold value	0FFFh (256°C)
0FFFh	Over-temperature fault detection disabled	N/A

8.5.2.6 OT_WARN_LIMIT (51h)

The OT_WARN_LIMIT command is a standard PMBus command that allows configuring or reading the threshold for the over-temperature warning detection. Reading and writing to this register should use the coefficients shown in Table 47. Accesses to this command should use the PMBus read or write word protocol. If the measured temperature exceeds this value, an over-temperature warning is triggered and the OT WARN flags set in the respective registers and the SMBA signal asserted. A single temperature measurement is an average of 16 round-robin cycles; therefore, the minimum temperature warn detection time is 16 ms.

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Table 7. OT_WARN_LIMIT Register

VALUE	MEANING	DEFAULT
0000h to 0FFEh	Over-temperature warn threshold value	0FFFh (256°C)
0FFFh	Over-temperature warn detection disabled	N/A

8.5.2.7 VIN_OV_WARN_LIMIT (57h)

The VIN_OV_WARN_LIMIT command is a standard PMBus command that allows configuring or reading the threshold for the VIN overvoltage warning detection. Reading and writing to this register should use the coefficients shown in Table 47. Accesses to this command should use the PMBus read or write word protocol. If the measured value of VIN rises above the value in this register, VIN OV warn flags are set in the respective registers and the SMBA signal is asserted.

Table 8. VIN_OV_WARN_LIMIT Register

VALUE	MEANING	DEFAULT
0h to 0FFEh	VIN overvoltage warning detection threshold	0FFFh (disabled)
0FFFh	VIN overvoltage warning disabled	N/A

8.5.2.8 VIN_UV_WARN_LIMIT (58h)

The VIN_UV_WARN_LIMIT command is a standard PMBus command that allows configuring or reading the threshold for the VIN undervoltage warning detection. Reading and writing to this register should use the coefficients shown in Table 47. Accesses to this command should use the PMBus read or write word protocol. If the measured value of VIN falls below the value in this register, VIN UV warn flags are set in the respective register, and the SMBA signal is asserted.

Table 9. VIN_UV_WARN_LIMIT Register

VALUE	MEANING	DEFAULT
1h to 0FFFh	VIN undervoltage warning detection threshold	0000h (disabled)
0000h	VIN undervoltage warning disabled	N/A

8.5.2.9 STATUS_BYTE (78h)

The STATUS BYTE is a standard PMBus command that returns the value of a number of flags indicating the state of the LM5066I. Accesses to this command should use the PMBus read byte protocol. To clear bits in this register, the underlying fault should be removed on the system and a CLEAR_FAULTS command issued.

Table 10. STATUS_BYTE Definitions

BIT	NAME	MEANING	DEFAULT
7	BUSY	Not supported, always 0	0
6	OFF	This bit is asserted if the MOSFET is not switched on for any reason.	0
5	VOUT OV	Not supported, always 0	0
4	IOUT OC	Not supported, always 0	0
3	VIN UV fault	A VIN undervoltage fault has occurred	0
2	TEMPERATURE	A temperature fault or warning has occurred	0
1	CML	A communication fault has occurred	0
0	None of the above	A fault or warning not listed in bits [7:1] has occurred	1

8.5.2.10 STATUS_WORD (79h)

The STATUS_WORD command is a standard PMBus command that returns the value of a number of flags indicating the state of the LM5066I. Accesses to this command should use the PMBus read word protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR _FAULTS command issued. The INPUT and VIN UV flags default to 1 on startup; however, they are cleared to 0 after the first time the input voltage exceeds the resistor-programmed UVLO threshold.

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Table 11. STATUS_WORD Definitions

BIT	NAME	MEANING	DEFAULT
15	VOUT	An output voltage fault or warning has occurred	0
14	IOUT/POUT	Not supported, always 0	0
13	INPUT	An input voltage or current fault has occurred	0
12	FET FAIL	FET is shorted	0
11	$\overline{\text{POWER GOOD}}$	The Power Good signal has been negated	1
10	FANS	Not supported, always 0	0
9	CB_Fault	Circuit breaker fault triggered	0
8	UNKNOWN	Not supported, always 0	0
7	BUSY	Not supported, always 0	0
6	OFF	This bit is asserted if the MOSFET is not switched on for any reason.	0
5	VOUT OV	Not supported, always 0	0
4	IOUT OC	Not supported, always 0	0
3	VIN UV	A VIN undervoltage fault has occurred	0
2	TEMPERATURE	A temperature fault or warning has occurred	0
1	CML	A communication fault has occurred	0
0	None of the above	A fault or warning not listed in bits [7:1] has occurred	1

8.5.2.11 STATUS_VOUT (7Ah)

The STATUS_VOUT command is a standard PMBus command that returns the value of the VOUT UV warn flag. Accesses to this command should use the PMBus read byte protocol. To clear bits in this register, the underlying fault should be cleared and a CLEAR_FAULTS command issued.

Table 12. STATUS_VOUT Definitions

BIT	NAME	MEANING	DEFAULT
7	VOUT OV fault	Not supported, always 0	0
6	VOUT OV warn	Not supported, always 0	0
5	VOUT UV warn	A VOUT undervoltage warning has occurred	0
4	VOUT UV fault	Not supported, always 0	0
3	VOUT max	Not supported, always 0	0
2	TON max fault	Not supported, always 0	0
1	TOFF max fault	Not supported, always 0	0
0	VOUT tracking error	Not supported, always 0	0

8.5.2.12 STATUS_INPUT (7Ch)

The STATUS_INPUT command is a standard PMBus command that returns the value of a number of flags related to input voltage, current, and power. Accesses to this command should use the PMBus read byte protocol. To clear bits in this register, the underlying fault should be cleared and a CLEAR_FAULTS command issued. The VIN UV warn flag defaults to 1 on startup; however, it is cleared to 0 after the first time the input voltage increases above the resistor-programmed UVLO threshold.

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Table 13. STATUS_INPUT Definitions

BIT	NAME	MEANING	DEFAULT
7	VIN OV fault	A VIN overvoltage fault has occurred	0
6	VIN OV warn	A VIN overvoltage warning has occurred	0
5	VIN UV warn	A VIN undervoltage warning has occurred	1
4	VIN UV fault	A VIN undervoltage fault has occurred	0
3	Insufficient voltage	Not supported, always 0	0
2	IIN OC fault	An IIN overcurrent fault has occurred	0
1	IIN OC warn	An IIN overcurrent warning has occurred	0
0	PIN OP warn	A PIN overpower warning has occurred	0

8.5.2.13 STATUS_TEMPERATURE (7dh)

The STATUS_TEMPERATURE is a standard PMBus command that returns the value of the of a number of flags related to the temperature telemetry value. Accesses to this command should use the PMBus read byte protocol. To clear bits in this register, the underlying fault should be cleared and a CLEAR_FAULTS command issued.

Table 14. STATUS_TEMPERATURE Definitions

BIT	NAME	MEANING	DEFAULT
7	Overtemp fault	An overtemperature fault has occurred	0
6	Overtemp warn	An overtemperature warning has occurred	0
5	Undertemp warn	Not supported, always 0	0
4	Undertemp fault	Not supported, always 0	0
3	Reserved	Not supported, always 0	0
2	Reserved	Not supported, always 0	0
1	Reserved	Not supported, always 0	0
0	Reserved	Not supported, always 0	0

8.5.2.14 STATUS_CML (7Eh)

The STATUS_CML is a standard PMBus command that returns the value of a number of flags related to communication faults. Accesses to this command should use the PMBus read byte protocol. To clear bits in this register, a CLEAR_FAULTS command should be issued.

Table 15. STATUS_CML Definitions

BIT	NAME	DEFAULT
7	Invalid or unsupported command received	0
6	Invalid or unsupported data received	0
5	Packet error check failed	0
4	Not supported, always 0	0
3	Not supported, always 0	0
2	Reserved, always 0	0
1	Miscellaneous communications fault has occurred	0
0	Not supported, always 0	0

8.5.2.15 STATUS_OTHER (7Fh)

Table 16. STATUS_OTHER Definitions

BIT	NAME	DEFAULT
7	Reserved: Always 0	0
6	Reserved: Always 0	0
5	CB Fault	0

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Table 16. STATUS_OTHER Definitions (continued)

BIT	NAME	DEFAULT
4	Not supported, always 0	0
3	Not supported, always 0	0
2	Not supported, always 0	0
1	Not supported, always 0	0
0	Not supported, always 0	0

8.5.2.16 STATUS_MFR_SPECIFIC (80h)

The STATUS_MFR_SPECIFIC command is a standard PMBus command that contains manufacturer specific status information. Accesses to this command should use the PMBus read byte protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command should be issued.

Table 17. STATUS_MFR_SPECIFIC Definitions

BIT	MEANING	DEFAULT
7	Circuit breaker fault	0
6	External MOSFET shorted fault	0
5	Not supported, always 0	0
4	Defaults loaded	1
3	Not supported, always 0	0
2	Not supported, always 0	0
1	Not supported, always 0	0
0	Not supported, always 0	0

8.5.2.17 READ_EIN (86h)

The READ_EIN command is a standard PMBus command that returns information the host can use to calculate average input power consumption. Accesses to this command should use the PMBus block read protocol. The information provided by this command is independent of any device-specific averaging period. Six data bytes are returned by this command. The first two bytes are the two's complement signed output of an accumulator that continuously sums samples of the instantaneous input power. The accumulator value is the summation of the instantaneous power measurement. These two data bytes are formatted in the DIRECT format. The next data byte is a rollover count for the accumulator. This byte is an unsigned integer that indicates the number of times the accumulator has rolled over from its maximum positive unsigned integer (7FFFh) to 0. The last three data bytes are a 24-bit unsigned integer that counts the number of samples of the instantaneous input power. This value also rolls over periodically from its maximum positive value to 0. It is up to the host to keep track of the sample count and account for the rollovers.

The combination of the accumulator and the roller count may overflow after a period of several seconds. Similarly, the sample count value overflows, but this event only occurs once every few hours.

To convert the data obtained from two separate READ_EIN commands into average power, first convert the accumulator and rollover count to an unsigned integer (see Equation 1).

$$\text{Accumulator_23} = (\text{rollover_count} << 15) + \text{accumulator} \quad (1)$$

Note that the overflow of this variable needs to be monitored and properly accounted for. Data from the previous calculation, along with the sample count values from the corresponding register access, can be used to get the unscaled average power:

$$\frac{\text{Accumulator_23 [n]} - \text{Accumulator_23 [n} - 1]}{\text{Sample_count [n]} - \text{Sample_count [n} - 1]}$$

where

- Accumulator_23 [n] = Overflow corrected, 23-bit accumulator data from this read
- Sample_count [n] = Sample count data from this read
- Accumulator_23 [n – 1] = Overflow corrected, 23-bit accumulator data from previous read
- Sample_count [n – 1] = Sample count data from previous read

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- Unscaled average power is now in the same units as the data from the READ_PIN command. Coefficients from Table 47 are used to convert the unscaled average power to Watts. (2)

Table 18. READ_EIN Definition

BYTE	MEANING	DEFAULT
0	Number of bytes	6
1	Power accumulator low byte	0
2	Power accumulator high byte	0
3	Power accumulator rollover count	0
4	Sample count low byte	0
5	Sample count mid byte	0
6	Sample count high byte	0

8.5.2.18 READ_VIN (88h)

The READ_VIN command is a0 standard PMBus command that returns the 12-bit measured value of the input voltage. Reading this register should use the coefficients shown in Table 47. Accesses to this command should use the P0MBus read word protocol. This value is also used internally for the VIN overvoltage and undervoltage warning detection.

Table 19. 0READ_VIN Register

VALUE	MEANING	DEFAULT
0000h to 0FFFh	Measured va0lue for VIN	0000h

8.5.2.19 READ_IIN (89h)

The READ_IIN command is a standard PMBus command that returns the 12-bit measured value of the input current. Reading this register should use the coefficients shown in Table 47. Accesses to this command should use the PMBus read word protocol. This value is also mirrored at (D1h).

Table 20. READ_IIN Register

VALUE	MEANING	DEFAULT
0000h to 0FFFh	Measured value for IIN	0000h

8.5.2.20 READ_VOUT (8Bh)

The READ_VOUT command is a standard PMBus command that returns the 12-bit measured value of the output voltage. Reading this register should use the coefficients shown in Table 47. Accesses to this command should use the PMBus read word protocol. This value is also used internally for the VOUT undervoltage warning detection.

Table 21. READ_VOUT Register

VALUE	MEANING	DEFAULT
0000h to 0FFFh	Measured value for VOUT	0000h

8.5.2.21 READ_TEMPERATURE_1 (8Dh)

The READ_TEMPERATURE_1 command is a standard PMBus command that returns the signed value of the temperature measured by the external temperature sense diode. Reading this register should use the coefficients shown in Table 47. Accesses to this command should use the PMBus read word protocol. This value is also used internally for the overtemperature fault and warning detection. This data has a range of –256°C to 255°C after the coefficients are applied.

Table 22. READ_TEMPERATURE_1 Register

VALUE	MEANING	DEFAULT
0000h to 0FFFh	Measured value for TEMPERATURE	0000h

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8.5.2.22 READ_PIN (97h)

The READ_PIN command is a standard PMBus command that returns the 12-bit measured value of the input power. Reading this register should use the coefficients shown in Table 47. Accesses to this command should use the PMBus read word protocol. This value is also mirrored at (D5h).

Table 23. READ_PIN Register

VALUE	MEANING	DEFAULT
0000h to 0FFFh	Measured value for PIN	0000h

8.5.2.23 MFR_ID (99h)

The MFR_ID command is a standard PMBus command that returns the identification of the manufacturer. To read the MFR_ID, use the PMBus block read protocol.

Table 24. MFR_ID Register

BYTE	NAME	VALUE
0	Number of bytes	03h
1	MFR ID-1	54h ‘T’
2	MFR ID-2	29h ‘I’
3	MFR ID-3	00h

8.5.2.24 MFR_MODEL (9Ah)

The MFR_MODEL command is a standard PMBus command that returns the part number of the chip. To read the MFR_MODEL, use the PMBus block read protocol.

Table 25. MFR_MODEL Register

BYTE	NAME	VALUE
0	Number of bytes	08h
1	MFR ID-1	4Ch ‘L’
2	MFR ID-2	4Dh ‘M’
3	MFR ID-3	35h ‘5’
4	MFR ID-4	30h ‘0’
5	MFR ID-5	36h ‘6’
6	MFR ID-6	36h ‘6’
7	MFR ID-7	49h 'I'
8	MFR ID-8	00h

8.5.2.25 MFR_REVISION (9Bh)

The MFR_REVISION command is a standard PMBus command that returns the revision level of the part. To read the MFR_REVISION, use the PMBus block read protocol.

Table 26. MFR_REVISION Register

BYTE	NAME	VALUE
0	Number of bytes	02h
1	MFR ID-1	41h ‘A’
2	MFR ID-2	41h ‘A’

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8.5.3 Manufacturer Specific PMBus Commands

8.5.3.1 MFR_SPECIFIC_00: READ_VAUX (D0h)

The READ_VAUX command reports the 12-bit ADC measured auxiliary voltage. Voltages greater than or equal to 2.97 V to ground are reported at plus full scale (0FFFh). Voltages less than or equal to 0 V referenced to ground are reported as 0 (0000h). To read data from the READ_VAUX command, use the PMBus read word protocol.

Table 27. READ_VAUX Register

VALUE	MEANING	DEFAULT
0000h to 0FFFh	Measured value for VAUX input	0000h

8.5.3.2 MFR_SPECIFIC_01: MFR_READ_IIN (D1h)

The MFR_READ_IIN command reports the 12-bit ADC measured current sense voltage. To read data from the MFR_READ_IIN command, use the PMBus read word protocol. Reading this register should use the coefficients shown in Table 47. See the section *Reading and Writing Telemetry Data and Warning Thresholds* to calculate the values to use.

Table 28. MFR_READ_IIN Register

VALUE	MEANING	DEFAULT
0000h to 0FFFh	Measured value for input current sense voltage	0000h

8.5.3.3 MFR_SPECIFIC_02: MFR_READ_PIN (D2h)

The MFR_READ_PIN command reports the upper 12 bits of the VIN × IIN product as measured by the 12-bit ADC. To read data from the MFR_READ_PIN command, use the PMBus read word protocol. Reading this register should use the coefficients shown in Table 47. See the section *Reading and Writing Telemetry Data and Warning Thresholds* to calculate the values to use.

Table 29. MFR_READ_PIN Register

VALUE	MEANING	DEFAULT
0000h to 0FFFh	VALUE for input current x input voltage	0000h

8.5.3.4 MFR_SPECIFIC_03: MFR_IN_OC_WARN_LIMIT (D3h)

The MFR_IIN_OC_WARN_LIMIT PMBus command sets the input overcurrent warning threshold. In the event that the input current rises above the value set in this register, the IIN overcurrent flags are set in the respective registers and the SMBA is asserted. To access the MFR_IIN_OC_WARN_LIMIT register, use the PMBus read/write word protocol. Reading and writing to this register should use the coefficients shown in Table 47.

Table 30. MFR_IIN_OC_WARN_LIMIT Register

VALUE	MEANING	DEFAULT
0000h to 0FFEh	Value for input overcurrent warn limit	0FFFh
0FFFh	Input overcurrent warning disabled	N/A

8.5.3.5 MFR_SPECIFIC_04: MFR_PIN_OP_WARN_LIMIT (D4h)

The MFR_PIN_OP_WARN_LIMIT PMBus command sets the input over-power warning threshold. In the event that the input power rises above the value set in this register, the PIN over-power flags are set in the respective registers and the SMBA is asserted. To access the MFR_PIN_OP_WARN_LIMIT register, use the PMBus read/write word protocol. Reading and writing to this register should use the coefficients shown in Table 47.

Table 31. MFR_PIN_OPWARN_LIMIT Register

VALUE	MEANING	DEFAULT
0000h to 0FFEh	Value for input over power warn limit	0FFFh

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Table 31. MFR_PIN_OPWARN_LIMIT Register (continued)

VALUE	MEANING	DEFAULT
0FFFh	Input over power warning disabled	N/A

8.5.3.6 MFR_SPECIFIC_05: READ_PIN_PEAK (D5h)

The READ_PIN_PEAK command reports the maximum input power measured since a power-on reset or the last CLEAR_PIN_PEAK command. To access the READ_PIN_PEAK command, use the PMBus read word protocol. Use the coefficients shown in Table 47.

Table 32. READ_PIN_PEAK Register

VALUE	MEANING	DEFAULT
0000h to 0FFFh	Maximum value for input current × input voltage since reset or last clear	0000h

8.5.3.7 MFR_SPECIFIC_06: CLEAR_PIN_PEAK (D6h)

The CLEAR_PIN_PEAK command clears the PIN PEAK register. This command uses the PMBus send byte protocol.

8.5.3.8 MFR_SPECIFIC_07: GATE_MASK (D7h)

The GATE_MASK register allows the hardware to prevent fault conditions from switching off the MOSFET. When the bit is high, the corresponding FAULT has no control over the MOSFET gate. All status registers are still updated (STATUS, DIAGNOSTIC) and $\overline{\text{SMBA}}$ is still asserted. This register is accessed with the PMBus read/write byte protocol.

CAUTION

Inhibiting the MOSFET switch off in response to overcurrent or circuit breaker fault conditions will likely result in the destruction of the MOSFET. This functionality must be used with great care and supervision.

Table 33. MFR_SPECIFIC_07 Gate Mask Definitions

BIT	NAME	DEFAULT
7	Not used, always 0	0
6	Not used, always 0	0
5	VIN UV FAULT	0
4	VIN OV FAULT	0
3	IIN/PFET FAULT	0
2	OVERTEMP FAULT	0
1	Not used, always 0	0
0	CIRCUIT BREAKER FAULT	0

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The IIN/PFET fault refers to the input current fault and the MOSFET power dissipation fault. There is no input power fault detection, only input power warning detection.

8.5.3.9 MFR_SPECIFIC_08: ALERT_MASK (D8h)

The ALERT_MASK command is used to mask the $\overline{\text{SMBA}}$ when a specific fault or warning has occurred. Each bit corresponds to one of the 14 different analog and digital faults or warnings that would normally result in an $\overline{\text{SMBA}}$ being asserted. When the corresponding bit is high, that condition does not cause the $\overline{\text{SMBA}}$ to be asserted. If that condition occurs, the registers where that condition is captured is still updated (STATUS registers, DIAGNOSTIC_WORD) and the external MOSFET gate control is still active (VIN_OV_FAULT, VIN_UV_FAULT, IIN/PFET_FAULT, CB_FAULT, OT_FAULT). This register is accessed with the PMBus read/write word protocol. The VIN UNDERVOLTAGE FAULT flag defaults to 1 on startup; however, it clears to 0 after the first time the input voltage increases above the resistor-programmed UVLO threshold.

Table 34. ALERT_MASK Definitions

BIT	NAME	DEFAULT
15	VOUT UNDERVOLTAGE WARN	1
14	IIN LIMIT warn	1
13	VIN UNDERVOLTAGE WARN	1
12	VIN OVERVOLTAGE WARN	1
11	$\overline{\text{POWER GOOD}}$	1
10	OVERTEMP WARN	1
9	Not used	0
8	OVERPOWER LIMIT WARN	1
7	Not used	0
6	EXT_MOSFET_SHORTED	0
5	VIN UNDERVOLTAGE FAULT	1
4	VIN OVERVOLTAGE FAULT	0
3	IIN/PFET FAULT	0
2	OVERTEMPERATURE FAULT	0
1	CML FAULT (communications fault)	0
0	CIRCUIT BREAKER FAULT	0

8.5.3.10 MFR_SPECIFIC_09: DEVICE_SETUP (D9h)

The DEVICE_SETUP command can be used to override pin settings to define operation of the LM5066I under host control. This command is accessed with the PMBus read/write byte protocol.

Table 35. DEVICE_SETUP Byte Format

BIT	NAME	MEANING
7:5	Retry setting	111 = Unlimited retries 110 = Retry 16 times 101 = Retry 8 times 100 = Retry 4 times 011 = Retry 2 times 010 = Retry 1 time 001 = No retries 000 = Pin configured retries
4	Current limit setting	0 = High setting (50 mV) 1 = Low setting (26 mV)
3	CB/CL ratio	0 = Low setting (1.9x) 1 = High setting (3.9x)
2	Current limit configuration	0 = Use pin settings 1 = Use SMBus settings
1	Unused	
0	Unused	

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To configure the current limit setting with this register, it is necessary to set the current limit configuration bit (2) to 1 to enable the register to control the current limit function and the current limit setting bit (4) to select the desired setting. If the current limit configuration bit is not set, the pin setting is used. The circuit breaker to current limit ratio value is set by the CB / CL ratio bit (3). Note that if the current limit configuration is changed, the samples for the telemetry averaging function are not reset. TI recommends to allow a full averaging update period with the new current limit configuration before processing the averaged data.

Note that the current limit configuration affects the coefficients used for the current and power measurements and warning registers.

8.5.3.11 MFR_SPECIFIC_10: BLOCK_READ (DAh)

The BLOCK_READ command concatenates the DIAGNOSTIC_WORD with input and output telemetry information (IIN, VOUT, VIN, PIN) as well as TEMPERATURE to capture all of the operating information of the LM5066I in a single SMBus transaction. The block is 12-bytes long with telemetry information being sent out in the same manner as if an individual READ_XXX command had been issued (shown in Table 36). The contents of the block read register are updated every clock cycle (85 ns) as long as the SMBus interface is idle. BLOCK_READ also specifies that the VIN, VOUT, IIN and PIN measurements are all time-aligned. If separate commands are used, individual samples may not be time-aligned because of the delay necessary for the communication protocol.

The block read command is read through the PMBus block read protocol.

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Table 36. BLOCK_READ Register Format

Byte Count (Always 12)	(1 Byte)
DIAGNOSTIC_WORD	(1 word)
IIN_BLOCK	(1 word)
VOUT_BLOCK	(1 word)
VIN_BLOCK	(1 word)
PIN_BLOCK	(1 word)
TEMP_BLOCK	(1 word)

8.5.3.12 MFR_SPECIFIC_11: SAMPLES_FOR_AVG (DBh)

The SAMPLES_FOR_AVG command is a manufacturer-specific command for setting the number of samples used in computing the average values for IIN, VIN, VOUT, and PIN. The decimal equivalent of the AVGN nibble is the power of 2 samples, (for example, AVGN = 12 equates to N = 4096 samples used in computing the average). The LM5066I supports average numbers of 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, and 4096. The SAMPLES_FOR_AVG number applies to average values of IIN, VIN, VOUT, and PIN simultaneously. The LM5066I uses simple averaging. This is accomplished by summing consecutive results up to the number programmed, then dividing by the number of samples. Averaging is calculated according to the following sequence:

$$Y = (X_{(N)} + X_{(N-1)} + ... + X_{(0)}) / N \quad (3)$$

When the averaging has reached the end of a sequence (for example, 4096 samples are averaged), then a whole new sequence begins that requires the same number of samples (in this example, 4096) to be taken before the new average is ready.

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Table 37. SAMPLES_FOR_AVG Register

AVGN (b)	N = 2^{AVGN}	Averaging / Register Update Period (ms)
0000b	1	1
0001b	2	2
0010b	4	4
0011b	8	8
0100b	16	16
0101b	32	32
0110b	64	64
0111b	128	128
1000b	256	256
1001b	512	512
1010b	1024	1024
1011b	2048	2048
1100b	4096	4096

Note that a change in the SAMPLES_FOR_AVG register is not reflected in the average telemetry measurements until the present averaging interval has completed. The default setting for AVGN is 1000b, or 08h.

The SAMPLES_FOR_AVG register is accessed with the PMBus read/write byte protocol.

Table 38. SAMPLES_FOR_AVG Register

VALUE	MEANING	DEFAULT
00h to 0Ch	Exponent (AVGN) for number of samples to average over	00h

8.5.3.13 MFR_SPECIFIC_12: READ_AVG_VIN (DCh)

The READ_AVG_VIN command reports the 12-bit ADC measured input average voltage. If the data is not ready, the returned value is the previous averaged data. However, if there is no previously averaged data, the default value (0000h) is returned. This data is read with the PMBus read word protocol. This register should use the coefficients shown in Table 47.

Table 39. READ_AVG_VIN Register

VALUE	MEANING	DEFAULT
0000h to 0FFFh	Average of measured values for input voltage	0000h

8.5.3.14 MFR_SPECIFIC_13: READ_AVG_VOUT (DDh)

The READ_AVG_VOUT command reports the 12-bit ADC measured current sense average voltage. The returned value is the default value (0000h) or previous data when the average data is not ready. This data is read with the PMBus read word protocol. This register should use the coefficients shown in Table 47.

Table 40. READ_AVG_VOUT Register

VALUE	MEANING	DEFAULT
0000h to 0FFFh	Average of measured values for output voltage	0000h

8.5.3.15 MFR_SPECIFIC_14: READ_AVG_IIN (DEh)

The READ_AVG_IIN command reports the 12-bit ADC measured current sense average voltage. The returned value is the default value (0000h) or previous data when the average data is not ready. This data is read with the PMBus read word protocol. This register should use the coefficients shown in Table 47.

Table 41. READ_AVG_IIN Register

VALUE	MEANING	DEFAULT
0000h to 0FFFh	Average of measured values for current sense voltage	0000h

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8.5.3.16 MFR_SPECIFIC_14: READ_AVG_PIN (DFh)

The READ_AVG_PIN command reports the 12-bit ADC measured VIN x IIN product. The returned value is the default value (0000h) or previous data when the average data is not ready. This data is read with the PMBus read word protocol. This register should use the coefficients shown in Table 47.

Table 42. READ_AVG_IIN Register

VALUE	MEANING	DEFAULT
0000h to 0FFFh	Average of measured values for current sense voltage	0000h

8.5.3.17 MFR_SPECIFIC_15: READ_AVG_PIN

The READ_AVG_PIN command reports the upper 12-bits of the average VIN × IIN product as measured by the 12-bit ADC. The user can read the default value (0000h) or previous data when the average data is not ready. This data is read with the PMBus read word protocol. This register should use the coefficients shown in Table 47.

Table 43. READ_AVG_PIN Register

VALUE	MEANING	DEFAULT
0000h to 0FFFh	Average of measured value for input voltage x input current sense voltage	0000h

8.5.3.18 MFR_SPECIFIC_16: BLACK_BOX_READ (E0h)

The BLACK BOX READ command retrieves the BLOCK READ data which was latched in at the first assertion of SMBA by the LM5066I. It is re-armed with the CLEAR_FAULTS command. It is the same format as the BLOCK_READ registers, the only difference is that its contents are updated with the SMBA edge rather than the internal clock edge. This command is read with the PMBus block read protocol.

8.5.3.19 MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h)

The READ_DIAGNOSTIC_WORD PMBus command reports all of the LM5066I faults and warnings in a single read operation. The standard response to the assertion of the SMBA signal of issuing multiple read requests to various status registers can be replaced by a single word read to the DIAGNOSTIC_WORD register. The READ_DIAGNOSTIC_WORD command should be read with the PMBus read word protocol. The READ_DIAGNOSTIC_WORD is also returned in the BLOCK_READ, BLACK_BOX_READ, and AVG_BLOCK_READ operations. Note that if UVLO is pulled low to shutt OFF the FET, the diagnostic word will return 08E0h.

Table 44. DIAGNOSTIC_WORD Format

BIT	MEANING	DEFAULT
15	VOUT_UNDERVOLTAGE_WARN	0
14	IIN_OP_WARN	0
13	VIN_UNDERVOLTAGE_WARN	0
12	VIN_OVERVOLTAGE_WARN	0
11	POWER GOOD	1
10	OVER_TEMPERATURE_WARN	0
9	TIMER_LATCHED_OFF	0
8	EXT_MOSFET_SHORTED	0
7	CONFIG_PRESET	1
6	DEVICE_OFF	0
5	VIN_UNDERVOLTAGE_FAULT	0
4	VIN_OVERVOLTAGE_FAULT	0
3	IIN_OC/PFET_OP_FAULT	0
2	OVER_TEMPERATURE_FAULT	0
1	CML_FAULT	0
0	CIRCUIT_BREAKER_FAULT	0

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8.5.3.20 MFR_SPECIFIC_18: AVG_BLOCK_READ (E2h)

The AVG_BLOCK_READ command concatenates the DIAGNOSTIC_WORD with input and output average telemetry information (IIN, VOUT, VIN, and PIN) and temperature to capture all of the operating information of the part in a single PMBus transaction. The block is 12-bytes long with telemetry information sent out in the same manner as if an individual READ_AVG_XXX command had been issued (shown in Table 45). AVG_BLOCK_READ also specifies that the VIN, VOUT, and IIN measurements are all time-aligned whereas there is a chance they may not be if read with individual PMBus commands. To read data from the AVG_BLOCK_READ command, use the SMBus block read protocol.

Table 45. AVG_BLOCK_READ Register Format

Byte Count (Always 12)	(1 Byte)
DIAGNOSTIC_WORD	(1 word)
AVG_IIN	(1 word)
AVG_VOUT	(1 word)
AVG_VIN	(1 word)
AVG_PIN	(1 word)
TEMPERATURE	(1 word)

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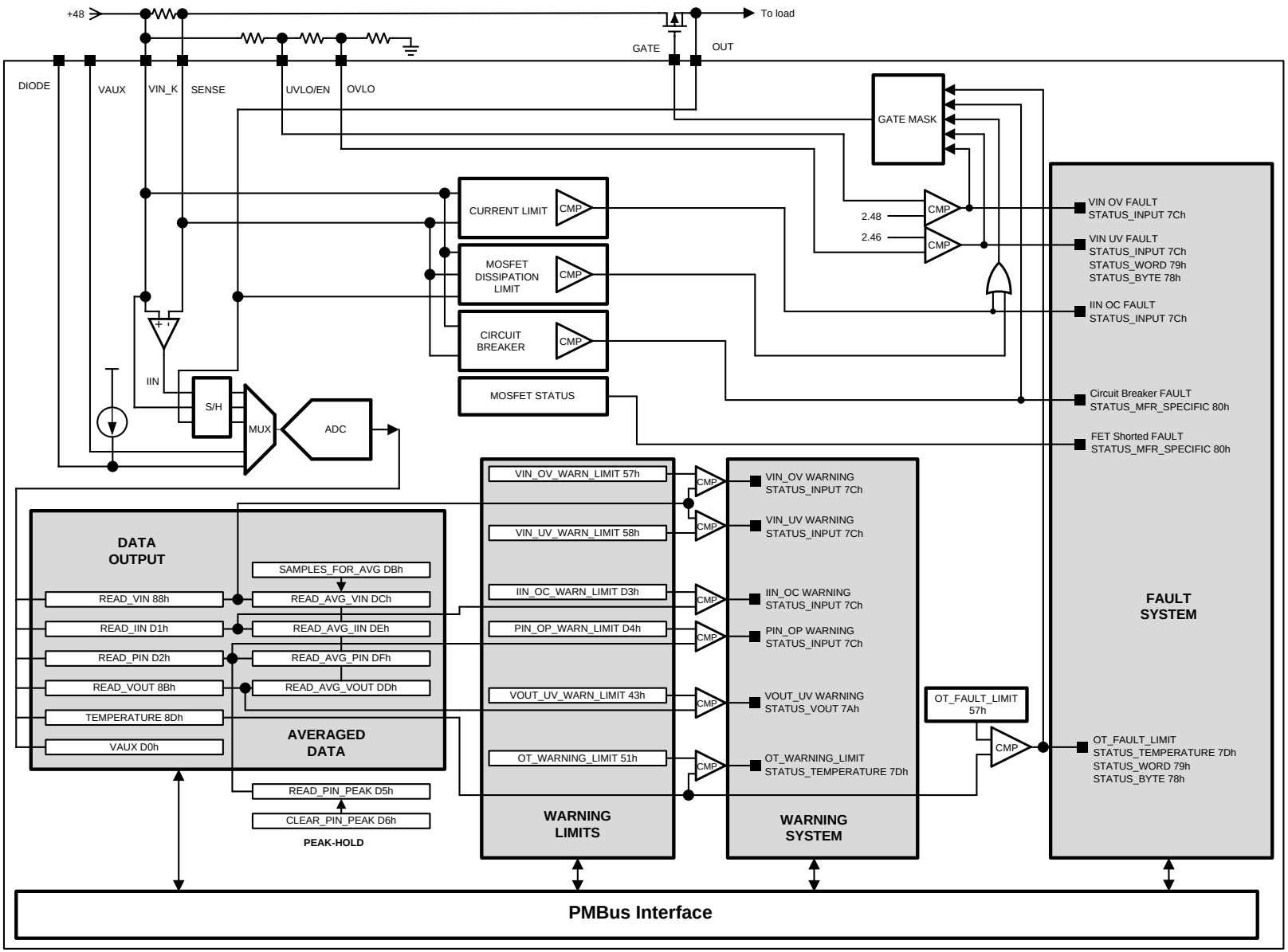


Figure 17. Command / Register and Alert Flow Diagram

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8.5.4 Reading and Writing Telemetry Data and Warning Thresholds

All measured telemetry data and user-programmed warning thresholds are communicated in 12-bit two's complement binary numbers read or written in 2-byte increments conforming to the direct format as described in section 8.3.3 of the *PMBus Power System Management Protocol Specification 1.1* (Part II). The organization of the bits in the telemetry or warning word is shown in Table 46, where Bit_11 is the most significant bit (MSB) and Bit_0 is the least significant bit (LSB). The decimal equivalent of all warning and telemetry words are constrained to be within the range of 0 to 4095, with the exception of temperature. The decimal equivalent value of the temperature word ranges from 0 to 65535.

Table 46. Telemetry and Warning Word Format

Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0
2	0	0	0	0	Bit_11	Bit_10	Bit_9	Bit_8

Conversion from direct format to real-world dimensions of current, voltage, power, and temperature is accomplished by determining appropriate coefficients as described in section 7.2.1 of the *PMBus Power System Management Protocol Specification 1.1* (Part II). According to this specification, the host system converts the values received into a reading of volts, amperes, watts, or other units using the following relationship:

$$x = \frac{1}{m}\left(Y \times 10^{-R} - b\right) \quad (4)$$

where

- **X** = The calculated real-world value (volts, amps, watt, and so forth)
- **m** = The slope coefficient
- **Y** = A 2-byte two's complement integer received from device
- **b** = The offset, a 2-byte two's complement integer
- **R** = The exponent, a 1-byte two's complement integer

R is only necessary in systems where m is required to be an integer (for example, where m may be stored in a register in an integrated circuit). In those cases, R only needs to be large enough to yield the desired accuracy.

Table 47. Telemetry and Warning Conversion Coefficients

Commands	Condition	Format	Number of Data Bytes	m	b	R	Unit
READ_VIN, READ_AVG_VIN VIN_OV_WARN_LIMIT VIN_UV_WARN_LIMIT		DIRECT	2	4617	–140.0	–2	V
READ_VOUT, READ_AVG_VOUT VOUT_UV_WARN_LIMIT		DIRECT	2	4602	500.0	–2	V
READ_VAUX		DIRECT	2	13774	73.0	–1	V
READ_IIN, READ_AVG_IIN(1) MFR_IIN_OC_WARN_LIMIT	CL = VDD	DIRECT	2	15076	-503.9	–2	A
READ_IN, READ_AVG_IN(1) MFR_IIN_OC_WARN_LIMIT	CL = GND	DIRECT	2	7645	100	–2	A
READ_PIN, READ_AVG_PIN(1), READ_PIN_PEAK MFR_PIN_OP_WARN_LIMIT	CL = VDD	DIRECT	2	1701	–4000	–3	W
READ_PIN, READ_AVG_PIN(1), READ_PIN_PEAK MFR_PIN_OP_WARN_LIMIT	CL = GND	DIRECT	2	860.6	–965	–3	W
READ_TEMPERATURE_1 OT_WARN_LIMIT OT_FAULT_LIMIT		DIRECT	2	16000	0	–3	°C

(1) The coefficients relating to current/power measurements and warning thresholds shown are normalized to a sense resistor (R_S) value of 1 mΩ. In general, the current or power coefficients can be calculated using the relationships shown in Table 48.

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Table 48. Current and Power Telemetry and Warning Conversion Coefficients (R_S in mΩ)

Commands	Condition	Format	Number of Data Bytes	m	b	R	Unit
READ_IIN, READ_AVG_IIN(1) MFR_IIN_OC_WARN_LIMIT	CL = VDD	DIRECT	2	15076 × R_S	–503.9	–2	A
READ_IIN, READ_AVG_IIN(1) MFR_IIN_OC_WARN_LIMIT	CL = GND	DIRECT	2	7645 × R_S	100.0	–2	A
READ_PIN, READ_AVG_PIN(1), READ_PIN_PEAK MFR_PIN_OP_WARN_LIMIT	CL = VDD	DIRECT	2	1701 × R_S	–4000	–3	W
READ_PIN, READ_AVG_PIN(1), READ_PIN_PEAK MFR_PIN_OP_WARN_LIMIT	CL = GND	DIRECT	2	860.6 × R_S	–965.0	–3	W

(1) The coefficients relating to current/power measurements and warning thresholds shown are normalized to a sense resistor (R_S) value of 1 mΩ. In general, the current or power coefficients can be calculated using the relationships shown in Table 48.

Take care to adjust the exponent coefficient, R, such that the value of m remains within the range of –32768 to 32767. For example, if a 5-mΩ sense resistor is used, the correct coefficients for the READ_IIN command with CL = VDD would be m = 7553, b = –65, R = –1.

8.5.5 Determining Telemetry Coefficients Empirically With Linear Fit

The coefficients for telemetry measurements and warning thresholds presented in Table 47 are adequate for the majority of applications. Current and power coefficients are dependent on R_{SNS} and must be calculated per application. Table 48 provides the equations necessary for calculating the current and power coefficients for the general case. These were obtained by characterizing multiple units over temperature and are considered optimal. The small signal nature of the current and power measurement makes it more susceptible to PCB parasitics than other telemetry channels. In addition there is some variation in R_{SNS} and the LM5066I itself. This may cause slight variations in the optimum coefficients (m, b, and R) for converting from digital values to real world values (for example, amps and watts). To maximize telemetry accuracy, the coefficients can be calibrated for a given board using empirical methods. This would determine optimum coefficients to cancel out the error from PCB parasitics, R_{SNS} variation, and the variation of LM5066I. It is not considered good practice to take measurements on one board and use the computed coefficients for all units in production, because the R_{SNS} and the LM5066I on a given board are randomly chosen and do not represent a statistical mean. It is recommended to either calibrate all boards individually or to use the recommended coefficients from Table 48.

The optimal current coefficients for a specific board can be determined using the following method:

1. While the LM5066I is in normal operation, measure the voltage across the sense resistor using Kelvin test points and a high accuracy DVM while controlling the load current. Record the integer value returned by the READ_AVG_IIN command (with the SAMPLES_FOR_AVG set to a value greater than 0) for two or more voltages across the sense resistor. For best results, the individual READ_AVG_IIN measurements should span nearly the full-scale range of the current (for example, voltage across R_{SNS} of 5 and 20 mV).
2. Convert the measured voltages to currents by dividing them by the value of R_{SNS}. For best accuracy, the value of R_{SNS} should be measured. Table 49 assumes a sense resistor value of 5 mΩ.

Table 49. Measurements for Linear Fit Determination of Current Coefficients

Measured Voltage Across R_S (V)	Measured Current (A)	READ_AVG_IIN (Integer Value)
0.005	1	568
0.01	2	1108
0.02	4	2185

3. Using the spreadsheet (or a math program) determine the slope and the y-intercept of the data returned by the READ_AVG_IIN command versus the measured current. For the data shown in Table 47:
   - READ_AVG_IN value = slope × (Measured Current) + (y-intercept)
   - Slope = 538.9
   - Y-intercept = 29.5
4. To determine the **m** coefficient, simply shift the decimal point of the calculated slope to arrive at integer with a suitable number of significant digits for accuracy (typically 4) while staying with the range of –32768 to 32767. This shift in the decimal point equates to the **R** coefficient. For the slope value shown in the previous

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step, the decimal point would be shifted to the right once hence **R** = –1.

5. After the **R** coefficient has been determined, the **b** coefficient is found by multiplying the y-intercept by 10^{-R}. In this case the value of **b** = 295.
   - Calculated current coefficients:
   - **m** = 5389
   - **b** = 295
   - **R** = –1

$$x = \frac{1}{m}\left(Y \times 10^{-R} - b\right)$$

where

- **X =** The calculated real-world value (volts, amps, watts, temperature)
- **m** = The slope coefficient, is the 2-byte, two's complement integer
- **Y** = A 2-byte two's complement integer received from device
- **b** = The offset, a 2-byte two's complement integer
- **R** = The exponent, a 1-byte two's complement integer (5)

This procedure can be repeated to determine the coefficients of any telemetry channel simply by substituting measured current for some other parameter (for example, power or voltage).

8.5.6 Writing Telemetry Data

There are several locations that require writing data if their optional usage is desired. Use the same coefficients previously calculated for your application, and apply them using this method as prescribed by the PMBus revision section 7.2.2 *Sending a Value*

$$Y = \left(mX + b\right) \times 10^{R}$$

where

- **X** = The calculated real-world value (volts, amps, watts, temperature)
- **m** = The slope coefficient is the 2-byte, two's complement integer
- **Y** = A 2-byte two's complement integer received from device
- **b** = The offset, a 2-byte two's complement integer
- **R** = The exponent, a 1-byte two's complement integer (6)

8.5.7 PMBus Address Lines (ADR0, ADR1, ADR2)

The three address lines are to be set high (connect to VDD), low (connect to GND), or open to select one of 27 addresses for communicating with the LM5066I. Table 50 depicts 7-bit addresses (eighth bit is read/write bit).

Table 50. Device Addressing

ADR2	ADR1	ADR0	DECODED ADDRESS
Z	Z	Z	40h
Z	Z	0	41h
Z	Z	1	42h
Z	0	Z	43h
Z	0	0	44h
Z	0	1	45h
Z	1	Z	46h
Z	1	0	47h
Z	1	1	10h
0	Z	Z	11h
0	Z	0	12h
0	Z	1	13h
0	0	Z	14h

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Table 50. Device Addressing (continued)

ADR2	ADR1	ADR0	DECODED ADDRESS
0	0	0	15h
0	0	1	16h
0	1	Z	17h
0	1	0	50h
0	1	1	51h
1	Z	Z	52h
1	Z	0	53h
1	Z	1	54h
1	0	Z	55h
1	0	0	56h
1	0	1	57h
1	1	Z	58h
1	1	0	59h
1	1	1	5Ah

8.5.8 $\overline{\text{SMBA}}$ Response

The $\overline{\text{SMBA}}$ effectively has two masks:

- The alert mask register at D8h
- The ARA automatic mask.

The ARA automatic mask is a mask that is set in response to a successful ARA read. An ARA read operation returns the PMBus address of the lowest addressed part on the bus that has its $\overline{\text{SMBA}}$ asserted. A successful ARA read means that this part was the one that returned its address. When a part responds to the ARA read, it releases the $\overline{\text{SMBA}}$ signal. When the last part on the bus that has an $\overline{\text{SMBA}}$ set has successfully reported its address, the $\overline{\text{SMBA}}$ signal de-asserts.

The way that the LM5066I releases the $\overline{\text{SMBA}}$ signal is by setting the ARA automatic mask bit for all fault conditions present at the time of the ARA read. All status registers will still the fault condition, but it does not generate a $\overline{\text{SMBA}}$ on that fault again until the ARA automatic mask is cleared by the host issuing a CLEAR_FAULTS command to this part. This should be done as a routine part of servicing an $\overline{\text{SMBA}}$ condition on a part, even if the ARA read is not done. Figure 18 depicts a schematic version of this flow.

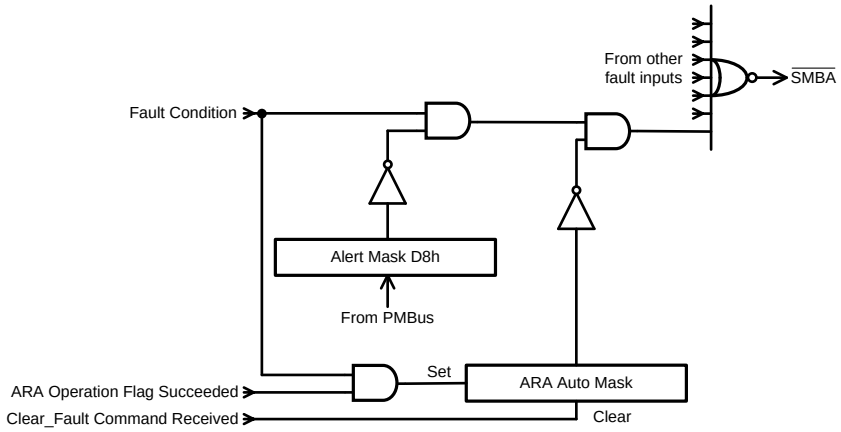


Figure 18. Typical Flow Schematic for $\overline{\text{SMBA}}$ Fault

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9 Application and Implementation

9.1 Application Information

The LM5066I is a hotswap with a PMBus interface that provides current, voltage, power, and status information to the host. As a hotswap, it is used to manage inrush current and protect in case of faults.

When designing a hotswap, three key scenarios should be considered:

- Start-up
- Output of a hotswap is shorted to ground when the hotswap is on. This is often referred to as a hot-short.
- Powering-up a board when the output and ground are shorted. This is usually called a start-into-short.

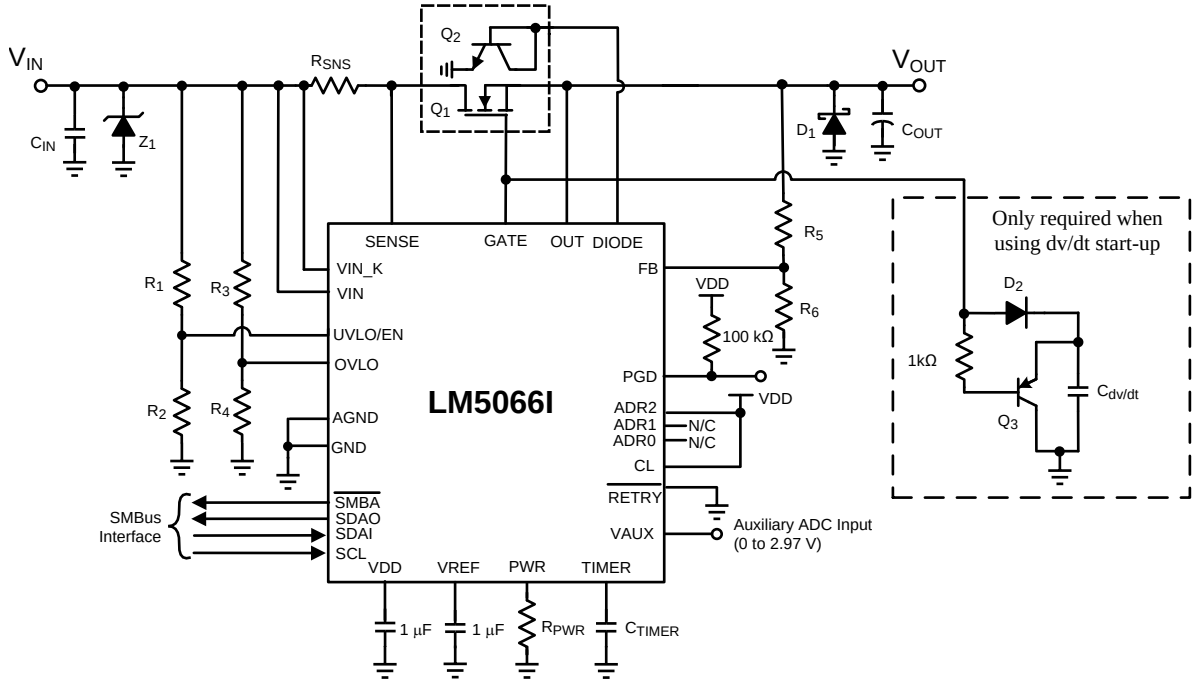
All of these scenarios place a lot of stress on the hotswap MOSFET and take special care when designing the hotswap circuit to keep the MOSFET within its SOA. Detailed design examples are provided in the following sections. Solving all of the equations by hand is cumbersome and can result in errors. Instead, TI recommends to use the LM5066I Design Calculator provided on the product page.

9.2 Typical Application

This section shows two application examples. The requirements are the same, except the second design requires twice the current and twice the output capacitance. In the 20A design example, a regular design is attempted using a power limiting based start-up. Unfortunately this results in insufficient margin and the final design relies on a dv/dt based start-up.

9.2.1 48-V, 10-A PMBus Hotswap Design

This section describes the design procedure for a 48-V, 10-A PMBUS hotswap design.



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Figure 19. Typical Application Circuit

9.2.1.1 Design Requirements

Table 51 summarizes the design parameters that must be known before designing a hotswap circuit. When charging the output capacitor through the hotswap MOSFET, the FET's total energy dissipation equals the total energy stored in the output capacitor ($1 / 2CV^2$). Thus, both the input voltage and output capacitance determine the stress experienced by the MOSFET. The maximum load current drives the current limit and sense resistor selection. In addition, the maximum load current, maximum ambient temperature, and thermal properties of the

Typical Application (continued)

PCB ($R_{\theta CA}$) drive the selection of the MOSFET R_{DSON} and the number of MOSFETs used. $R_{\theta CA}$ is a strong function of the layout and the amount of copper that is connected to the drain of the MOSFET. Note that the drain is not electrically connected to the ground plane, and thus the ground plane cannot be used to help with heat dissipation. This design example uses $R_{\theta CA}$ = 30°C/W, which is similar to the LM5066I EVM. It is a good practice to measure the $R_{\theta CA}$ of a given design after the physical PCBs are available.

Finally, it is important to understand what test conditions the hotswap needs to pass. In general, a hotswap is designed to pass both a hot-short and a start into a short, which are described in the previous section. Also, TI recommends to keep the load OFF until the hotswap is fully powered-up. Starting the load early causes unnecessary stress on the MOSFET and could lead to MOSFET failures or a failure to start-up.

Table 51. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	40 to 60 V
Maximum load current	10 A
Maximum output capacitance of the hotswap	220 µF
Maximum ambient temperature	85°C
MOSFET $R_{\theta CA}$ (function of layout)	30°C/W
Pass hot-short on output?	Yes
Pass a start into short?	Yes
Is the load off until PG asserted?	Yes
Can a hot board be plugged back in?	Yes

9.2.1.2 Detailed Design-In Procedure

9.2.1.2.1 Select R_{SNS} and CL Setting

LM5066I can be used with a VCL of 26 or 50 mV. Using the 26-mV threshold results in a lower R_{SNS} and lower I^2R losses. The 26-mV option is selected for this design by connecting the CL pin directly to V_{DD}. TI recommends to target a current limit that is at least 10% above the maximum load current to account for the tolerance of the LM5066I current limit. Targeting a current limit of 11 A, the sense resistor can be computed as follows:

$$R_{SNS,CLC} = \frac{I_{LIM}}{V_{CL}} = \frac{26mV}{11A} = 2.36m\Omega \quad (7)$$

Typically, sense resistors are only available in discrete values. If a precise current limit is desired, a sense resistor along with a resistor divider can be used as shown in Figure 20.

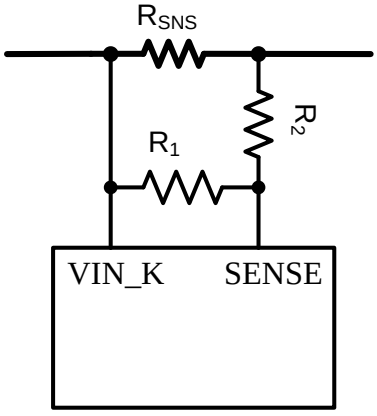


Figure 20. SENSE Resistor Divider

The next larger available sense resistor should be chosen (3 mΩ in this case). The ratio of R_1 and R_2 can be computed as follows:

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$$\frac{R_1}{R_2} = \frac{R_{SNS,CLC}}{R_{SNS} - R_{SNS,CLC}} = \frac{2.36m\Omega}{3m\Omega - 2.36m\Omega} = 3.69 \quad (8)$$

Note that the SENSE pin pulls 25 μA of current, which creates an offset across R_2. TI recommends to keep R_2 below 10 Ω to reduce the offset that this introduces. In addition, the 1% resistors add to the current monitoring error. Finally, if the resistor divider approach is used, the user should compute the effective sense resistance ($R_{SNS,EFF}$) using Equation 9 and use that in all equations instead of R_{SNS}.

$$R_{SNS,EFF} = \frac{R_{SNS} \times R_1}{R_1 + R_2} \quad (9)$$

Note that for many applications, a precise current limit may not be required. In that case, it is simpler to pick the next smaller available sense resistor. For this application, a 2-mΩ resistor can be used for a 13-A current limit.

9.2.1.2.2 Selecting the Hotswap FETs

It is critical to select the correct MOSFET for a hotswap design. The device must meet the following requirements:

- The V_{DS} rating should be sufficient to handle the maximum system voltage along with any ringing caused by transients. For most 48-V systems, a 100-V FET is a good choice.
- The SOA of the FET should be sufficient to handle all usage cases: start-up, hot-short, and start into short.
- R_{DSON} should be sufficiently low to maintain the junction and case temperature below the maximum rating of the FET. In fact, TI recommends to keep the steady-state FET temperature below 125°C to allow margin to handle transients.
- Maximum continuous current rating should be above the maximum load current and the pulsed-drain current must be greater than the current threshold of the circuit breaker. Most MOSFETs that pass the first three requirements also pass these two.
- A V_{GS} rating of ±20 V is required because the LM5066I can pull up the gate as high as 16 V above source.

For this design, the PSMN4R8-100BSE was selected for its low R_{DSON} and superior SOA. After selecting the MOSFET, the maximum steady-state case temperature can be computed as follows:

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times I^2_{LOAD,MAX} \times R_{DSON}(T_J) \quad (10)$$

Note that the R_{DSON} is a strong function of junction temperature, which for most D2PACK MOSFETs is very close to the case temperature. A few iterations of the previous equations may be necessary to converge on the final R_{DSON} and $T_{C,MAX}$ value. According to the PSMN4R8-100BSE data sheet, it's R_{DSON} doubles at 110°C. Equation 11 uses this R_{DSON} value to compute the $T_{C,MAX}$. Note that the computed $T_{C,MAX}$ is close to the junction temperature assumed for R_{DSON}. Thus, no further iterations are necessary.

$$T_{C,MAX} = 85°C + 30° \frac{C}{W} \times (10A)^2 \times (2 \times 4.8m\Omega) = 114°C \quad (11)$$

9.2.1.2.3 Select Power Limit

In general, a lower power limit setting is preferred to reduce the stress on the MOSFET. However, when the LM5066I is set to a very-low power limit setting, it has to regulate the FET current and hence the voltage across the sense resistor (V_{SNS}) to a very-low value. V_{SNS} can be computed as shown in Equation 12.

$$V_{SNS} = \frac{P_{LIM} \times R_{SNS}}{V_{DS}} \quad (12)$$

To avoid significant degradation of the power limiting, TI does not recommend a V_{SNS} of less than 4 mV. Based on this requirement, the minimum allowed power limit can be computed as follows:

$$P_{LIM,MIN} = \frac{V_{SNS,MIN} \times V_{IN,MAX}}{R_{SNS}} = \frac{4mV \times 60V}{2m\Omega} = 120W \quad (13)$$

In most applications, the power limit can be set to $P_{LIM,MIN}$ using Equation 14. Here R_{SNS} and R_{PWR} are in ohms and P_{LIM} is in watts.

$$R_{PWR} = \frac{P_{LIM} \times R_{SNS} - 0.043}{7 \times 10^{-6}} = \frac{120 \times 0.002 - 0.043}{7 \times 10^{-6}} = 28143\Omega \quad (14)$$

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The closest available resistor should be selected. In this case, a 28.2-kΩ resistor was chosen.

9.2.1.2.4 Set Fault Timer

The fault timer runs when the hotswap is in power limit or current limit, which is the case during start-up. Thus, the timer has to be sized large enough to prevent a time-out during start-up. If the part starts directly into current limit ($I_{LIM} \times V_{DS} < P_{LIM}$), the maximum start time can be computed with Equation 15.

$$t_{start,max} = \frac{C_{OUT} \times V_{IN,MAX}}{I_{LIM}} \tag{15}$$

For most designs (including this example), $I_{LIM} \times V_{DS} > P_{LIM}$, so the hotswap starts in power limit and transitions into current limit. In that case, the maximum start time can be computed as in Equation 16.

$$t_{start,max} = \frac{C_{OUT}}{2} \times \left[\frac{V_{IN,MAX}^2}{P_{LIM}} + \frac{P_{LIM}}{I_{LIM}^2} \right] = \frac{220\mu F}{2} \times \left[\frac{(60V)^2}{120W} + \frac{120W}{(13A)^2} \right] = 3.38ms \tag{16}$$

Note that the above start-time is based on typical current limit and power limit values. To ensure that the timer never times out during start-up, TI recommends to set the fault time (t_{flt}) to be 1.5 × $t_{start,max}$ or 5.1 ms. This accounts for the variation in power limit, timer current, and timer capacitance. Thus, C_{TIMER} can be computed as follows:

$$C_{TIMER} = \frac{t_{flt} \times i_{timer}}{v_{timer}} = \frac{5.1ms \times 75\mu A}{3.9V} = 98.07nF \tag{17}$$

The next largest standards capacitor value for C_{TIMER} is chosen as 100 nF. After C_{TIMER} is chosen, the actual programmed fault time can be computed as follows:

$$t_{flt} = \frac{C_{TIMER} \times v_{timer}}{i_{timer}} = \frac{100nF \times 3.9V}{75\mu A} = 5.2ms \tag{18}$$

9.2.1.2.5 Check MOSFET SOA

When the power limit and fault timer are chosen, it is critical to check that the FET stays within its SOA during all test conditions. During a hot-short the circuit breaker trips and the LM5066I restarts into power limit until the timer runs out. In the worst case, the MOSFET's V_{DS} equals $V_{IN,MAX}$, I_{DS} equals P_{LIM} / $V_{IN,MAX}$ and the stress event lasts for t_{flt}. For this design example, the MOSFET has 60 V, 2 A across it for 5.2 ms.

Based on the SOA of the PSMN4R8-100BSE, it can handle 60 V, 30 A for 1 ms and it can handle 60 V, 6 A for 10 ms. For 5.2 ms, the SOA can be extrapolated by approximating SOA versus time as a power function as shown below:

$$I_{SOA}(t) = a \times t^m$$

$$m = \frac{\ln\left(I_{SOA}(t_1) / I_{SOA}(t_2)\right)}{\ln(t_1 / t_2)} = \frac{\ln\left(\frac{30A}{6A}\right)}{\ln\left(\frac{1ms}{10ms}\right)} = -0.7$$

$$a = \frac{I_{SOA}(t_1)}{t_1^m} = \frac{30A}{(1ms)^{-0.7}} = 30A \times (ms)^{0.7}$$

$$I_{SOA}(5.2ms) = 30A \times (ms)^{0.7} \times (5.2ms)^{-0.7} = 9.46A \tag{19}$$

Note that the SOA of a MOSFET is specified at a case temperature of 25°C, while the case temperature can be much hotter during a hot-short. The SOA should be de-rated based on $T_{C,MAX}$ using Equation 20:

$$I_{SOA}(5.2ms, T_{C,MAX}) = I_{SOA}(5.2ms, 25°C) \times \frac{T_{J,ABSMAX} - T_{C,MAX}}{T_{J,ABSMAX} - 25°C} = 9.46A \times \frac{175°C - 114°C}{175°C - 25°C} = 3.85A \tag{20}$$

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Based on this calculation, the MOSFET can handle 3.85 A, 60 V for 5.2 ms at elevated case temperature, but is only required to handle 2 A during a hot-short. Thus, there is good margin and the design is robust. In general, TI recommends that the MOSFET can handle 1.3× more than what is required during a hot-short. This provides margin to account for the variance of the power limit and fault time.

9.2.1.2.6 Set UVLO and OVLO Thresholds

By programming the UVLO and OVLO thresholds, the LM5066I enables the series-pass device (Q_1) when the input supply voltage (V_{IN}) is within the desired operational range. If V_{IN} is below the UVLO threshold or above the OVLO threshold, Q_1 is switched off, denying power to the load. Hysteresis is provided for each threshold.

9.2.1.2.6.1 Option A

The configuration shown in Figure 21 requires three resistors (R1 to R3) to set the thresholds.

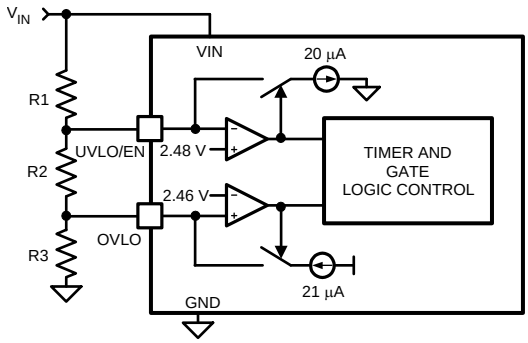


Figure 21. UVLO And OVLO Thresholds Set By R1-R3

The procedure to calculate the resistor values is as follows:

- Choose the upper UVLO threshold (V_{UVH}) and the lower UVLO threshold (V_{UVL}).
- Choose the upper OVLO threshold (V_{OVH}).
- The lower OVLO threshold (V_{OVL}) cannot be chosen in advance in this case, but is determined after the values for R1 to R3 are determined. If V_{OVL} must be accurately defined in addition to the other three thresholds, see Option B. The resistors are calculated as follows:

$$R1 = \frac{V_{UVH} - V_{UVL}}{20\mu A} = \frac{V_{UV(HYS)}}{20\mu A} \quad (21)$$

$$R3 = \frac{R1 \times V_{UVL} \times 2.46V}{V_{OVH} \times (V_{UVL} - 2.48V)} \quad (22)$$

$$R2 = \frac{2.48V \times R1}{V_{UVL} - 2.48V} - R3 \quad (23)$$

The lower OVLO threshold is calculated from:

$$V_{OVL} = \left[(R1 + R2) \times \left(\left(\frac{2.46V}{R3} \right) - 21\,\mu A \right) \right] + 2.46V \quad (24)$$

When the R1 to R3 resistor values are known, the threshold voltages and hysteresis are calculated from the following:

$$V_{UVH} = 2.48V + R1 \times \left(\frac{2.48V}{R2 + R3} + 20\ \mu A \right) \quad (25)$$

$$V_{UVL} = \frac{2.48V \times (R1 + R2 + R3)}{R2 + R3} \quad (26)$$

$$V_{UV(HYS)} = R1 \times 20\ \mu A \quad (27)$$

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$$V_{OVH} = \frac{2.46V \times (R1 + R2 + R3)}{R3} \quad (28)$$

$$V_{OVL} = \left(\frac{2.46V}{R3} - 21\ \mu A\right) \times (R1 + R2) + 2.46V \quad (29)$$

$$V_{OV(HYS)} = (R1 + R2) \times 21\ \mu A \quad (30)$$

9.2.1.2.6.2 Option B

If all four thresholds must be accurately defined, the configuration in Figure 22 can be used.

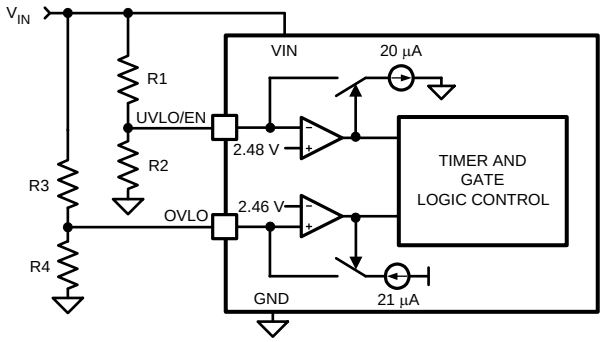


Figure 22. Programming the Four Thresholds

The four resistor values are calculated as follows:

- Choose the upper and lower UVLO thresholds (V_{UVH}) and (V_{UVL}).

$$R1 = \frac{V_{UVH} - V_{UVL}}{20\ \mu A} = \frac{V_{UV(HYS)}}{20\ \mu A} \quad (31)$$

$$R2 = \frac{2.48V \times R1}{V_{UVL} - 2.48V} \quad (32)$$

- Choose the upper and lower OVLO threshold (V_{OVH}) and (V_{OVL}).

$$R3 = \frac{V_{OVH} - V_{OVL}}{21\ \mu A} \quad (33)$$

$$R4 = \frac{2.46V \times R3}{(V_{OVH} - 2.46V)} \quad (34)$$

- When the R1 to R4 resistor values are known, the threshold voltages and hysteresis are calculated from the following:

$$V_{UVH} = 2.48V + \left[R1 \times \left(\frac{2.48V}{R2} + 20\ \mu A\right)\right] \quad (35)$$

$$V_{UVL} = \frac{2.48V \times (R1 + R2)}{R2} \quad (36)$$

$$V_{UV(HYS)} = R1 \times 20\ \mu A \quad (37)$$

$$V_{OVH} = \frac{2.46V \times (R3 + R4)}{R4} \quad (38)$$

$$V_{OVL} = 2.46V + \left[R3 \times \left(\frac{2.46V}{R4} - 21\ \mu A\right)\right] \quad (39)$$

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9.2.1.2.6.3 Option C

The minimum UVLO level is obtained by connecting the UVLO/EN pin to VIN as shown in Figure 23. Q1 is switched on when the VIN voltage reaches the POR_{EN} threshold (≅8.6 V). The OVLO thresholds are set using R3, R4. Their values are calculated using the procedure in *Option B*.

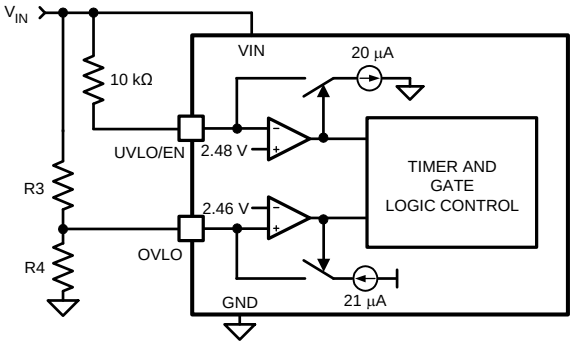


Figure 23. UVLO = POR_{EN}

9.2.1.2.6.4 Option D

The OVLO function can be disabled by grounding the OVLO pin. The UVLO thresholds are set as described in *Option B* or *Option C*.

For this design example, option B was used and the following options were targeted: V_{UVH} = 38 V, V_{UVL} = 35 V, V_{OVH} = 65 V, and V_{OVL} = 63 V. The V_{UVH} and V_{OVL} were chosen to be 5% below or above the input voltage range of 40 to 60 V to allow for some tolerance in the thresholds of the part. R1, R2, R3, and R4 are computed using the following equations:

$$R1 = \frac{V_{UVH} - V_{UVL}}{20\mu A} = \frac{38\,V - 35\,V}{20\mu A} = 150k\Omega$$

$$R2 = \frac{2.48\,V \times R1}{\left(V_{UVL} - 2.48\,V\right)} = \frac{2.48\,V \times 150k\Omega}{\left(35V - 2.48\,V\right)} = 11.44k\Omega$$

$$R3 = \frac{V_{OVH} - V_{OVL}}{21\mu A} = \frac{65\,V - 63\,V}{21\mu A} = 95.24k\Omega$$

$$R4 = \frac{2.46\,V \times R3}{\left(V_{OVH} - 2.46\,V\right)} = \frac{2.46\,V \times 95.24k\Omega}{\left(65V - 2.46\,V\right)} = 3.75k\Omega \quad (40)$$

Nearest available 1% resistors should be chosen. Set R1 = 150 kΩ, R2 = 11.5 kΩ, R3 = 95.3 kΩ, and R4 = 3.74 kΩ.

9.2.1.2.7 Power Good Pin

The Power Good indicator pin (PGD) is connected to the drain of an internal N-channel MOSFET capable of sustaining 80 V in the off-state and transients up to 100 V. An external pullup resistor is required at PGD to an appropriate voltage to indicate the status to downstream circuitry. The off-state voltage at the PGD pin can be higher or lower than the voltages at VIN and OUT. PGD is switched high when the voltage at the FB pin exceeds the PGD threshold voltage. Typically, the output voltage threshold is set with a resistor divider from output to feedback, although the monitored voltage need not be the output voltage. Any other voltage can be monitored as long as the voltage at the FB pin does not exceed its maximum rating. Referring to the *Functional Block Diagram*, when the voltage at the FB pin is below its threshold, the 20-µA current source at FB is disabled. As the output voltage increases, taking FB above its threshold, the current source is enabled, sourcing current out of the pin, raising the voltage at FB to provide threshold hysteresis. The PGD output is forced low when either the UVLO/EN pin is below its threshold or the OVLO pin is above its threshold. The status of the PGD pin can be read through the PMBus interface in either the STATUS_WORD (79h) or DIAGNOSTIC_WORD (E1h) registers.

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When the voltage at the FB pin increases above its threshold, the internal pulldown acting on the PGD pin is disabled allowing PGD to rise to V_{PGD} through the pullup resistor, R_{PG}, as shown in Figure 25. The pullup voltage (V_{PGD}) can be as high as 80 V, and can be higher or lower than the voltages at VIN and OUT. VDD is a convenient choice for V_{PGD} as it allows interface to low voltage logic and avoids glitching on PGD during power-up. If a delay is required at PGD, suggested circuits are shown in Figure 26. In Figure 26(A), capacitor C_{PG} adds delay to the rising edge, but not to the falling edge. In Figure 26(B), the rising edge is delayed by R_{PG1} + R_{PG2} and C_{PG}, while the falling edge is delayed a lesser amount by R_{PG2} and C_{PG}. Adding a diode across R_{PG2} (Figure 26(C)) allows for equal delays at the two edges, or a short delay at the rising edge and a long delay at the falling edge.

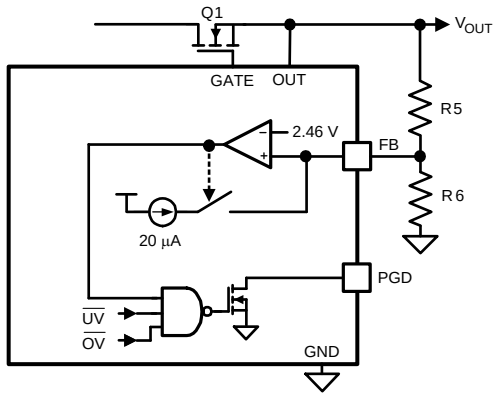


Figure 24. Programming the PGD Threshold

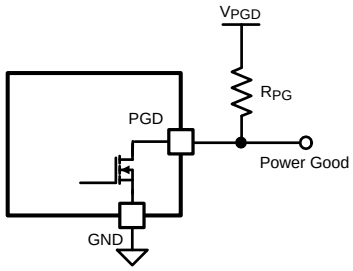


Figure 25. Power Good Output

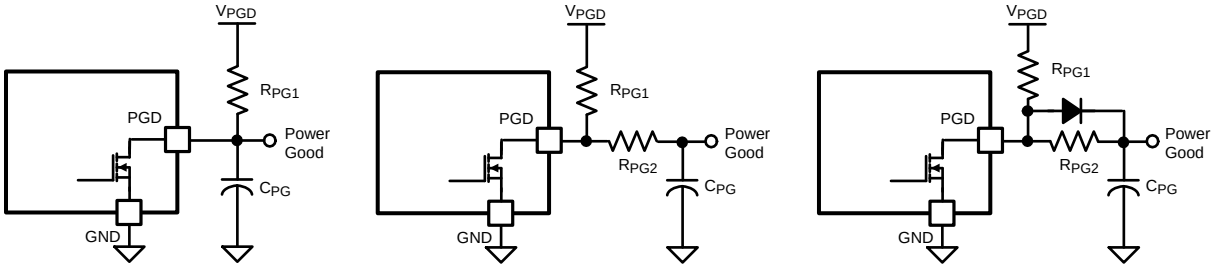


Figure 26. Adding Delay to the Power Good Output Pin

TI recommends to set the PG threshold 5% below the minimum input voltage to ensure that the PG is asserted under all input voltage conditions. For this example, PGDH of 38 V and PGDL of 35 V is targeted. R5 and R6 are computed using the following equations:

$$R5 = \frac{V_{PGDH} - V_{PGDL}}{20\mu A} = \frac{38\,V - 35\,V}{20\mu A} = 150k\Omega \quad (41)$$

$$R6 = \frac{2.46\,V \times R5}{(V_{PGDH} - 2.46\,V)} = \frac{2.46\,V \times 150k\Omega}{(38V - 2.46\,V)} = 10.38k\Omega \quad (42)$$

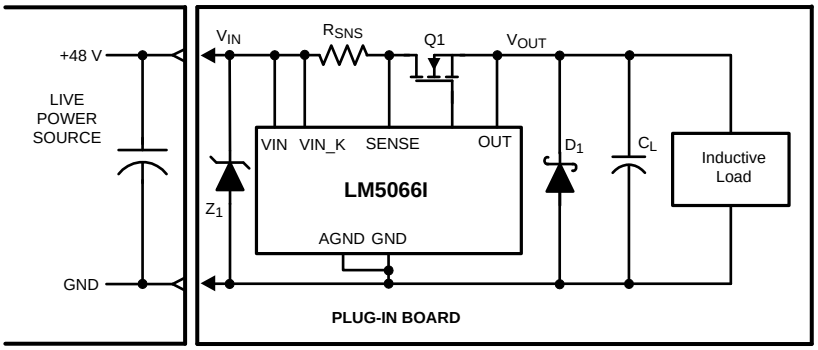
Nearest available 1% resistors should be chosen. Set R5 = 150 kΩ and R6 = 10.5 kΩ.

9.2.1.2.8 Input and Output Protection

Proper operation of the LM5066I hot swap circuit requires a voltage clamping element present on the supply side of the connector into which the hot swap circuit is plugged in. A TVS is ideal, as depicted in Figure 27. The TVS is necessary to absorb the voltage transient generated whenever the hot swap circuit shuts off the load current. This effect is the most severe during a hot-short when a large current is suddenly interrupted when the FET shutts off. The TVS should be chosen to have minimal leakage current at $V_{IN,MAX}$ and to clamp the voltage to under 100V during hot-short events. For many high power applications 5.0SMDJ60A is a good choice.

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If the load powered by the LM5066I hot swap circuit has inductive characteristics, a Schottky diode is required across the LM5066I's output, along with some load capacitance. The capacitance and the diode are necessary to limit the negative excursion at the OUT pin when the load current is shut off.



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Figure 27. Output Diode Required for Inductive Loads

9.2.1.2.9 Final Schematic and Component Values

Figure 19 shows the schematic used to implement the requirements described in the previous section. In addition, Table 52 provides the final component values that were used to meet the design requirements for a 48-V, 10-A hotswap design. The application curves in the next section are based on these component values.

Table 52. Final Component Values (48-V, 10-A Design)

COMPONENT	VALUE
R_{SNS}	2 mΩ
R1	150 kΩ
R2	11.5 kΩ
R3	95.3 kΩ
R4	3.74 kΩ
R5	150 kΩ
R6	10.5 kΩ
R_{PWR}	28.2 kΩ
Q1	PSMN4R8-100BSEJ
Q2	MMBT3904
D1	B380-13-F
Z1	5.0SMDJ60A
C_{TIMER}	100 nF
Optional dv/dt circuit	DNP

9.2.1.3 Application Curves

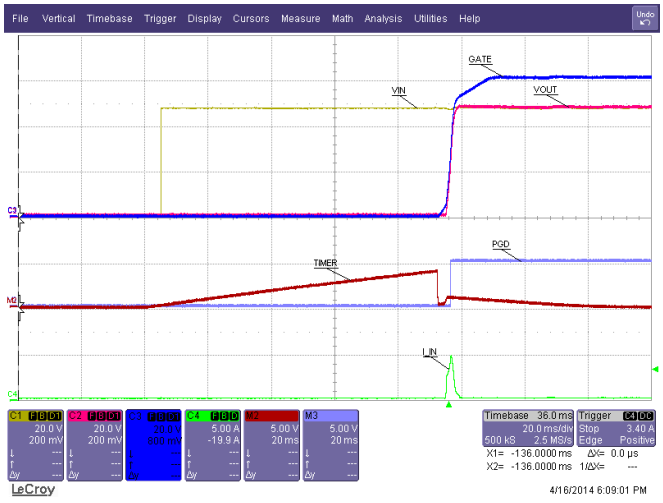
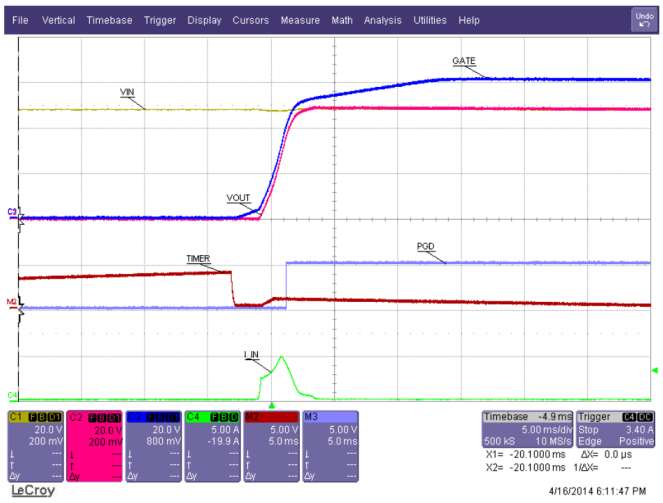
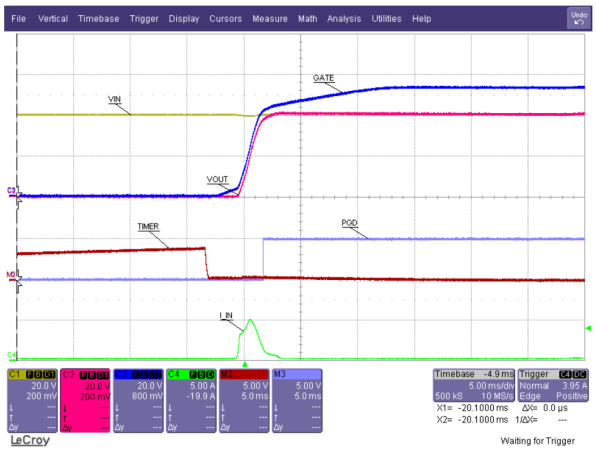


Figure 28. Insertion Delay



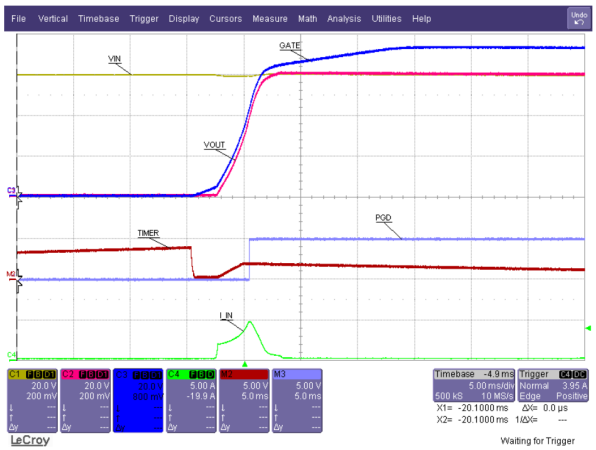
V_{IN} = 48 V

Figure 29. Start-Up



V_{IN} = 40 V

Figure 30. Start-Up



V_{IN} = 60 V

Figure 31. Start-Up

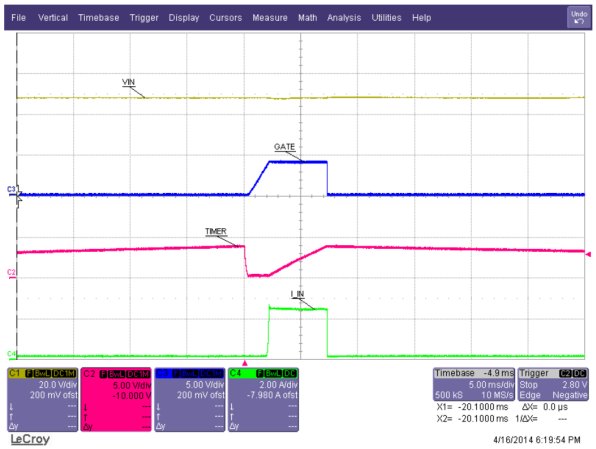


Figure 32. Start-Up into Short Circuit

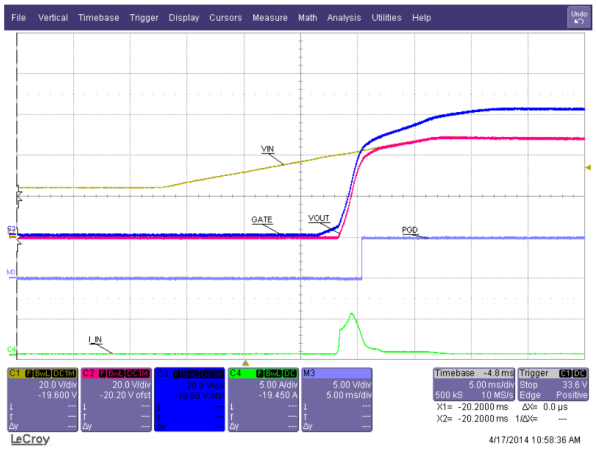


Figure 33. Under-Voltage

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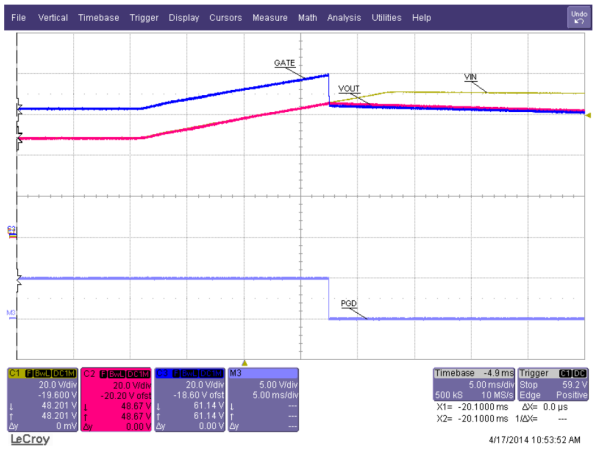


Figure 34. Over-Voltage

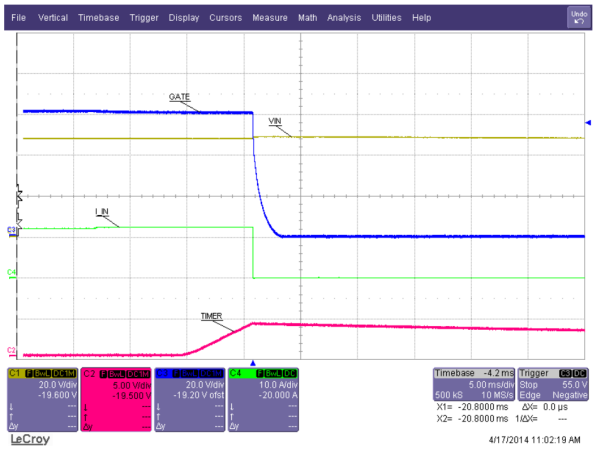


Figure 35. Gradual Over-Current

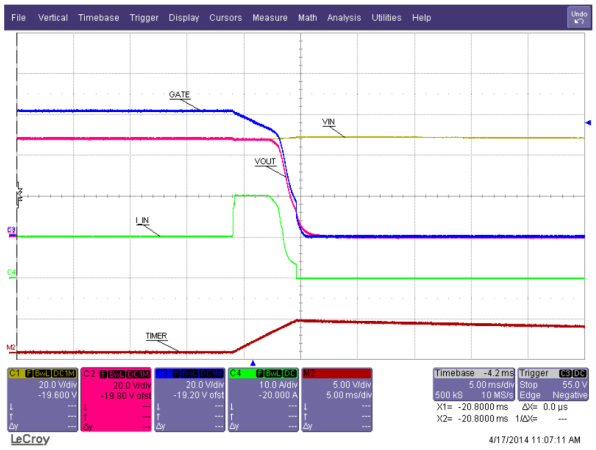


Figure 36. Loadstep

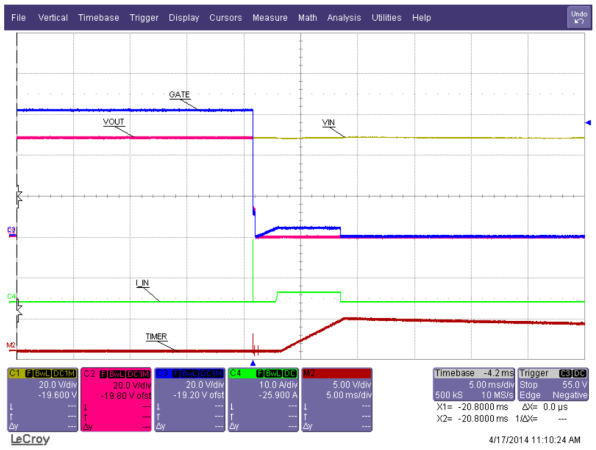


Figure 37. Hotshort on Output (Zoomed Out)

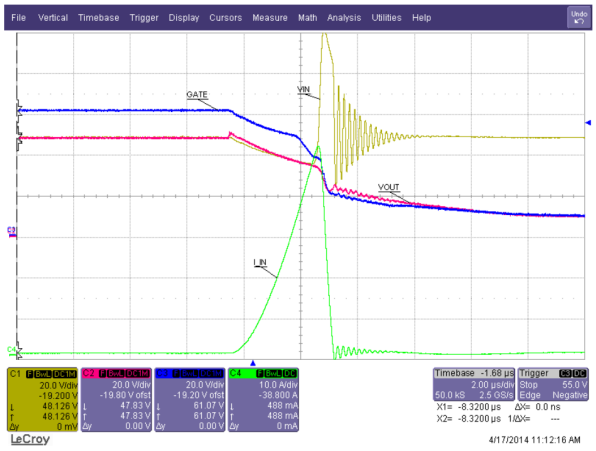


Figure 38. Hotshort on Output (Zoomed In)

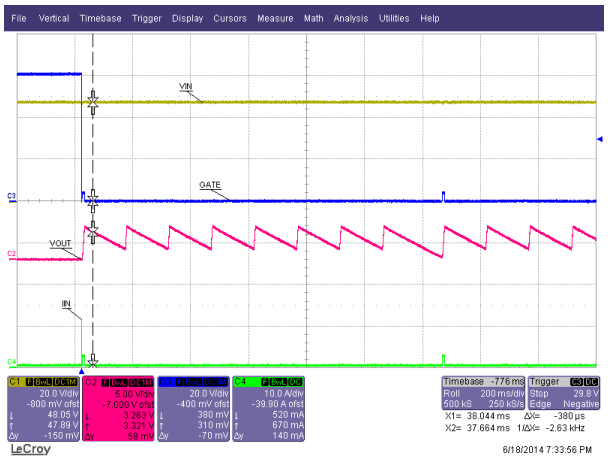
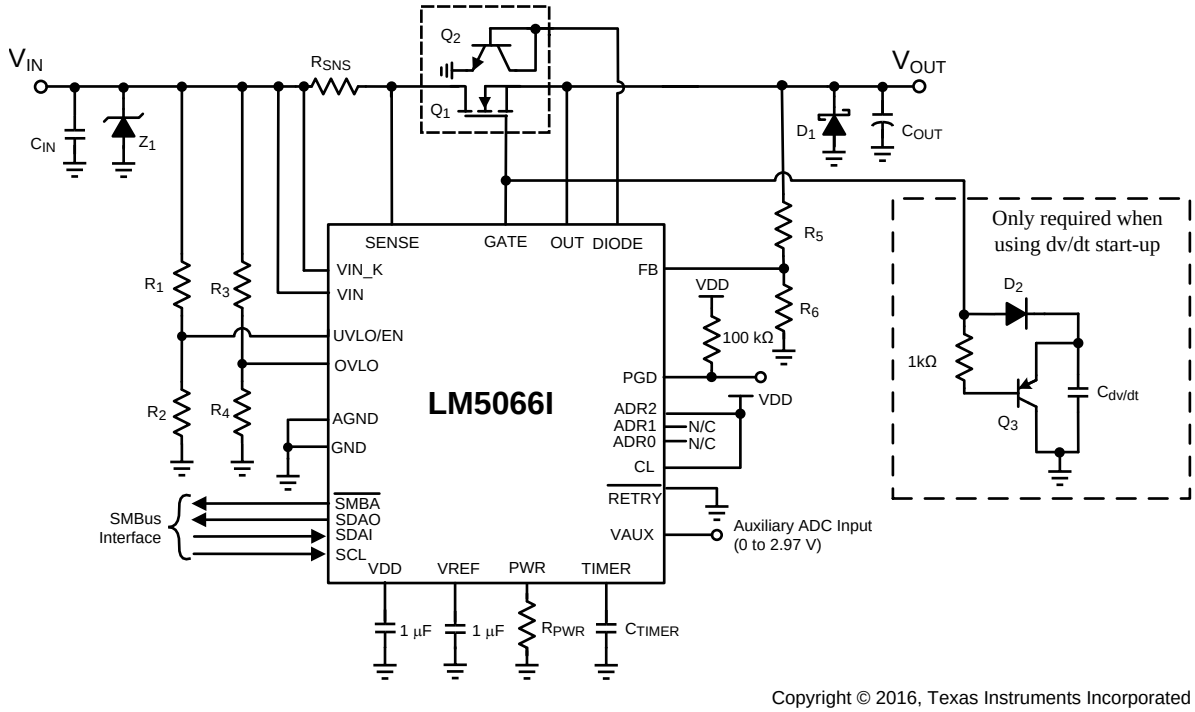


Figure 39. Auto-retry

9.2.2 48-V, 20-A PMBus Hotswap Design

This section describes the design procedure for a 48-V, 20-A PMBUS hotswap design.



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Figure 40. Typical Application Schematic, LM5066I

9.2.2.1 Design Requirements

Table 53. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	40 to 60 V
Maximum load current	20 A
Maximum output capacitance of the hotswap	440 µF
Maximum ambient temperature	85°C
MOSFET $R_{\theta CA}$ (function of layout)	30°C/W
Pass hot-short on output?	Yes
Pass a start into short?	Yes
Is the load off until PG asserted?	Yes
Can a hot board be plugged back in?	Yes

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Selecting the Sense Resistor and CL Setting

LM5066I can be used with a V_{CL} of 26 or 50 mV. In general using the 26-mV threshold results in a lower R_{SNS} and lower I^2R losses. This option is selected for this design by connecting the CL pin directly to V_{DD}. TI recommends to target a current limit that is at least 10% above the maximum load current to account for the tolerance of the LM5066I current limit. Targeting a current limit of 22 A, the sense resistor can be computed as follows:

$$R_{SNS,CLC} = \frac{I_{LIM}}{V_{CL}} = \frac{26mV}{22A} = 1.18m\Omega \quad (43)$$

For this application, a 1-mΩ resistor can be used for a 26-A current limit.

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9.2.2.2.2 Selecting the Hotswap FETs

For this design, the PSMN4R8-100BSE was selected for its low R_{DSON} and superior SOA. After selecting the MOSFET, the maximum steady-state case temperature can be computed as follows:

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times I^2_{LOAD,MAX} \times R_{DSON}(T_J) \quad (44)$$

Note that the R_{DSON} is a strong function of junction temperature, which for most D2PACK MOSFETs are very close to the case temperature. A few iterations of the previous equations may be necessary to converge on the final R_{DSON} and $T_{C,MAX}$ value. According to the PSMN4R8-100BSE data sheet, its R_{DSON} doubles at 110°C. Equation 45 uses this R_{DSON} value to compute the $T_{C,MAX}$. Note that the computed $T_{C,MAX}$ is already above the absolute maximum of the FET.

$$T_{C,MAX} = 85°C + 30° \frac{C}{W} \times (20A)^2 \times (2 \times 4.8m\Omega) = 200°C \quad (45)$$

This suggests that two FETs should be used for the design. During steady-state operation, the MOSFETs are fully enhanced and share current evenly. Thus, assuming that each FET carries half of the current, the $T_{C,MAX}$ can be computed with Equation 46. Now $T_{C,MAX}$ is 114°C, which is reasonable.

$$T_{C,MAX} = 85°C + 30° \frac{C}{W} \times \left(\frac{20A}{2}\right)^2 \times (2 \times 4.8m\Omega) = 114°C \quad (46)$$

9.2.2.2.3 Select Power Limit

In general, a lower power limit setting is preferred to reduce the stress on the MOSFET. However, when the LM5066I is set to a very-low power limit setting, it has to regulate the FET current and hence the voltage across the sense resistor (V_{SNS}) to a very-low value. V_{SNS} can be computed as shown in Equation 47.

$$V_{SNS} = \frac{P_{LIM} \times R_{SNS}}{V_{DS}} \quad (47)$$

To avoid significant degradation of the power limiting, TI does not recommend a V_{SNS} below 4 mV. Based on this requirement, the minimum allowed power limit can be computed as follows:

$$P_{LIM,MIN} = \frac{V_{SNS,MIN} \times V_{IN,MAX}}{R_{SNS}} = \frac{4mV \times 60V}{1m\Omega} = 240W \quad (48)$$

In most applications, the power limit can be set to $P_{LIM,MIN}$ as shown. Here R_{SNS} and R_{PWR} are in ohms and P_{LIM} is in watts.

$$R_{PWR} = \frac{P_{LIM} \times R_{SNS} - 0.043}{7 \times 10^{-6}} = \frac{240 \times 0.001 - 0.043}{7 \times 10^{-6}} = 28143\Omega \quad (49)$$

The closest available resistor should be selected. In this case a 28.2-kΩ resistor was chosen.

9.2.2.2.4 Set Fault Timer

The maximum start time can be computed to 3.37 ms as shown in Equation 50.

$$t_{start,max} = \frac{C_{OUT}}{2} \times \left[\frac{V^2_{IN,MAX}}{P_{LIM}} + \frac{P_{LIM}}{I^2_{LIM}}\right] = \frac{440\mu F}{2} \times \left[\frac{(60V)^2}{240W} + \frac{240W}{(26A)^2}\right] = 3.37ms \quad (50)$$

Note this start-time is based on typical current limit and power limit values. To ensure that the timer never times out during start-up, TI recommends to set the fault time (T_{FLT}) to be 1.5× $t_{start,max}$ or 5.1 ms. This accounts for the variation in power limit, timer current, and timer capacitance. Thus, C_{TIMER} can be computed as follows:

$$C_{TIMER} = \frac{t_{flt} \times i_{timer}}{v_{timer}} = \frac{5.1ms \times 75\mu A}{3.9V} = 98.07nF \quad (51)$$

The next largest available C_{TIMER} is chosen as 100 nF. After C_{TIMER} is chosen, the actual programmed fault time can be computed as follows:

$$t_{flt} = \frac{C_{TIMER} \times v_{timer}}{i_{timer}} = \frac{100nF \times 3.9V}{75\mu A} = 5.2ms \quad (52)$$

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9.2.2.2.5 Check MOSFET SOA

After the power limit and fault timer are chosen, it is critical to check that the FET stays within its SOA during all test conditions. During a hot-short, the circuit breaker trips and the LM5066I restarts into power limit until the timer runs out. In the worst case, the MOSFET's V_{DS} equals $V_{IN,MAX}$, I_{DS} equals P_{LIM} / $V_{IN,MAX}$, and the stress event lasts for t_{flt}. For this design example, the MOSFET has 60 V, 4 A across it for 5.2 ms.

When the hotswap is in power limit and the FETs are operating in saturation region (V_{GS} close to threshold voltage), the designer cannot assume that the FETs will share. Even a small V_T mismatch causes a large difference in the current carried by the two MOSFETs. Thus, the SOA checking should be done assuming that all of the current is flowing through a single FET.

Based on the SOA of the PSMN4R8-100BSE, it can handle 60 V, 30 A for 1 ms and it can handle 60 V, 6 A for 10 ms. The SOA for 5.2 ms can be extrapolated by approximating SOA versus time as a power function as shown in the following equations:

$$I_{SOA}(t) = a \times t^m$$

$$m = \frac{\ln\left(I_{SOA}(t_1) / I_{SOA}(t_2)\right)}{\ln\left(t_1 / t_2\right)} = \frac{\ln\left(\frac{30A}{6A}\right)}{\ln\left(\frac{1ms}{10ms}\right)} = -0.7$$

$$a = \frac{I_{SOA}(t_1)}{t_1^m} = \frac{30A}{(1ms)^{-0.7}} = 30A \times (ms)^{0.7}$$

$$I_{SOA}(5.2ms,\ 25°C) = 30A \times (ms)^{0.7} \times (5.2ms)^{-0.7} = 9.46A \quad (53)$$

Note that the SOA of a MOSFET is specified at a case temperature of 25°C, while the case temperature can be much hotter during a hot-short. The SOA should be de-rated based on $T_{C,MAX}$ using Equation 54.

$$I_{SOA}(5.2ms, T_{C,MAX}) = I_{SOA}(5.2ms, 25°C) \times \frac{T_{J,ABSMAX} - T_{C,MAX}}{T_{J,ABSMAX} - 25°C} = 9.46A \times \frac{175°C - 114°C}{175°C - 25°C} = 3.85A \quad (54)$$

Based on this calculation, the MOSFET can handle 3.85 A, 60 V for 5.2 ms at elevated case temperature, but it is required to handle 4 A during a hot-short. In addition, there is tolerance on the power limit and timer, so using these settings would not produce a robust hotswap design.

9.2.2.2.6 Switching to dv/dt-Based Start-Up

For designs with large load currents and output capacitances, using a power-limit-based start-up can be impractical. Fundamentally, increasing load currents reduces the sense resistor, which increases the minimum power limit. Using a larger output capacitor results in a longer start-up time and requires a longer timer. Thus, a longer timer and a larger power limit setting is required, which places more stress on the MOSFET during a hot-short or a start into short. Eventually, there will be no FETs that can support such a requirement.

To avoid this problem, a dv/dt limiting capacitor ($C_{dv/dt}$) can be used to limit the slew rate of the gate and the output voltage. The inrush current can be set arbitrarily small by reducing the slew rate of V_{OUT}. In addition, the power limit is set to satisfy the minimum power limit requirement and to keep the timer from running during start-up (make P_{LIM} / V_{INMAX} > I_{INR}). Because the timer does not run during start-up, it can be made arbitrarily small to reduce the stress that the MOSFET experiences during a start into short or a hot-short.

The D2 prevents the charge of $C_{dv/dt}$ from interfering with the power limit loop during a hot-short event and Q3 discharges $C_{dv/dt}$ when the hotswap gate comes down.

9.2.2.2.7 Choosing the V_{OUT} Slew Rate

The inrush current should be kept low enough to keep the MOSFET within its SOA during start-up. Note that the total energy dissipated in the MOSFET during start-up is constant regardless of the inrush time. Thus, stretching it out over a longer time always reduces the stress on the MOSFET as long as the load is off during start-up.

When choosing a target slew rate, one should pick a reasonable number, check the SOA, and reduce the slew rate if necessary. Using 4 V/ms as a starting point, the inrush current can be computed as follows:

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$$I_{INR} = C_{OUT} \times \frac{dV_{OUT}}{dt} = 440\mu F \times \frac{4V}{ms} = 1.76A \quad (55)$$

Assuming a maximum input voltage of 60 V, it takes 15 ms to start-up. Note that the power dissipation of the FET starts at $V_{IN,MAX} \times I_{INR}$ and reduce to 0 as the V_{DS} of the MOSFET is reduced. Note that the SOA curves assume the same power dissipation for a given time. A conservative approach is to assume an equivalent power profile where $P_{FET} = V_{IN,MAX} \times I_{INR}$ for $t = t_{start\text{-}up} / 2$. In this instance, the SOA can be checked by looking at a 60-V, 1.76-A, 7.5-ms pulse. Using the same technique as section *Check MOSFET SOA*, the MOSFET SOA can be estimated as follows:

$$I_{SOA}(7.5ms) = 30A \times (ms)^{0.7} \times (7.5ms)^{-0.7} = 7.32A \quad (56)$$

This value has to also be derated for temperature. For this calculation, it is assumed that T_C can equal $T_{C,MAX}$ when the board is plugged in. This would only occur if a hot board is unplugged, then plugged back in before it cools off. This is worst case and for many applications, the $T_{A,MAX}$ can be used for this derating.

$$I_{SOA}(7.5ms, T_{C,MAX}) = I_{SOA}(7.5ms, 25°C) \times \frac{T_{J,ABSMAX} - T_{C,MAX}}{T_{J,ABSMAX} - 25°C} = 7.32A \times \frac{175°C - 114°C}{175°C - 25°C} = 2.98A \quad (57)$$

This calculation shows that the MOSFET stays well-within its SOA during a start-up if the slew rate is 4 V/ms. Note that if the load is off during start-up, the total energy dissipated in the FET is constant regardless of the slew rate. Thus, a lower slew rate always places less stress on the FET. To ensure that the slew rate is at most 4 V/ms, the $C_{dv/dt}$ should be chosen as follows:

$$c_{dv/dt} = \frac{I_{SOURCE,MAX}}{4V/ms} = \frac{40\mu A}{4V/ms} = 10nF \quad (58)$$

Next, the typical slew rate and start time can be computed to be 2 V/ms as shown in Equation 59, making the typical start time 30 ms.

$$V_{OUT,dv/dt} = \frac{I_{SOURCE}}{c_{dv/dt}} = \frac{20\mu A}{10nF} = 2V/ms \quad (59)$$

9.2.2.2.8 Select Power Limit and Fault Timer

When picking the power limit it needs to meet two requirements:

- Power limit is large enough to avoid operating with $V_{SNS} < 4$ mV
- Power limit is large enough to ensure that the timer does not run during start up. Picking a power limit such that it is 2× of $I_{INR,MAX} \times V_{IN,MAX}$ is good practice.

Thus, the minimum allowed power limit can be computed as follows:

$$P_{LIM,MIN} = \max\left(\frac{V_{SNS,MIN} \times V_{IN,MAX}}{R_{SNS}}, 2 \times V_{IN,MAX} \times I_{INR,MAX}\right) = \max(240W, 211.2W) = 240W \quad (60)$$

Next, the power limit is set to $P_{LIM,MIN}$ using Equation 61. Here R_{SNS} and R_{PWR} are in ohms and P_{LIM} is in watts.

$$R_{PWR} = \frac{P_{LIM} \times R_{SNS} - 0.043}{7 \times 10^{-6}} = \frac{240 \times 0.001 - 0.043}{7 \times 10^{-6}} = 28143\Omega \quad (61)$$

The closest available resistor should be selected. In this case, a 28.2-kΩ resistor was chosen.

Next, a fault timer value should be selected. In general, the timer value should be decreased until there is enough margin between available SOA and the power pulse the FET experiences during a hot-short. For this design, a 10-nF C_{TIMER} was chosen corresponding to a 520 µs. The available SOA is extrapolated using the method described earlier.

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$$I_{SOA}(t) = a \times t^{m}$$

$$m = \frac{\ln\left(I_{SOA}(t_1) / I_{SOA}(t_2)\right)}{\ln(t_1 / t_2)} = \frac{\ln\left(\frac{100A}{30A}\right)}{\ln\left(\frac{0.1ms}{1ms}\right)} = -0.52$$

$$a = \frac{I_{SOA}(t_2)}{t_2^{m}} = \frac{30A}{(1ms)^{-0.52}} = 30A \times (ms)^{0.52}$$

$$I_{SOA}(0.52ms,\ 25°C) = 30A \times (ms)^{0.52} \times (0.52ms)^{-0.52} = 42.3A \quad (62)$$

Next, the available SOA is derated for temperature:

$$I_{SOA}(0.52ms, T_{C,MAX}) = 42.3A \times \frac{175°C - 114°C}{175°C - 25°C} = 17.17A \quad (63)$$

Note that only 4 A was required, while the FET can support 17.17 A. This confirms that the design is robust and has plenty of margin.

9.2.2.2.9 Chose Input and Output Protection and Set Undervoltage, Overvoltage, and Power Good Thresholds

This is identical to the previous design. Refer to *Set UVLO and OVLO Thresholds*, *Power Good Pin*, and *Input and Output Protection* for these settings.

9.2.2.2.10 Final Schematic and Component Values

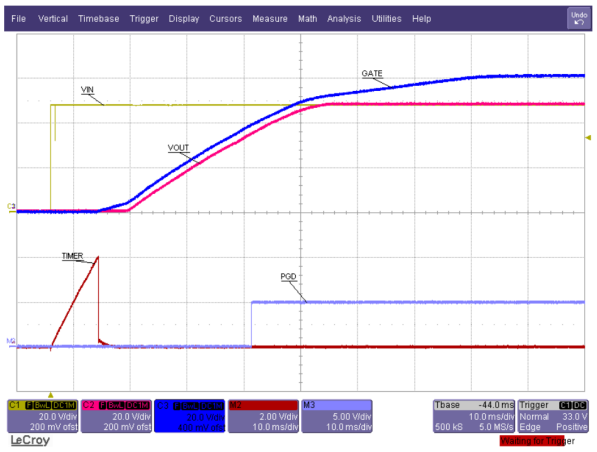
Figure 40 shows the schematic used to implement the requirements described in the *48-V, 20-A PMBus Hotswap Design* section. In addition, Table 54 provides the final component values used to meet the design requirements for a 48-V, 20-A hotswap design. The application curves in the next section are based on these components.

Table 54. Final Component Values (48-V, 20-A Design)

Component	Value
R_{SNS}	1 mΩ
R1	150 kΩ
R2	11.5 kΩ
R3	95.3 kΩ
R4	3.74 kΩ
R5	150 kΩ
R6	10.5 kΩ
R_{PWR}	28.2 kΩ
Q1	2x (PSMN4R8-100BSEJ)
Q2	MMBT3904
D1	B380-13-F
Z1	5.0SMDJ60A
C_{TIMER}	10 nF
Optional dv/dt circuit	Yes
D2	1N4148W-7-F
Q3	MMBT5401LT1G
C_{dvdt}	10 nF

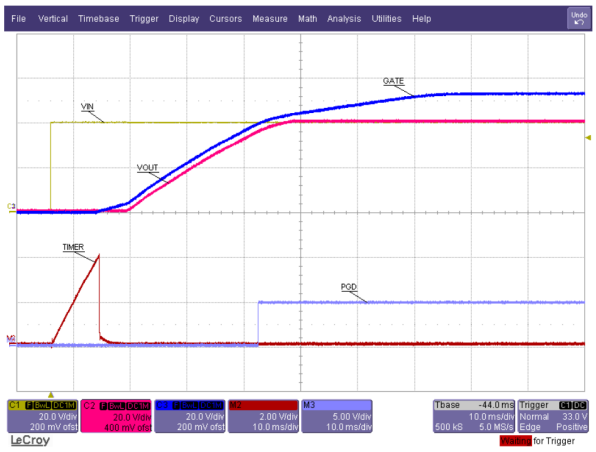
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9.2.2.3 Application Curves



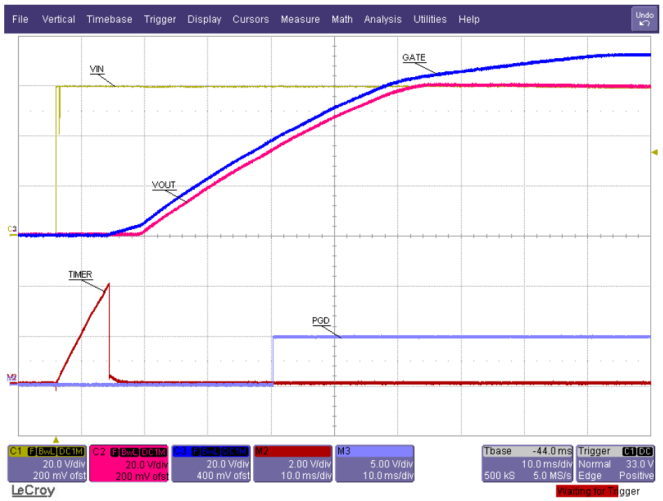
V_{IN} = 48 V

Figure 41. Start-Up



V_{IN} = 40 V

Figure 42. Start-Up



V_{IN} = 60 V

Figure 43. Start-Up



Figure 44. Start-Up into Short

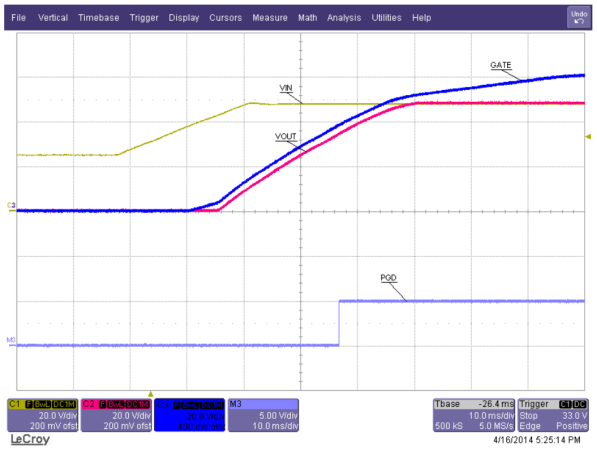


Figure 45. Under-Voltage

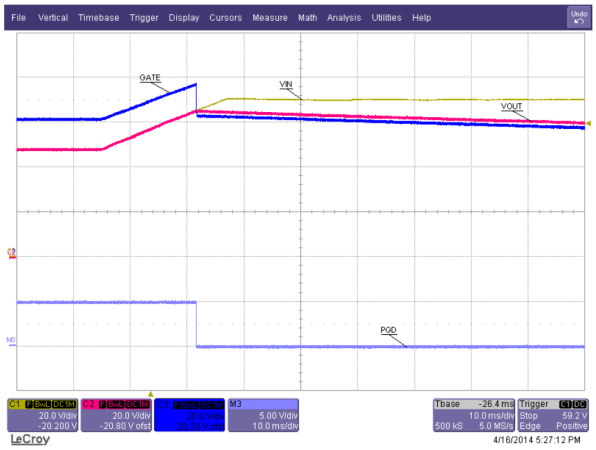


Figure 46. Over-Voltage

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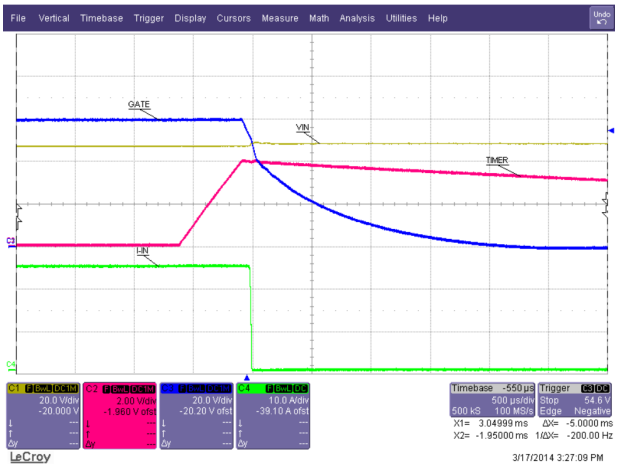


Figure 47. Gradual Overcurrent

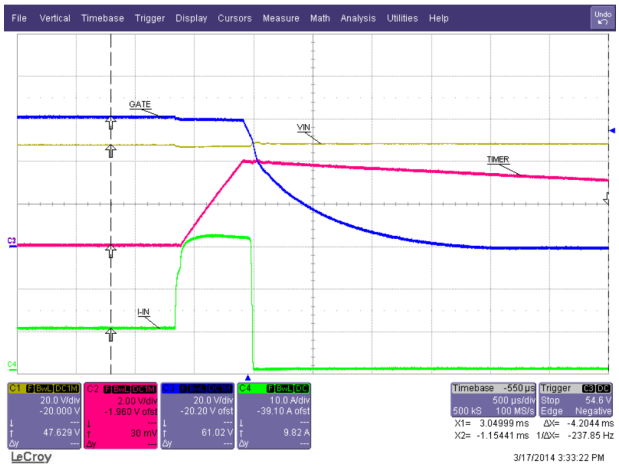


Figure 48. Loadstep



Figure 49. Hot Short on Vout (Zoomed Out)

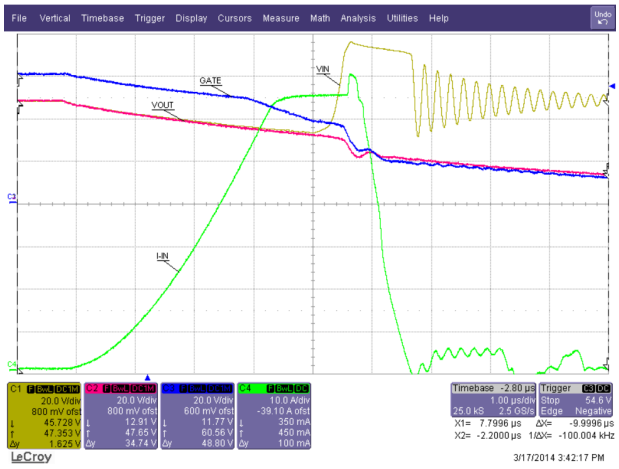


Figure 50. Hot Short on Vout (Zoomed In)

10 Power Supply Recommendations

In general, the LM5066I behavior is more reliable if it is supplied from a very regulated power supply. However, high-frequency transients on a backplane are not uncommon due to adjacent card insertions or faults. If this is expected in the end system, TI recommends to place a 1-µF ceramic capacitor to ground close to the source of the hotswap MOSFET. This reduces the common mode seen by VIN_K and SENSE. Additional filtering may be necessary to avoid nuisance trips.

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11 Layout

11.1 Layout Guidelines

The following guidelines should be followed when designing the PC board for the LM5066I:

1. Place the LM5066I close to the board's input connector to minimize trace inductance from the connector to the MOSFET.
2. Place a TVS, Z_1, directly adjacent to the VIN and GND pins of the LM5066I to help minimize voltage transients which may occur on the input supply line. The TVS should be chosen such that the peak V_{IN} is just lower the TVS reverse-bias voltage. Transients of 20 V or greater over the nominal input voltage can easily occur when the load current is shut off. A small capacitor may be sufficient for low current sense applications (I < 2 A). TI recommends to test the VIN input voltage transient performance of the circuit by current limiting or shorting the load and measuring the peak input voltage transient.
3. Place a 1-µF ceramic capacitor as close as possible to VREF pin.
4. Place a 1-µF ceramic capacitor as close as possible to VDD pin.
5. The sense resistor (R_{SNS}) should be placed close to the LM5066I. A trace should connect the VIN pad and Q_1 pad of the sense resistor to VIN_K and SENSE pins, respectively. Connect R_{SNS} using the Kelvin techniques as shown in Figure 52.
6. The high current path from the board's input to the load (through Q_1), and the return path, should be parallel and close to each other to minimize loop inductance.
7. The AGND and GND connections should be connected at the pins of the device. The ground connections for the various components around the LM5066I should be connected directly to each other, and to the LM5066I's GND and AGND pin connection, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.
8. Provide adequate thermal sinking for the series pass device (Q_1) to help reduce stresses during turn-on and turn-off.
9. The board's edge connector can be designed such that the LM5066I detects through the UVLO/EN pin that the board is being removed, and responds by turning off the load before the supply voltage is disconnected. For example, in Figure 51, the voltage at the UVLO/EN pin goes to ground before V_{IN} is removed from the LM5066I as a result of the shorter edge connector pin. When the board is inserted into the edge connector, the system voltage is applied to the LM5066I's VIN pin before the UVLO voltage is taken high, thereby allowing the LM5066I to turn on the output in a controlled fashion.

11.2 Layout Example

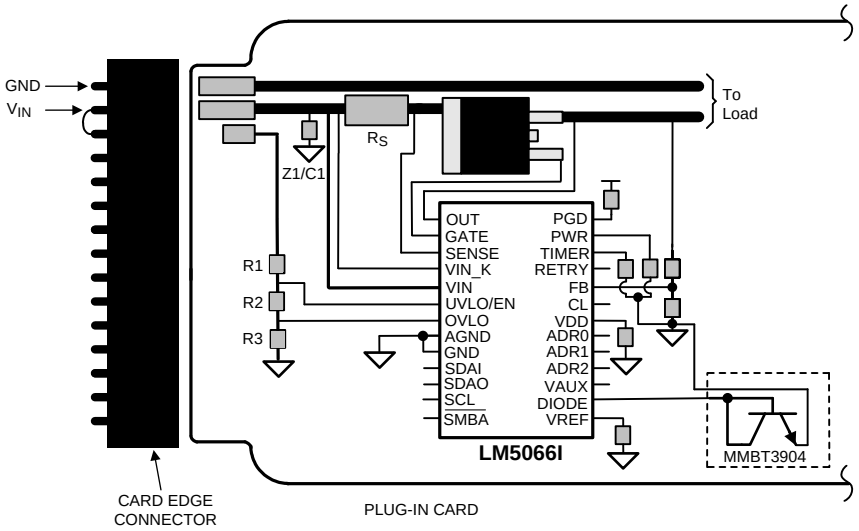


Figure 51. Recommended Board Connector Design

Layout Example (continued)

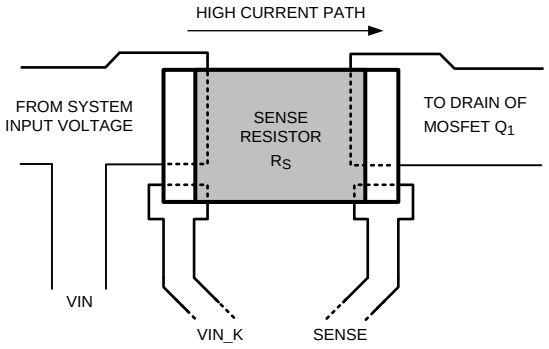


Figure 52. Sense Resistor Connections

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12 Device and Documentation Support

12.1 Trademarks

PMBus is a trademark of SMIF, Inc.

12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5066IPMHE/NOPB	ACTIVE	HTSSOP	PWP	28	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	LM5066I	Samples
LM5066IPMHX/NOPB	ACTIVE	HTSSOP	PWP	28	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	LM5066I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

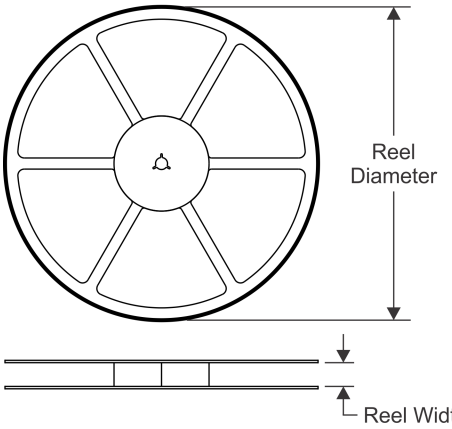
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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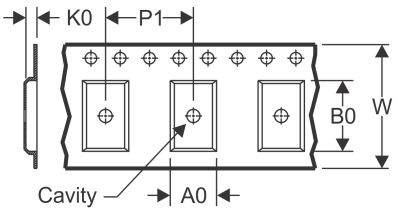
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

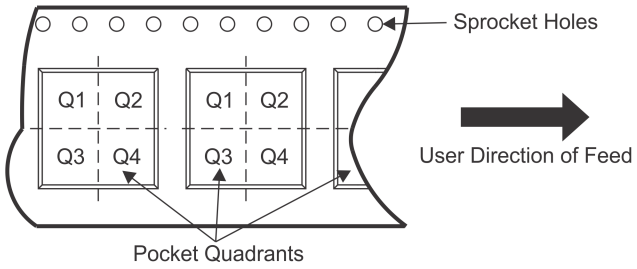


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

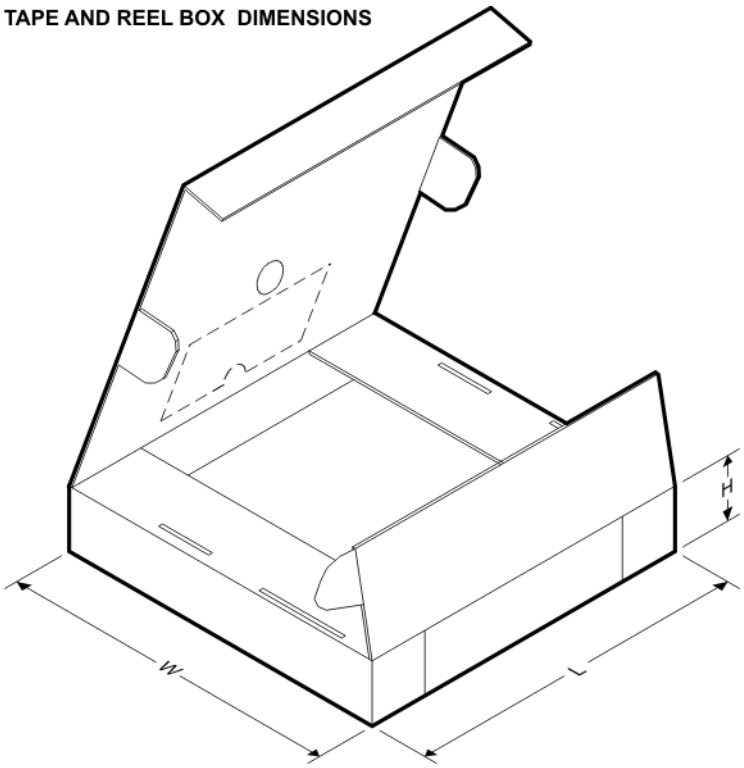
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5066IPMHE/NOPB	HTSSOP	PWP	28	250	178.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1
LM5066IPMHX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5066IPMHE/NOPB	HTSSOP	PWP	28	250	210.0	185.0	35.0
LM5066IPMHX/NOPB	HTSSOP	PWP	28	2500	367.0	367.0	38.0

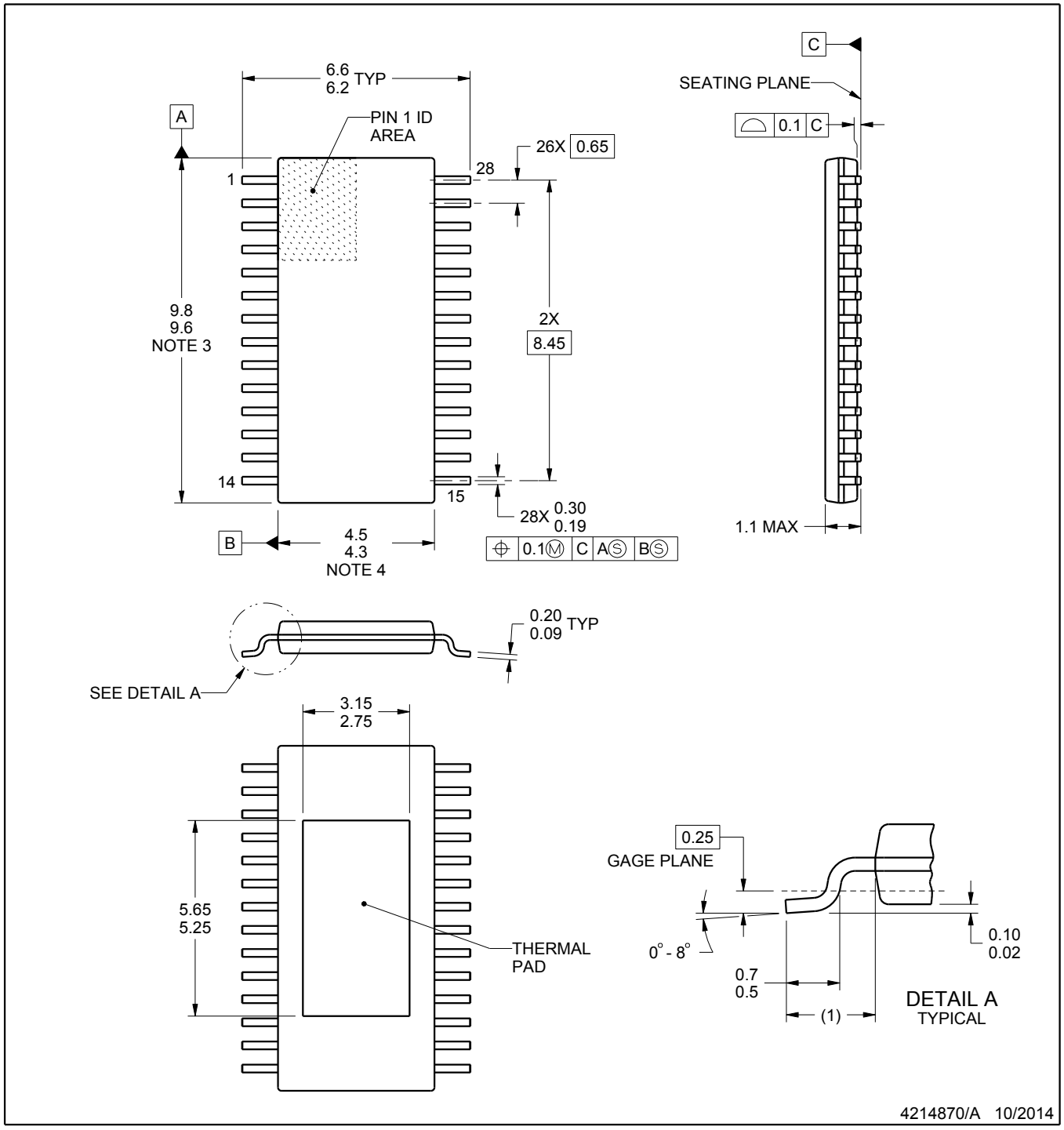


PACKAGE OUTLINE

PWP0028A

PowerPAD™ - 1.1 mm max height

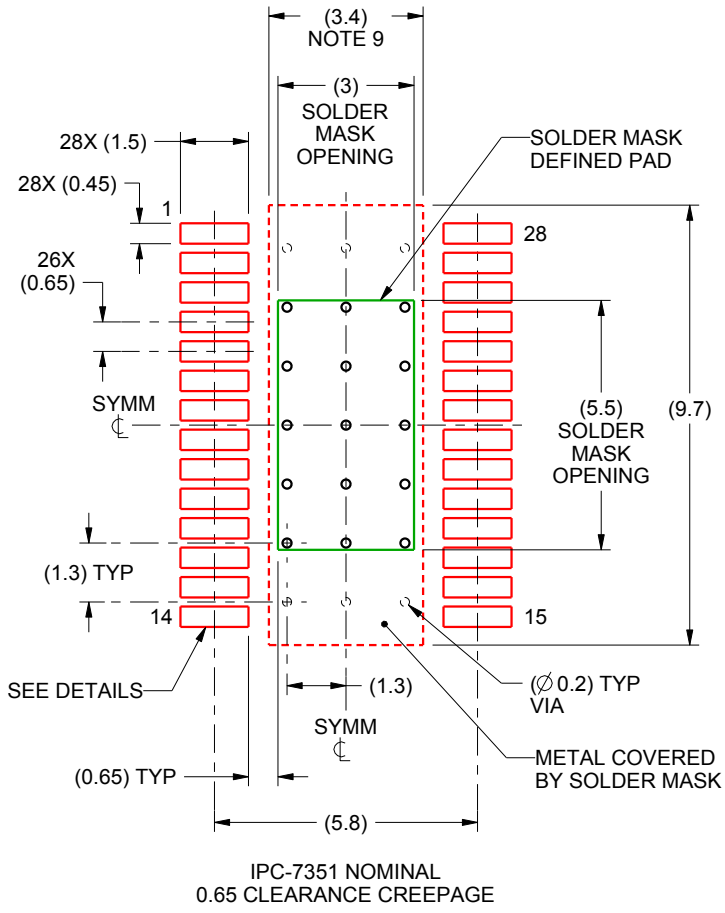
PLASTIC SMALL OUTLINE



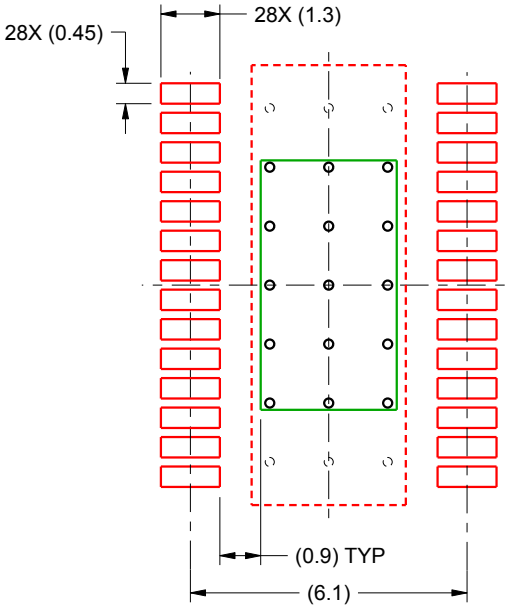
NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-153, variation AET.

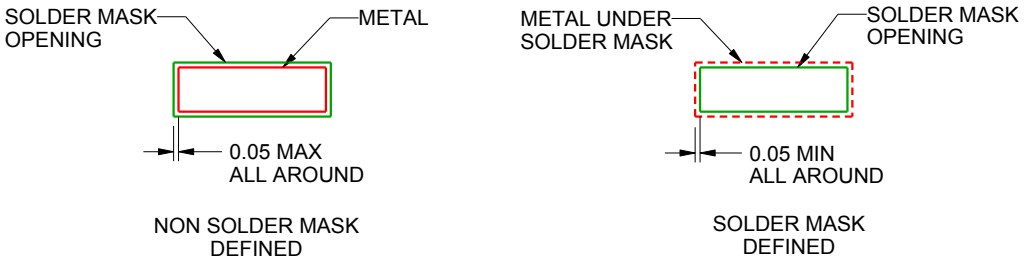


IPC-7351 NOMINAL
0.65 CLEARANCE CREEPAGE



HV / ISOLATION OPTION
0.9 CLEARANCE CREEPAGE
OTHER DIMENSIONS IDENTICAL TO IPC-7351

LAND PATTERN EXAMPLE
SCALE:6X

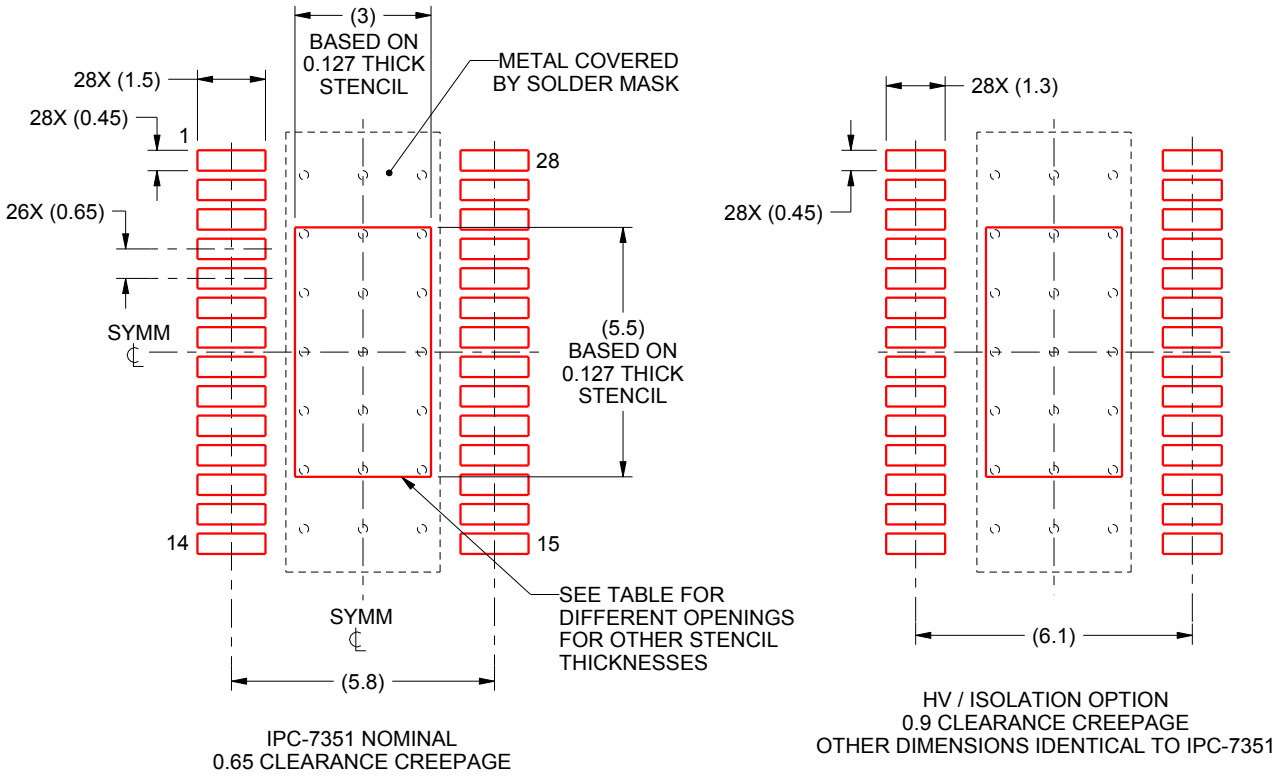


SOLDER MASK DETAILS

4214870/A 10/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.55 X 6.37
0.127	3.0 X 5.5 (SHOWN)
0.152	2.88 X 5.16
0.178	2.66 X 4.77

4214870/A 10/2014

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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