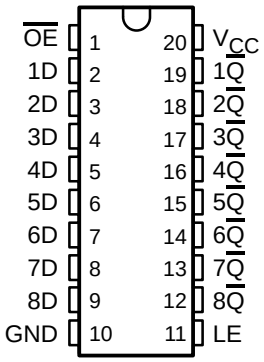
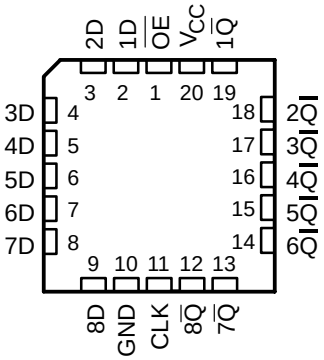
- **4.5-V to 5.5-V $V_{CC}$ Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Max $t_{pd}$ of 8.5 ns at 5 V**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Inverted Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture to Optimize PCB Layout**

**SN54ACT563 . . . J OR W PACKAGE**
**SN74ACT563 . . . DB, DW, N, NS, OR PW PACKAGE**
**(TOP VIEW)**




**SN54ACT563 . . . FK PACKAGE**
**(TOP VIEW)**




## description/ordering information

The 'ACT563 devices are octal D-type transparent latches with 3-state outputs. When the latch-enable (LE) input is high, the $\overline{Q}$ outputs are set to the complements of the data (D) inputs. When LE is taken low, the $\overline{Q}$ outputs are latched at the inverse logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high logic level provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | PDIP – N | Tube | SN74ACT563N | SN74ACT563N |
| | SOIC – DW | Tube | SN74ACT563DW | ACT563 |
| | | Tape and reel | SN74ACT563DWR | |
| | SOP – NS | Tape and reel | SN74ACT563NSR | ACT563 |
| | SSOP – DB | Tape and reel | SN74ACT563DBR | AD563 |
| | TSSOP – PW | Tape and reel | SN74ACT563PWR | AD563 |
| –55°C to 125°C | CDIP – J | Tube | SNJ54ACT5634J | SNJ54ACT563J |
| | CFP – W | Tube | SNJ54ACT563W | SNJ54ACT563W |
| | LCCC – FK | Tube | SNJ54ACT563FK | SNJ54ACT563FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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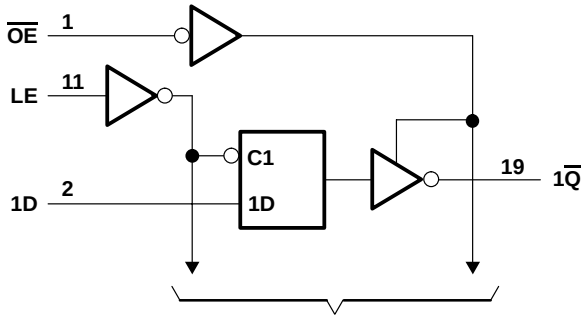
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**FUNCTION TABLE**
**(each latch)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | $\overline{Q}$ |
| L | H | H | L |
| L | H | L | H |
| L | L | X | $\overline{Q}_0$ |
| H | X | X | Z |

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND . . . . . ±200 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package . . . . . 70°C/W
DW package . . . . . 58°C/W
N package . . . . . 69°C/W
NS package . . . . . 60°C/W
PW package . . . . . 83°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

| | | SN54ACT563 | | SN74ACT563 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –24 | | –24 | mA |
| $I_{OL}$ | Low-level output current | | 24 | | 24 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 8 | | 8 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54ACT563 | | SN74ACT563 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.49 | | 4.4 | | 4.4 | | V |
| | | 5.5 V | 5.4 | 5.49 | | 5.4 | | 5.4 | | |
| | $I_{OH}$ = –24 mA | 4.5 V | 3.86 | | | 3.7 | | 3.76 | | |
| | | 5.5 V | 4.86 | | | 4.7 | | 4.76 | | |
| | $I_{OH}$ = –50 mA† | 5.5 V | | | | 3.85 | | | | |
| | $I_{OH}$ = –75 mA† | 5.5 V | | | | | | 3.85 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | V |
| | | 5.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 24 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | 5.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 50 mA† | 5.5 V | | | | | 1.65 | | | |
| | $I_{OL}$ = 75 mA† | 5.5 V | | | | | | | 1.65 | |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±5 | | ±2.5 | μA |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 80 | | 40 | μA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at GND or $V_{CC}$ | 5.5 V | | 0.6 | | | 1.6 | | 1.5 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 4.5 | | | | | | pF |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or $V_{CC}$.

## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | $T_A$ = 25°C | | SN54ACT563 | | SN74ACT563 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 3 | | 5 | | 3 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 4 | | 4.5 | | 4.5 | | ns |
| $t_h$ | Hold time, data after LE↓ | 0 | | 1.5 | | 0 | | ns |

PRODUCT PREVIEW

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**switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | SN54ACT563 | | SN74ACT563 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | D | $\overline{Q}$ | 3 | 7 | 11.5 | 1 | 14.5 | 2.5 | 12.5 | ns |
| $t_{PHL}$ | | | 3 | 6 | 10 | 1 | 12 | 2.5 | 11 | |
| $t_{PLH}$ | LE | $\overline{Q}$ | 3 | 6.5 | 10.5 | 1 | 12.5 | 2.5 | 11.5 | ns |
| $t_{PHL}$ | | | 2.5 | 5.5 | 9.5 | 1 | 11.5 | 2 | 10.5 | |
| $t_{PZH}$ | $\overline{OE}$ | $\overline{Q}$ | 2.5 | 5.5 | 9 | 1 | 11.5 | 2 | 10 | ns |
| $t_{PZL}$ | | | 2 | 5.5 | 8.5 | 1 | 11 | 2 | 9.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | $\overline{Q}$ | 3.5 | 6.5 | 10.5 | 1 | 12 | 2.5 | 11.5 | ns |
| $t_{PLZ}$ | | | 2 | 4.5 | 8 | 1 | 9.5 | 1 | 8.5 | |

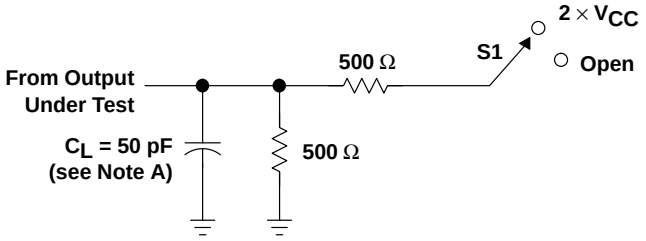
PRODUCT PREVIEW

**operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C**

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF, f = 1 MHz | 50 | pF |

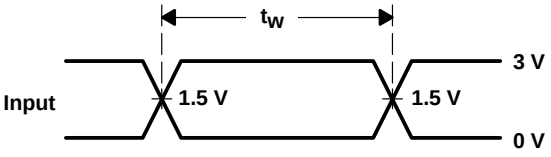
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## PARAMETER MEASUREMENT INFORMATION

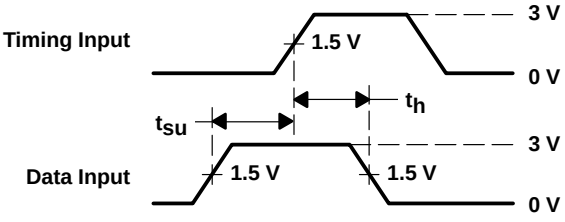



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | Open |

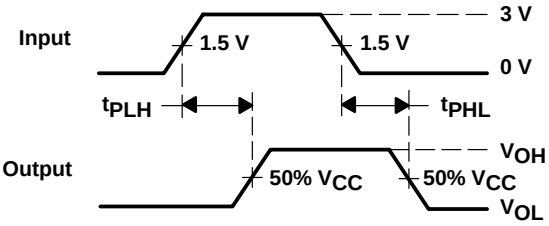
LOAD CIRCUIT



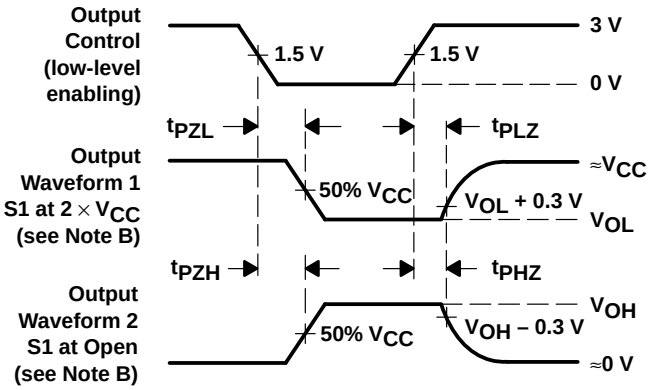

VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ACT563DW | LIFEBUY | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT563 | |
| SN74ACT563DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT563 | Samples |
| SN74ACT563N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Non-Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74ACT563N | Samples |
| SN74ACT563PW | LIFEBUY | TSSOP | PW | 20 | 70 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AD563 | |
| SN74ACT563PWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AD563 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

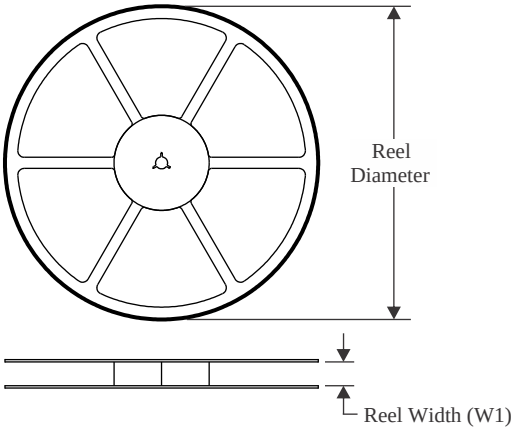
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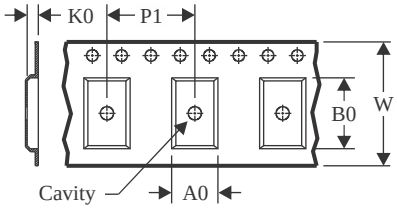
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**REEL DIMENSIONS**

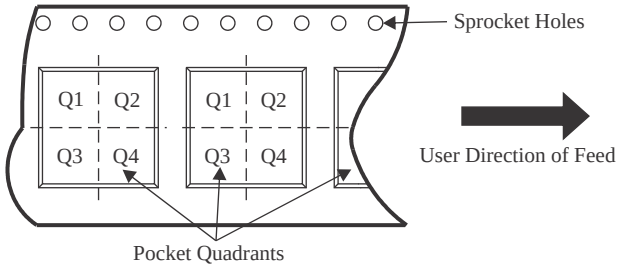



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

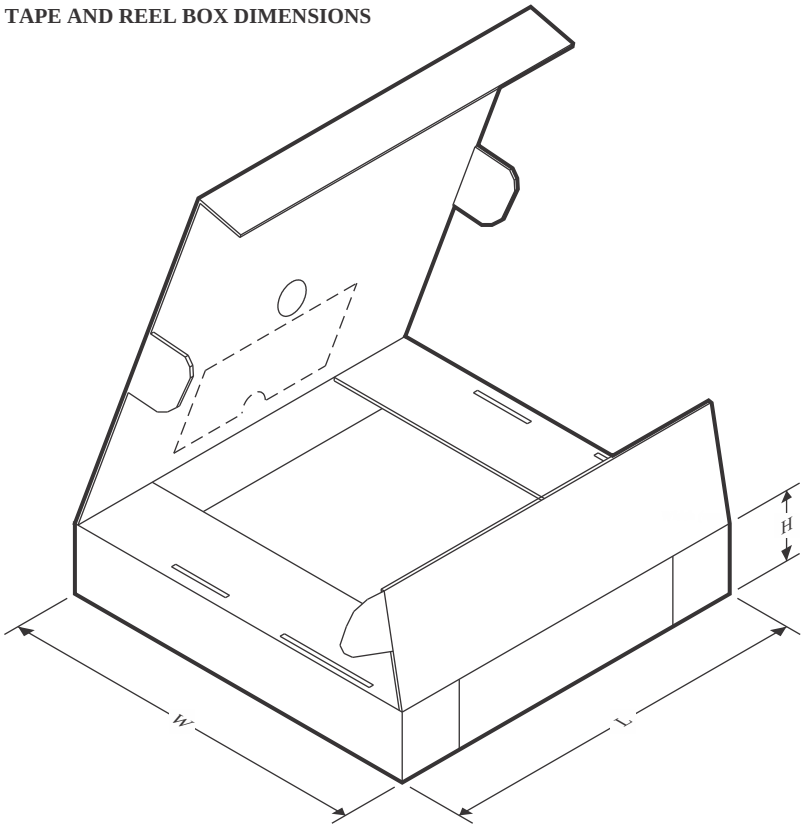
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ACT563DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74ACT563PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

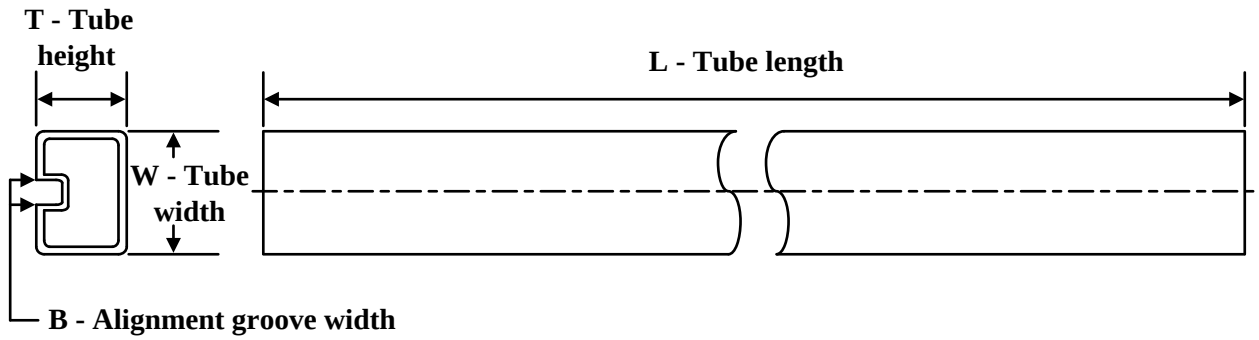
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74ACT563DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74ACT563PWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74ACT563DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74ACT563N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74ACT563PW | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |

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