

钍地半导体
Tudi Semiconductor

Product Specification

TUDI-MAX14840EASA

40Mbps, +3.3V, RS-485 Half-Duplex Transceivers

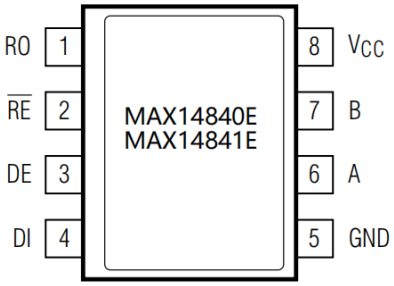
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semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Benefits and Features



MAX14840E
MAX14841E

- High ESD Protection Provides Increases Equipment Uptime
- ±35kV Human Body Model (HBM) per JEDEC JS-001-2012
- ±20kV Air Gap Discharge per IEC 61000-4-2
- ±12kV Contact Discharge per IEC 61000-4-2
- Integrated Features Increases Robustness
- Large 170mV Receiver Hysteresis (MAX14840) for High Receiver Noise Tolerance
- True Fail Safe Receiver Input (MAX14841E) Keeps Receiver Output Logic-High Upon Shorts and Open On Receiver Input
- Thermal Self-Protection Shutdown at 160 ° C Junction Temperature
- High Industrial -40 ° C to +125 ° C Ambient Operating Temperature Range/-40 ° C to +150 ° C Junction Temperature Range
- Hot Swap Capability Eliminates False Transition During Power-Up or Hot Insertion
- Low Current Reduces Power Requirements
- 10μA (max) Shutdown Current
- 1.5mA (typ) Supply Current
- 3.3V Supply Voltage
- Available in Industry Standard 8-Pin SO Packages

Applications

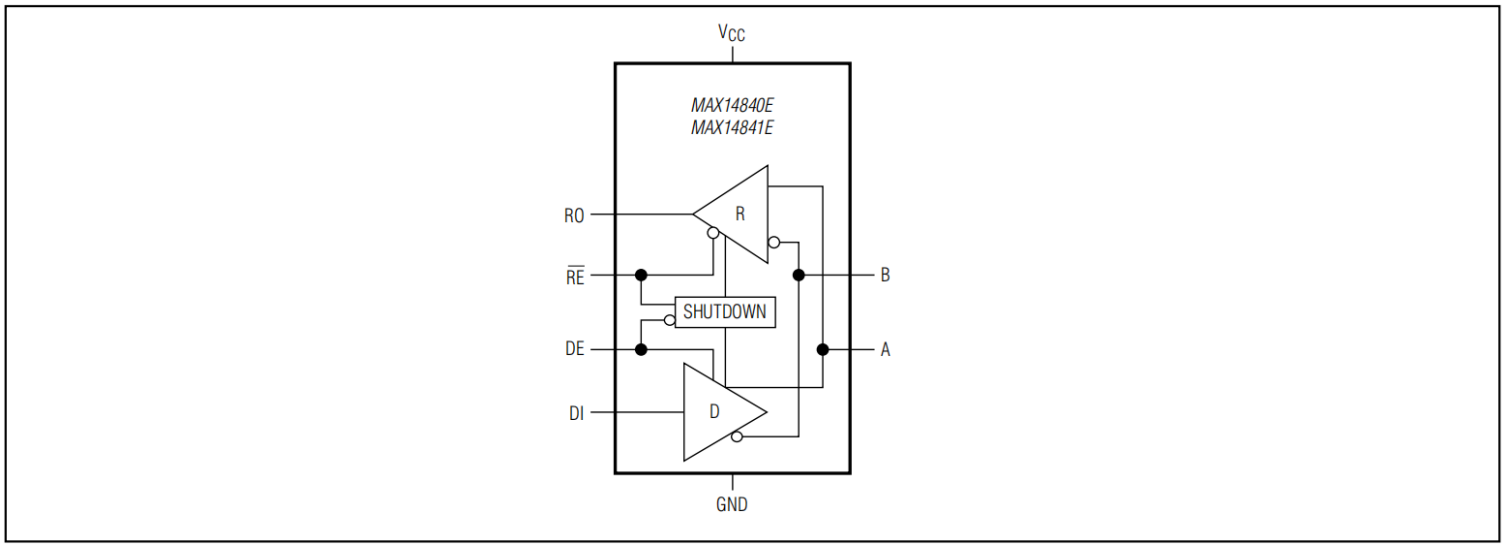
- Motion Controllers
- Fieldbus Networks
- Industrial Control Systems
- Backplane Buses
- HVAC Networks

General Description

The MAX14840E/MAX14841E are +3.3V ESD-protected transceivers intended for half-duplex RS-485 communica-tion up to 40Mbps. These transceivers are optimized for high speeds over extended cable runs while maximizing tolerance to noise.

The MAX14840E features symmetrical fail-safe and larg-er receiver hysteresis, providing improved noise rejection and improved recovered signals in high-speed and long cable applications. The MAX14841E has true fail-safe
receiver inputs guaranteeing a logic-high receiver output when inputs are shorted or open. The MAX14840E/MAX14841E are available in 8-pin SO and small, 8-pin (3mm x 3mm) TDFN-EP packages. Both devices operate over the -40NC to +125NC temperature
range

Functional Diagram



Absolute Maximum Ratings

(Voltages referenced to GND.)
V_{CC} ..... -0.3V to +6.0V
$\overline{RE}$, RO ..... -0.3V to +(V_{CC} + 0.3V)
DE, DI ..... -0.3V to +6.0V
A, B..... -8.0V to +13.0V
Short-Circuit Duration (RO, A, B) to GND ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 7.6mW/°C above +70°C) 606mW
8-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1)
8-Pin SO.....38°C/W
8-Pin TDFN .....8°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
8-Pin SO .....132°C/W
8-Pin TDFN .....41°C/W
Operating Temperature Range (Note 2) ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.
Note 2: Operation is specified with junction temperatures up to +150°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage	V_{CC}			3.0		3.6	V
Supply Current	I_{CC}	DE = $\overline{RE}$ = V_{CC}, or DE = $\overline{RE}$ = GND, or DE = V_{CC}, $\overline{RE}$ = GND, DI = V_{CC} or GND, no load			1.5	4	mA
Shutdown Supply Current	I_{SH}	DE = GND and $\overline{RE}$ = V_{CC}				10	µA
DRIVER							
Differential Driver Output	V_{OD}	R_L = 54Ω, Figure 1		1.5			V
Change in Magnitude of Differential Output Voltage	ΔV_{OD}	R_L = 54Ω, Figure 1 (Note 5)		-0.2	0	+0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R_L = 54Ω, Figure 1			V_{CC}/2	3	V
Change in Common-Mode Voltage	ΔV_{OC}	R_L = 54Ω, Figure 1 (Note 5)		-0.2		0.2	V
Single-Ended Driver Output High	V_{OH}	A/B output, I_{OUT} = -20mA		2.2			V
Single-Ended Driver Output Low	V_{OL}	A/B output, I_{OUT} = 20mA				0.8	V
Driver Short-Circuit Output Current	$\lvert I_{OSD} \rvert$	0V ≤ V_{OUT} ≤ +12V, output low				250	mA
		-7V ≤ V_{OUT} ≤ V_{CC}, output high		250			
RECEIVER							
Input Current (A and B)	$I_{A,B}$	DE = GND, V_{CC} = GND or +3.6V	V_{IN} = +12V			1000	µA
			V_{IN} = -7V	-800			
Differential Input Capacitance	$C_{A,B}$	Between A and B, DE = GND, f = 2MHz			12		pF

DC Electrical Characteristics (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Receiver Differential Threshold Voltage (MAX14840E Only)	V_{THF}	-7V ≤ V_{CM} ≤ 12V, V_{OD} falling	-200		-10	mV
	V_{THR}	-7V ≤ V_{CM} ≤ 12V, V_{OD} rising	10		200	mV
Receiver Input Hysteresis (MAX14840E Only)		V_{CM} = 0V	20	170		mV
Receiver Differential Threshold Voltage (MAX14841E Only)	V_{TH}	-7V ≤ V_{CM} ≤ 12V	-200	-105	-10	mV
Receiver Input Hysteresis (MAX14841E Only)	ΔV_{TH}	V_{CM} = 0V		10		mV
LOGIC INTERFACE						
Input High Voltage	V_{IH}	DE, DI	2.0		5.5	V
		$\overline{RE}$	2.0			
Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$			0.8	V
Input Hysteresis	V_{HYS}	DE, DI, $\overline{RE}$		50		mV
Input Current	I_{IN}	DE, DI, $\overline{RE}$	-1		+1	µA
Input Impedance on First Transition		DE, $\overline{RE}$	1		10	kΩ
Output High Voltage	V_{OH}	$\overline{RE}$ = GND, I_O = -1mA, V_A - V_B > 200mV	V_{CC} - 1.5			V
Output Low Voltage	V_{OL}	$\overline{RE}$ = GND, I_O = 1mA, V_A - V_B < -200mV			0.4	V
Three-State Output Current at Receiver	I_{OZR}	$\overline{RE}$ = V_{CC}, 0V ≤ V_O ≤ V_{CC}	-1		+1	µA
Receiver Output Short-Circuit Current	I_{OSR}	0V ≤ V_{RO} ≤ V_{CC}	-95		+95	mA
PROTECTION						
Thermal-Shutdown Threshold	T_{TS}			160		°C
Thermal-Shutdown Hysteresis	T_{TSH}			15		°C
ESD Protection: A, B to GND		IEC 61000-4-2 Air Gap Discharge		±20		kV
		IEC 61000-4-2 Contact Discharge		±12		
		HBM		±35		
ESD Protection: All Other Pins		HBM		±2		kV

Switching Characteristics

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER						
Propagation Delay	t_{DPLH}	R_L = 54Ω, C_L = 50pF, Figures 2 and 3 (Note 6)	5	12	20	ns
	t_{DPHL}		5	12	20	
Differential Driver Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	R_L = 54Ω, C_L = 50pF, Figures 2 and 3 (Notes 6, 9)			2	ns

Switching Characteristics (continued)

(VCC = +3.0V to +3.6V, TA = -40°C to +125°C, unless otherwise noted. Typical values are at VCC = +3.3V and TA = +25°C.) (Notes 3, 4)

Driver Differential Output Rise or Fall Time	t_{HL}, t_{LH}	R_L = 54Ω, C_L = 50pF, Figures 2 and 3 (Notes 6, 9)			7.5	ns
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Maximum Data Rate	DR_{MAX}		40			Mbps
Driver Enable to Output High	t_{DZH}	R_L = 110Ω, C_L = 50pF, Figures 4 and 5 (Notes 6, 7)			30	ns
Driver Enable to Output Low	t_{DZL}	R_L = 110Ω, C_L = 50pF, Figures 4 and 5 (Notes 6, 7)			30	ns
Driver Disable Time from Low	t_{DLZ}	R_L = 110Ω, C_L = 50pF, Figures 4 and 5 (Notes 6, 7)			30	ns
Driver Disable Time from High	t_{DHZ}	R_L = 110Ω, C_L = 50pF, Figures 4 and 5 (Notes 5, 6)			30	ns
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	R_L = 110Ω, C_L = 50pF, Figures 4 and 5 (Notes 6, 7)			4	µs
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	R_L = 110Ω, C_L = 50pF, Figures 4 and 5 (Notes 6, 7)			4	µs
Time to Shutdown	t_{SHDN}	(Note 8)	50		800	ns
RECEIVER						
Propagation Delay	t_{RPLH}	C_L = 15pF, Figures 6 and 7 (Note 6)			25	ns
	t_{RPHL}				25	
Receiver Output Skew	t_{RSKEW}	C_L = 15pF, Figures 6 and 7 (Notes 6, 9)			2	ns
Maximum Data Rate	DR_{MAX}		40			Mbps
Receiver Enable to Output High	t_{RZH}	R_L = 1kΩ, C_L = 15pF, Figure 8 (Notes 6, 7)			20	ns
Receiver Enable to Output Low	t_{RZL}	R_L = 1kΩ, C_L = 15pF, Figure 8 (Notes 6, 7)			20	ns
Receiver Disable Time from Low	t_{RLZ}	R_L = 1kΩ, C_L = 15pF, Figure 8 (Notes 6, 7)			20	ns
Receiver Disable Time from High	t_{RHZ}	R_L = 1kΩ, C_L = 15pF, Figure 8 (Notes 6, 7)			20	ns
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, Figure 8 (Notes 6, 7)			4	µs
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, Figure 8 (Notes 6, 7)			4	µs
Time to Shutdown	t_{SHDN}	(Note 8)	50		800	ns

Note 3: All devices are 100% production tested at T_A = +25°C. Specifications for all temperature limits are guaranteed by design.
Note 4: All currents into the device are positive; all currents out of the device are negative. All voltages are referenced to device ground, unless otherwise noted.
Note 5: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.
Note 6: Capacitive load includes test probe and fixture capacitance.
Note 7: The timing parameter refers to the driver or receiver enable delay when the device has exited the initial hot-swap protect state and is in normal operating mode.
Note 8: Shutdown is enabled by driving $\overline{RE}$ high and DE low. The device is guaranteed to have entered shutdown after t_{SHDN} has elapsed.
Note 9: Parameter is guaranteed by characterization and not production tested.

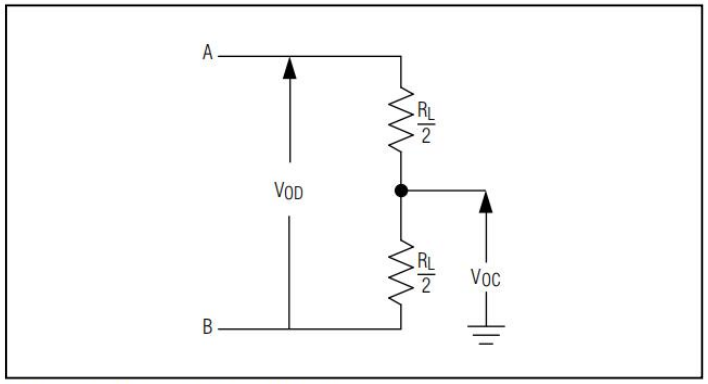


Figure 1. Driver DC Test Load

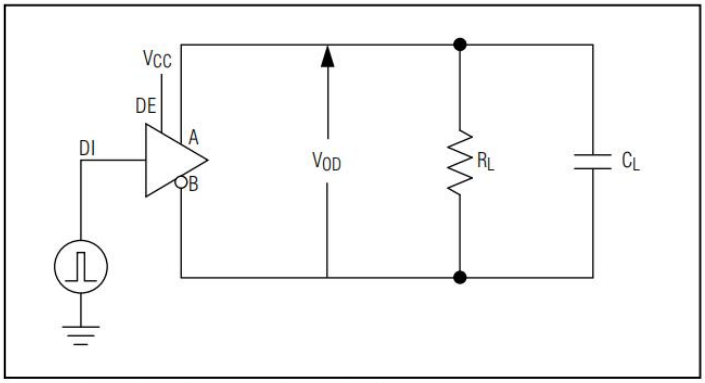


Figure 2. Driver Timing Test Circuit

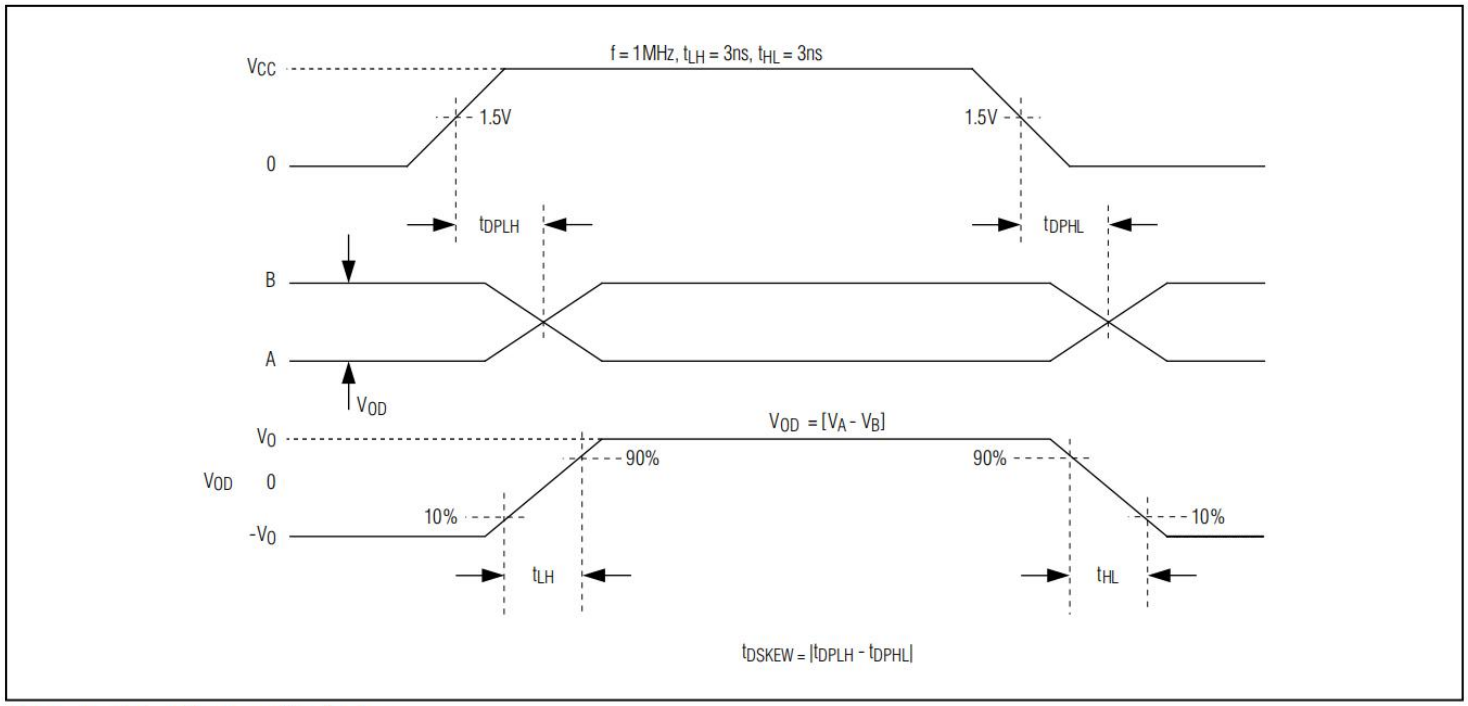


Figure 3. Driver Propagation Delays

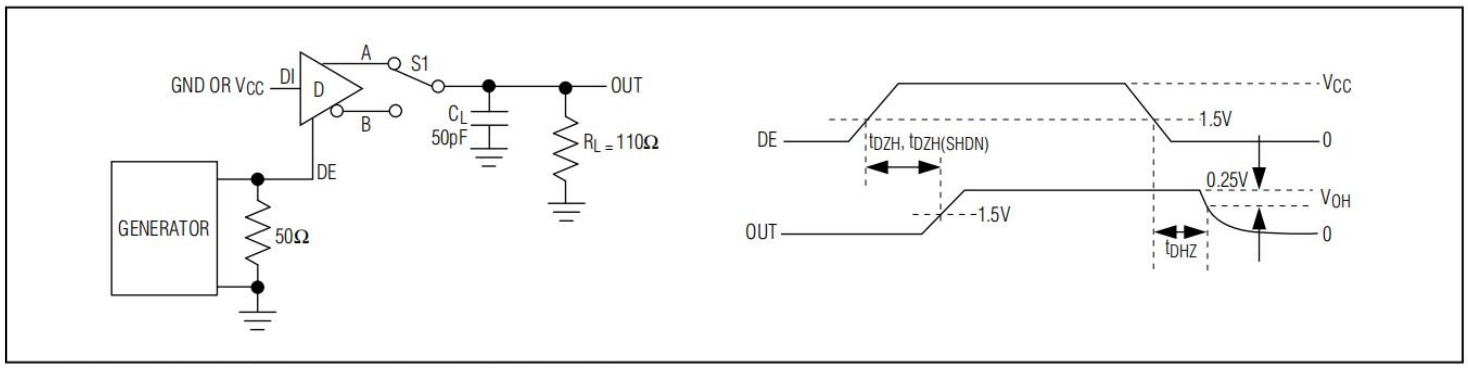


Figure 4. Driver Enable and Disable Times (t_{DZH}, t_{DHZ})

Test and Timing Diagrams (continued)

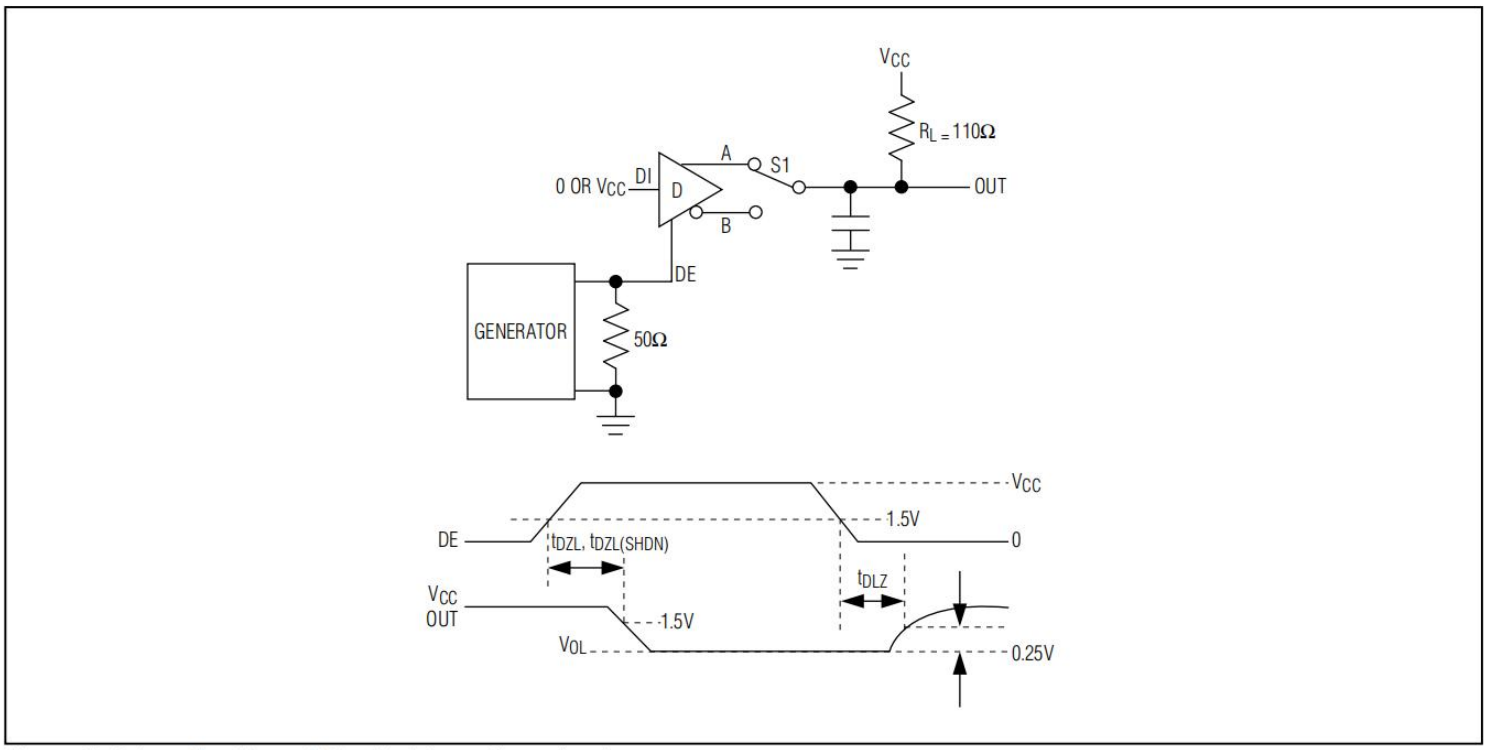


Figure 5. Driver Enable and Disable Times (t_{DLZ}, t_{DZL})

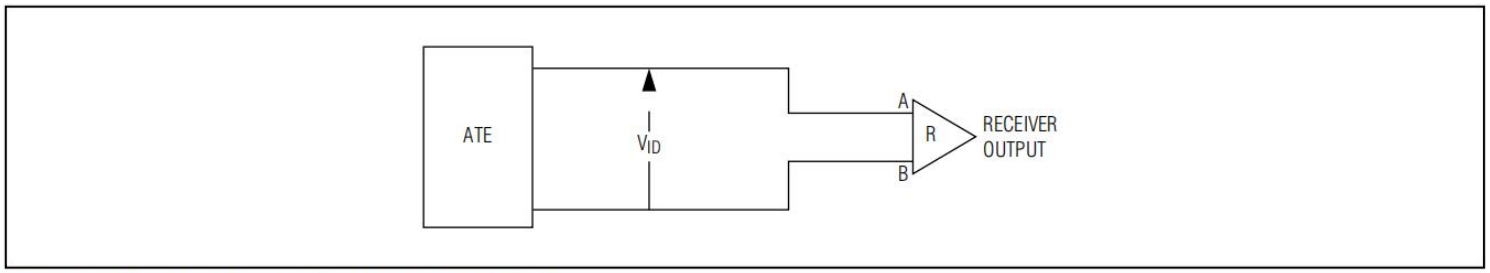


Figure 6. Receiver Propagation Delay Test Circuit

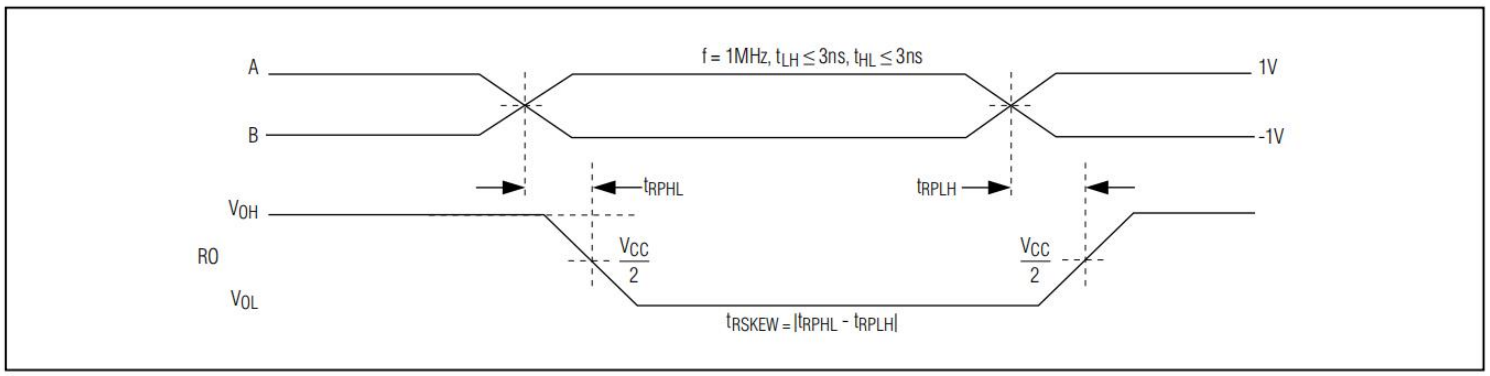


Figure 7. Receiver Propagation Delays

Test and Timing Diagrams (continued)

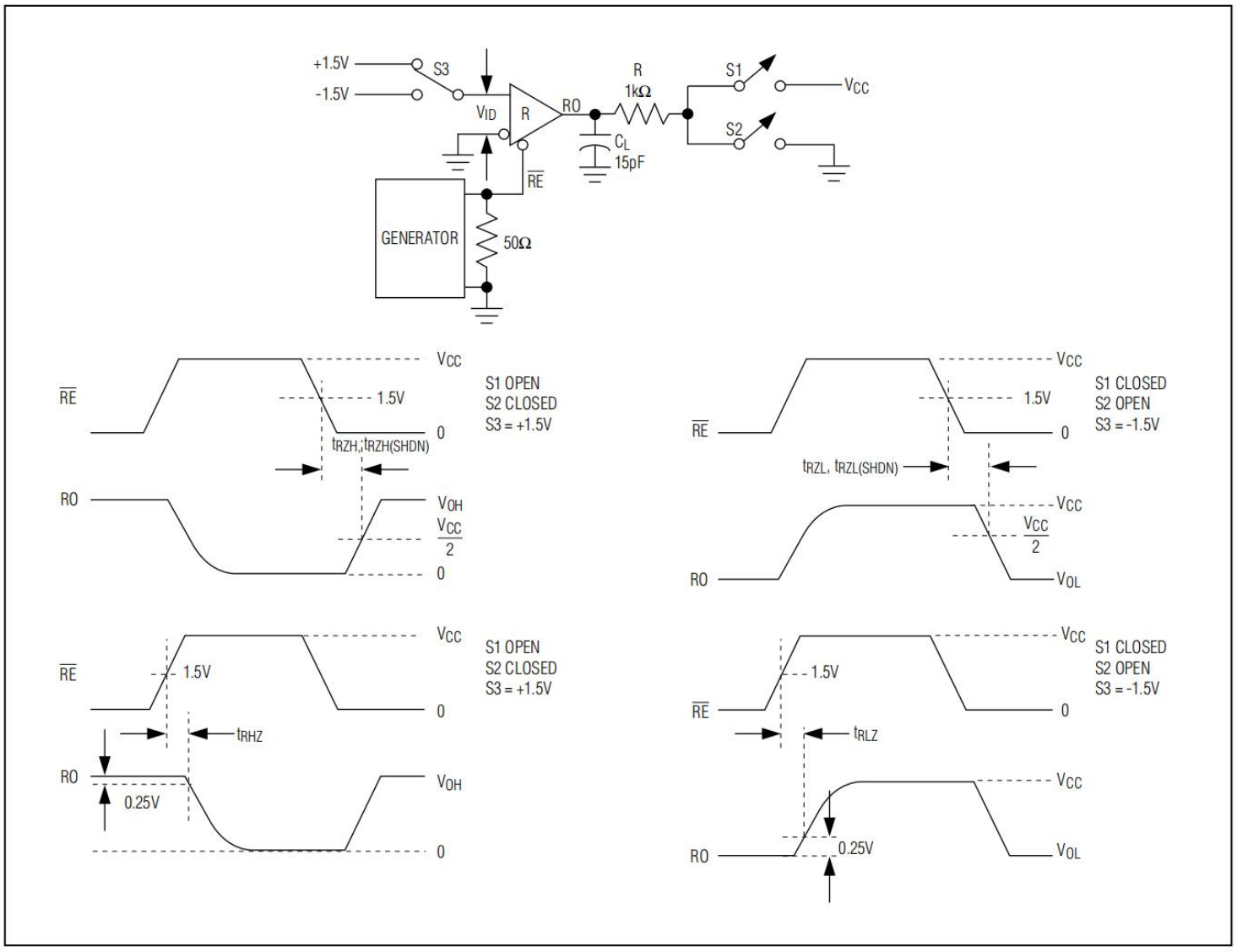


Figure 8. Receiver Enable and Disable Times

Pin Descriptions

PIN	NAME	FUNCTION
1	RO	Receiver Output. See the *Function Table*.
2	$\overline{RE}$	Active-Low Receiver-Output Enable. Drive $\overline{RE}$ low to enable RO. RO is high impedance when $\overline{RE}$ is high. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode. $\overline{RE}$ is a hot-swap input (see the *Hot-Swap Capability* section for details).
3	DE	Driver-Output Enable. Drive DE high to enable driver outputs. These outputs are high impedance when DE is low. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode. DE is a hot-swap input (see the *Hot-Swap Capability* section for details).
4	DI	Driver Input. With DE high, a low on DI forces the A output low and the B output high. Similarly, a high on DI forces the A output high and the B output low.
5	GND	Ground
6	A	Noninverting Receiver Input and Noninverting Driver Output
7	B	Inverting Receiver Input and Inverting Driver Output
8	V_{CC}	Positive Supply Voltage Input. Bypass V_{CC} with a 0.1µF ceramic capacitor to GND.
—	EP	Exposed Pad (TDFN Only). Connect EP to GND.

Function Table

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	High Impedance	High Impedance
1	0	X	Shutdown (see note)	

RECEIVING (MAX14840E)			
INPUTS			OUTPUTS
$\overline{RE}$	DE	A-B	RO
0	X	≥ 200mV	1
0	X	≤ -200mV	0
0	X	Open/Shorted	Previous State
1	1	X	High Impedance
1	0	X	Shutdown (see note)

RECEIVING (MAX14841E)			
INPUTS			OUTPUTS
$\overline{RE}$	DE	A-B	RO
0	X	≥ -10mV	1
0	X	≤ -200mV	0
0	X	Open/Shorted	1
1	1	X	High Impedance
1	0	X	Shutdown (see note)

X = Don't care.

Note: *Shutdown mode, driver, and receiver outputs are in high impedance.*

Detailed Description

The MAX14840E/MAX14841E are +3.3V ESD-protected RS-485 transceivers intended for high-speed, half-duplex communications. A hot-swap capability eliminates false transitions on the bus during power-up or hot insertion.

The MAX14840E features symmetrical fail-safe and larger receiver hysteresis, providing improved noise rejection and improved recovered signals in high-speed and long cable applications. The MAX14841E has true fail-safe receiver inputs guaranteeing a logic-high receiver output when inputs are shorted or open. All devices have a 1-unit load receiver input impedance, allowing up to 32 transceivers on the bus.

The MAX14840E/MAX14841E transceivers draw 1.5mA (typ) supply current when unloaded or when fully loaded with the drivers disabled.

Symmetrical Fail Safe (MAX14840E)

At high data rates and with long cable lengths, the signal at the end of the cable is attenuated and distorted due to the lowpass characteristic of the transmission line. Under these conditions, fail-safe RS-485 receivers, which have offset threshold voltages, produce recovered signals with uneven mark-space ratios. The MAX14840E has symmetrical receiver thresholds, as shown in Figure 9. This produces near even mark-space ratios at the receiver's output (RO). The MAX14840E also has higher receiver hysteresis than the MAX14841E and most other RS-485 transceivers. This results in higher receiver noise tolerance.

Symmetrical fail safe means that the receiver's output (RO) remains at the same logic state that it was before the differential input voltage V_{OD} went to 0V. Under normal conditions, where UART signaling is used, this means that the state on the line prior to all drivers being disabled is a logic-high (i.e., a UART STOP bit).

True Fail Safe (MAX14841E)

The MAX14841E guarantees a logic-high receiver output when the receiver inputs are shorted or open or when they are connected to a terminated transmission line with all drivers disabled. This is the case if the receiver input threshold is between -10mV and -200mV. RO is logic-high if the differential receiver input voltage V_{OD} is greater than or equal to -10mV.

Hot-Swap Capability

Hot-Swap Inputs

When circuit boards are inserted into a hot or powered backplane, disturbances to the enable inputs and differential receiver inputs can lead to data errors. Upon initial circuit board insertion, the processor undergoes its power-up sequence. During this period, the processor output drivers are high impedance and are unable to drive the DE and $\overline{RE}$ inputs of the MAX14840E/MAX14841E to a defined logic level. Leakage currents up to 10µA from the high-impedance output of a controller could cause DE and $\overline{RE}$ to drift to an incorrect logic state. Additionally, parasitic circuit board capacitance could cause coupling of V_{CC} or GND to DE and $\overline{RE}$. These factors could improperly enable the driver or receiver. However, the MAX14840E/MAX14841E have hot-swap inputs that avoid these potential problems.

When V_{CC} rises, an internal pulldown circuit holds DE low and $\overline{RE}$ high. After the initial power-up sequence, the pulldown circuit becomes transparent, resetting the hot-swap-tolerable inputs.

How-Swap Input Circuitry

The MAX14840E/MAX14841E DE and $\overline{RE}$ enable inputs feature hot-swap capability. At the input, there are two nMOS devices, M1 and M2 (Figure 10). When V_{CC} ramps

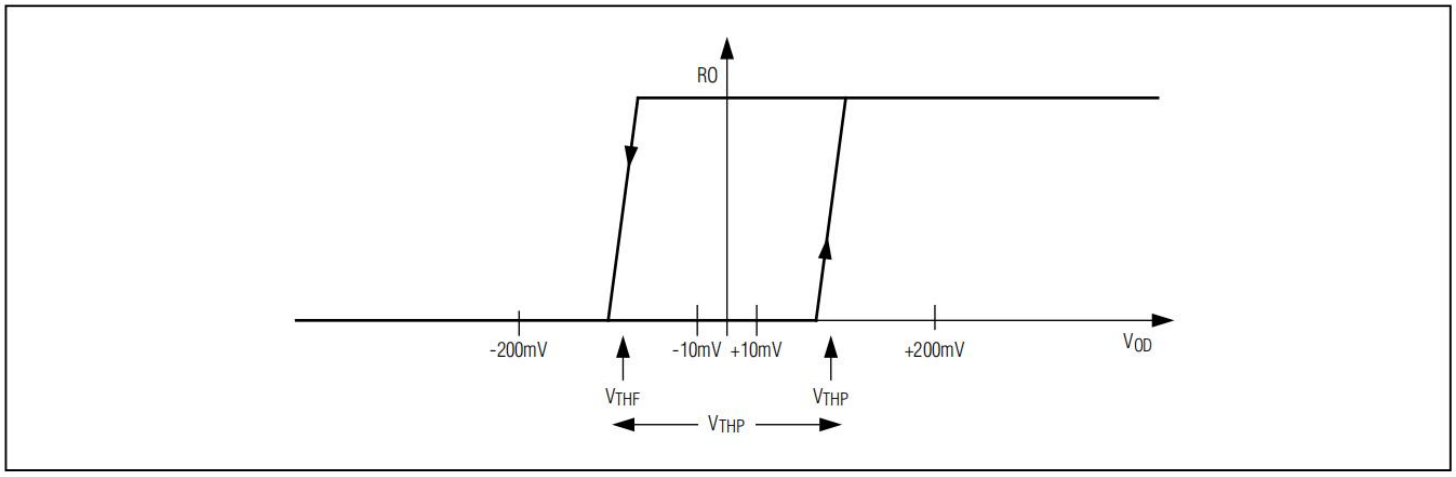


Figure 9. Symmetrical Hysteresis

from 0V, an internal 15µs timer turns on M2 and sets the SR latch that also turns on M1. Transistors M2 (a 1mA current sink) and M1 (a 100µA current sink) pull DE to GND through a 5.6kΩ resistor. M2 is designed to pull DE to the disabled state against an external parasitic capacitance up to 100pF that can drive DE high. After 15µs, the timer deactivates M2 while M1 remains on, holding DE low against three-state leakages that can drive DE high. M1 remains on until an external source overcomes the required input current. At this time, the SR latch resets and M1 turns off. When M1 turns off, DE reverts to a standard, high-impedance CMOS input. Whenever V_{CC} drops below 1V, the hot-swap input is reset.

For $\overline{RE}$, there is a complementary circuit employing two pMOS devices pulling $\overline{RE}$ to V_{CC}.

±35kV ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs of the MAX14840E family of devices have extra protection against static electricity. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the MAX14840E/MAX14841E keep working without latchup or damage.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the MAX14840E/MAX14841E are characterized for protection to the following limits:

- ±35kV HBM
- ±20kV using the Air Gap Discharge method specified in IEC 61000-4-2
- ±12kV using the Contact Discharge method specified in IEC 61000-4-2

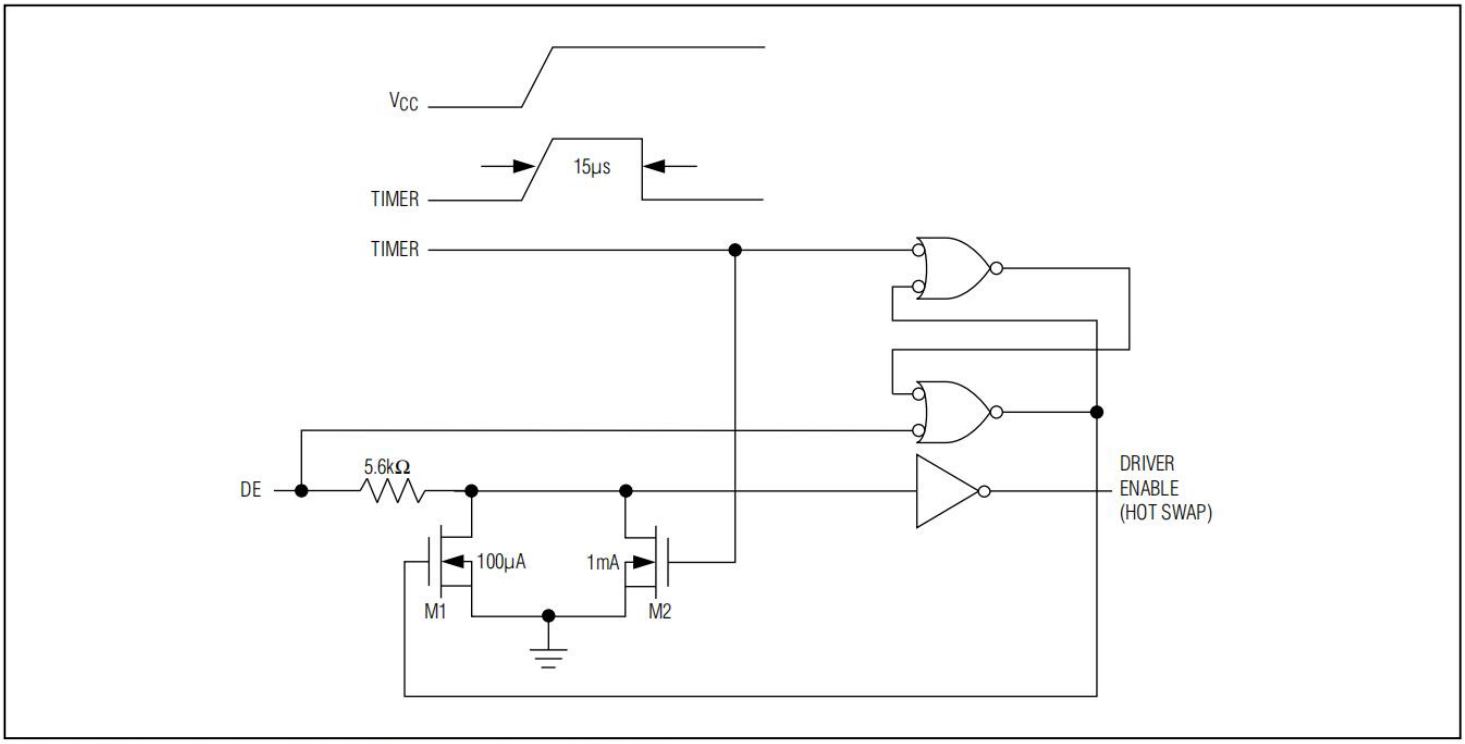


Figure 10. Simplified Structure of the Driver Enable Pin (DE)

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 11 shows the HBM, and Figure 12 shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The MAX14840E/MAX14841E family of devices helps you design equipment to meet IEC 61000-4-2, without the need for additional ESD protection components.

The major difference between tests done using the HBM and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the HBM.

Figure 13 shows the IEC 61000-4-2 model, and Figure 14 shows the current waveform for IEC 61000-4-2 ESD Contact Discharge test.

Applications Information

High-Speed Operation

The MAX14840E and MAX14841E are high-performance RS-485 transceivers supporting data rates up to 40Mbps.

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. Current limit on the output stage provides immediate

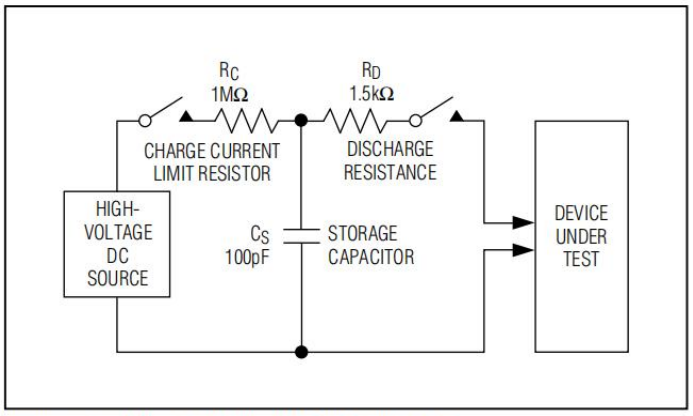


Figure 11. Human Body ESD Test Model

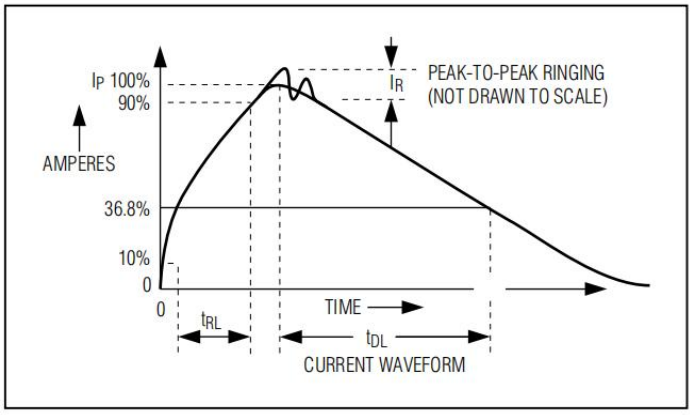


Figure 12. Human Body current Waveform

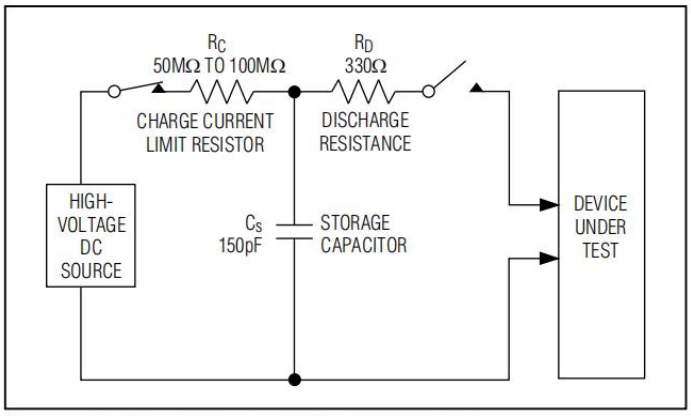


Figure 13. IEC 61000-4-2 ESD Test Model

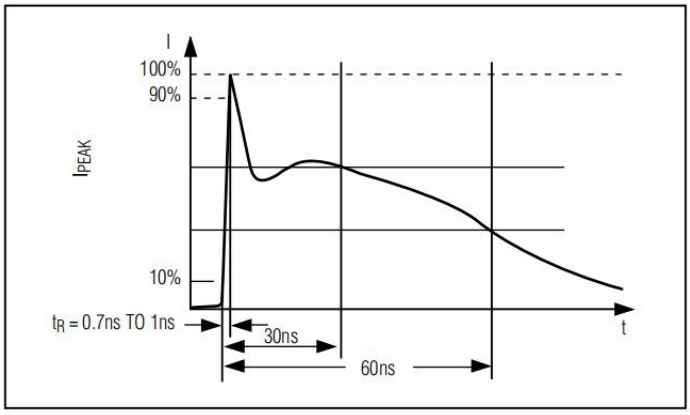


Figure 14. IEC 61000-4-2 ESD Generator Current Waveform

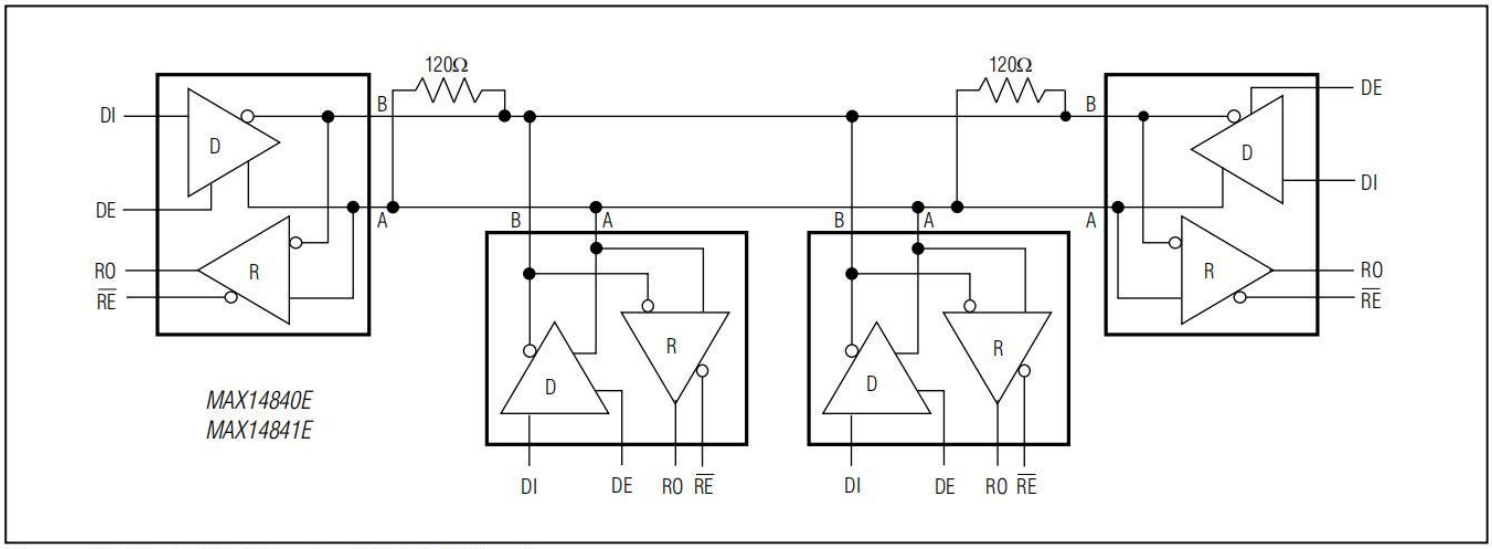


Figure 15. Typical Half-Duplex RS-485 Network

protection against short circuits over the whole common-mode voltage range (see the *Typical Operating Characteristics* section). Additionally, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature exceeds +160°C (typ).

Low-Power Shutdown Mode

Low-power shutdown mode is initiated by bringing $\overline{RE}$ high and DE low. In shutdown, the devices draw less than 10µA of supply current.

$\overline{RE}$ and DE can be driven simultaneously; the parts are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 800ns, the parts are guaranteed to enter shutdown.

Typical Applications

The MAX14840E/MAX14841E transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figure 15 shows a typical network application circuit. To minimize reflections, terminate the line at both ends with its characteristic impedance and keep stub lengths off the main line as short as possible.

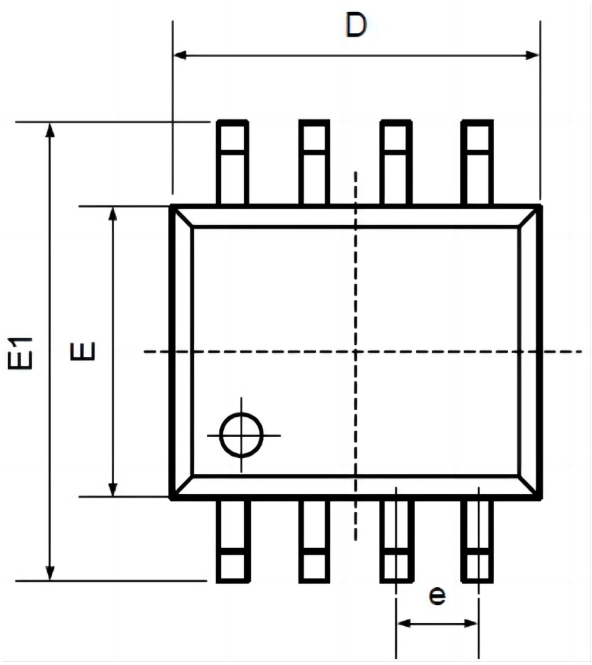
Chip Information

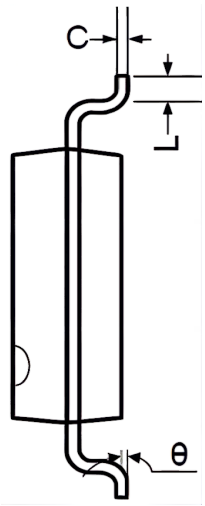
PROCESS: BiCMOS

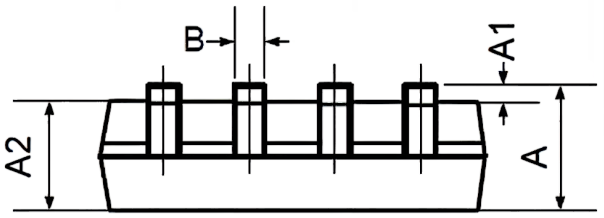
ORDERING INFORMATION

Order Number	Package	Package Quantity	Marking On The park	Temperature
MAX14840EASA-TUDI	SOP8	Tape,Reel,2500	MAX14840EASA	–40°C to +125°C

Package SOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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