

钍地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65HVD1780/HVD1781/HVD1782

Fault-Protected RS-485 Transceivers With 3.3-V to 5-V Operation

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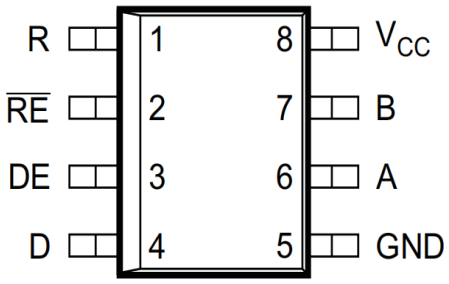
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semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

●Bus-Pin Fault Protection to: – > ±70 V (SN65HVD1780, SN65HVD1781)
– > ±30 V (SN65HVD1782)
●Operation With 3.3-V to 5-V Supply Range
●±16-kV HBM Protection on Bus Pins
●Reduced Unit Load for Up to 320 Nodes
●Failsafe Receiver for Open-Circuit, Short-Circuit, and Idle-Bus Conditions
●Low Power Consumption
– Low Standby Supply Current, 1 μA Maximum
– I_{CC} 4-mA Quiescent Current During Operation
●Pin-Compatible With Industry-Standard SN75176
●Signaling Rates of 115 kbps, 1 Mbps, and up to 10 Mbps
●Create a Custom Design using the SN65HVD178x with the WEBENCH®Power Designer



D Package and P Package
8-Pin SOIC and 8-Pin PDIP
Top View

Applications

●HVAC Networks
●Security Electronics
● Building Automation
●Telecommunication Equipment
●Motion Control
●Industrial Networks

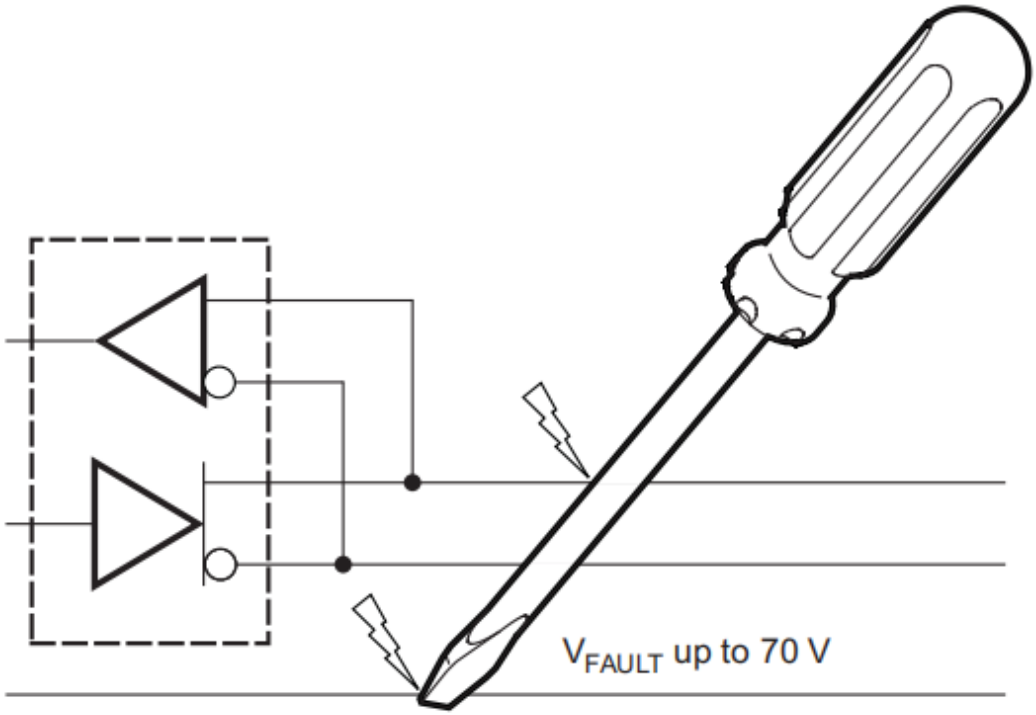
Description

The SN65HVD178x devices are designed to survive overvoltage faults such as direct shorts to power supplies, mis-wiring faults, connector failures, cable crushes, and tool mis-applications. The devices are also robust to ESD events with high levels of protection to the human-body-model specification.

The SN65HVD178x devices combine a differential driver and a differential receiver, which operate from a single power supply. In the SN65HVD1782, the driver differential outputs and the receiver differential nputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. This port features a wide common-mode voltage range, making the devices suitable for multipoint applications over long cable runs. These devices are characterized from –40 ° C to 125 ° C. These devices are pin-compatible with the industry-standard SN75176 transceiver, making them drop-in upgrades in most systems.

These devices are fully compliant with ANSI TIA/EIA 485-A with a 5-V supply and can operate with a 3.3-V supply with reduced driver output voltage for low-power applications.For applications where operation is required over an extended common-mode voltage range, see the SN65HVD1785 (SLLS872) data sheet.

Protection Against Bus Shorts



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
A	6	Bus input/output	Driver output or receiver input (complimentary to B)
B	7	Bus input/output	Driver output or receiver input (complimentary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable low
V_{CC}	8	Supply	4.5-V to 5.5-V supply

7 Specifications

7.1 Absolute Maximum Ratings(1)

			MIN	MAX	UNIT
Supply voltage, V_{CC}			–0.5	7	V
Voltage at bus pin	SN65HVD1780, SN65HVD1781	A, B pins	–70	70	V
	SN65HVD1782	A, B pins	–70	30	
Input voltage at any logic pin			–0.3	V_{CC} + 0.3	V
Transient overvoltage pulse through 100 Ω per TIA-485			–70	70	V
Receiver output current			–24	24	mA
Junction temperature, T_J				170	°C
Storage temperature, T_{stg}			–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings: JEDEC

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	Bus pins and GND	±16000	V
			All pins	±4000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		±2000	
		Machine model JEDEC Standard 22, Test Method A115, all pins		±400	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings: IEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 60749-26 ESD (human body model), bus terminals and GND	±16000	V

7.4 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.15	5	5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)(1)		–7		12	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)		0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_O	Output current, driver		–60		60	mA
	Output current, receiver		–8		8	mA
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
$1/t_{UI}$	Signaling rate	SN65HVD1780			115	kbps
		SN65HVD1781			1	Mbps
		SN65HVD1782			10	
T_A	Operating free-air temperature (See *Power Dissipation Characteristics*)	5-V supply	–40		105	°C
		3.3-V supply	–40		125	
T_J	Junction temperature		–40		150	°C

(1) By convention, the least positive (most negative) limit is designated as minimum in this data sheet.

7.5 Thermal Information

THERMAL METRIC(1)			SN65HVD178x		UNIT
			D (SOIC)	P (PDIP)	
			8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	JEDEC high-K model	138	59	°C/W
		JEDEC low-K model	242	128	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		61	61	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		62	39	°C/W
ψ_{JT}	Junction-to-top characterization parameter		3.4	17.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter		33.4	28.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, 4.75 V ≤ V_{CC} 375 Ω on each output to –7 V to 12 V Figure 6		T_A < 85°C	1.5			V
				T_A < 125°C	1.4			
		R_L = 54 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V		T_A < 85°C	1.7	2		
				T_A < 125°C	1.5			
		R_L = 54 Ω, 3.15 V ≤ V_{CC} ≤ 3.45 V			0.8	1		
		R_L = 100 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V		T_A < 85°C	2.2	2.5		
				T_A < 125°C	2			
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L = 54 Ω			–50	0	50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage				1	V_{CC}/2	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage				–50	0	50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors See Figure 7				500		mV
C_{OD}	Differential output capacitance					23		pF
V_{IT+}	Positive-going receiver differential input voltage threshold					–100	–35	mV
V_{IT-}	Negative-going receiver differential input voltage threshold				–180	–150		mV
V_{HYS}	Receiver differential input voltage threshold hysteresis (V_{IT+} – V_{IT-})				30	50		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA			2.4	V_{CC} – 0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA		T_A < 85°C		0.2	0.4	V
				T_A < 125°C			0.5	
$I_{I(LOGIC)}$	Driver input, driver enable, and receiver enable input current				–50		50	µA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}			–1		1	µA
I_{OS}	Driver short-circuit output current				–200		200	mA
$I_{I(BUS)}$	Bus input current (disabled driver)	V_{CC} = 3.15 to 5.5 V or V_{CC} = 0 V, DE at 0 V	V_I = 12 V	1780, 1781		75	100	µA
				1782		400	500	
			V_I = –7 V	1780, 1781	–60	–40		
				1782	–400	–300		
I_{CC}	Supply current (quiescent)	Driver and receiver enabled		DE = V_{CC}, RE = GND, no load		4	6	mA
		Driver enabled, receiver disabled		DE = V_{CC}, RE = V_{CC}, no load		3	5	
		Driver disabled, receiver enabled		DE = GND, RE = GND, no load		2	4	
		Drive and receiver disabled (standby mode)		DE = GND, D = open, RE = V_{CC}, no load, T_A < 85°C		0.15	1	µA
				DE = GND, D = open, RE = V_{CC}, no load, T_A < 125°C			12	
	Supply current (dynamic)	See *Typical Characteristics*						

7.7 Power Dissipation Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MAX	UNIT
P_D	Power dissipation	V_{CC} = 5.5 V, T_J = 150°C, R_L = 300 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, unterminated(1)	290	mW
		V_{CC} = 5.5 V, T_J = 150°C, R_L = 100 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-422 load(1)	320	
		V_{CC} = 5.5 V, T_J = 150°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-485 load(1)	400	
T_{SD}	Thermal-shutdown junction temperature		170	°C

(1) Driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: 1 Mbps.

7.8 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER (SN65HVD1780)							
t_r, t_f	Driver differential output rise or fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 8	3.15 V < V_{CC} < 3.45 V	0.4	1.4	1.8	µs
			3.15 V < V_{CC} < 5.5 V	0.4	1.7	2.6	
t_{PHL}, t_{PLH}	Driver propagation delay	R_L = 54 Ω, C_L = 50 pF, See Figure 8			0.8	2	µs
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$	R_L = 54 Ω, C_L = 50 pF, See Figure 8			20	250	ns
t_{PHZ}, t_{PLZ}	Driver disable time	See Figure 9 and Figure 10			0.1	5	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled	See Figure 9 and Figure 10		0.2	3	µs
		Receiver disabled	See Figure 9 and Figure 10		3	12	
DRIVER (SN65HVD1781)							
t_r, t_f	Driver differential output rise or fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 8		50		300	ns
t_{PHL}, t_{PLH}	Driver propagation delay	R_L = 54 Ω, C_L = 50 pF, See Figure 8				200	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$	R_L = 54 Ω, C_L = 50 pF, See Figure 8				25	ns
t_{PHZ}, t_{PLZ}	Driver disable time	See Figure 9 and Figure 10				3	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled	See Figure 9 and Figure 10			300	ns
		Receiver disabled	See Figure 9 and Figure 10			10	µs
DRIVER (SN65HVD1782)							
t_r, t_f	Driver differential output rise or fall time	R_L = 54 Ω, C_L = 50 pF	All V_{CC} and Temperature			50	ns
			V_{CC} > 4.5 V and T < 105°C			16	
t_{PHL}, t_{PLH}	Driver propagation delay	R_L = 54 Ω, C_L = 50 pF	See Figure 8			55	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$	R_L = 54 Ω, C_L = 50 pF	See Figure 8			10	ns
t_{PHZ}, t_{PLZ}	Driver disable time	See Figure 9 and Figure 10				3	µs

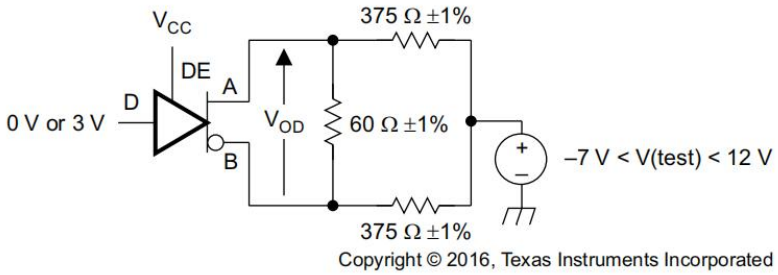
Switching Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled	See Figure 9 and Figure 10			300	ns
		Receiver disabled	See Figure 9 and Figure 10			9	µs
RECEIVER							
t_r, t_f	Receiver output rise or fall time	C_L = 15 pF, See Figure 11	All devices		4	15	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time	C_L = 15 pF, See Figure 11	SN65HVD1780, SN65HVD1781		100	200	ns
			SN65HVD1782			80	
$t_{SK(P)}$	Receiver output pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$	C_L = 15 pF, See Figure 11	SN65HVD1780, SN65HVD1781		6	20	ns
			SN65HVD1782			5	
t_{PLZ}, t_{PHZ}	Receiver disable time	Driver enabled, See Figure 12			15	100	ns
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled, See Figure 12			80	300	ns
		Driver disabled, See Figure 13			3	9	µs

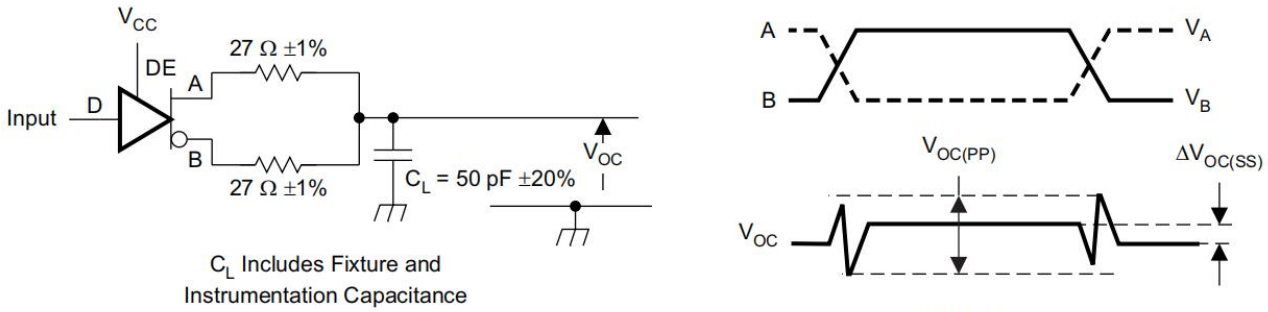
8 Parameter Measurement Information

Input generator rate is 100 kbps, 50% duty cycle, rise or fall time is less than 6 ns, output impedance is 50 Ω.



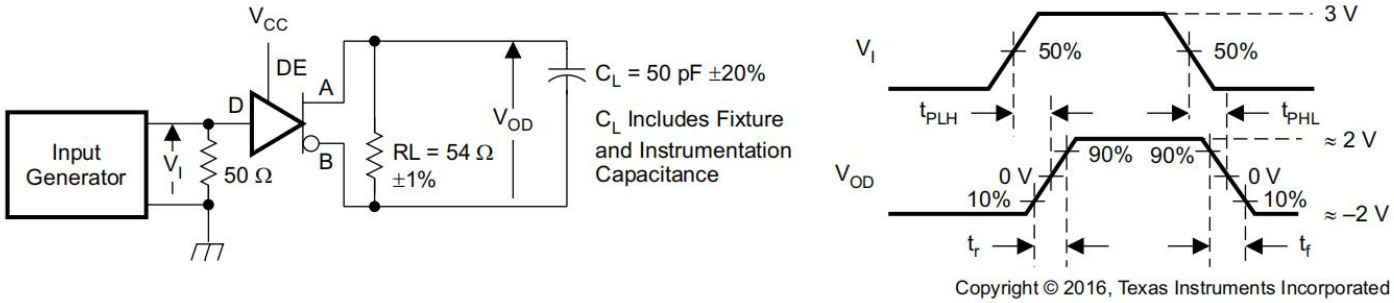
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Figure 6. Measurement of Driver Differential Output Voltage With Common-Mode Load



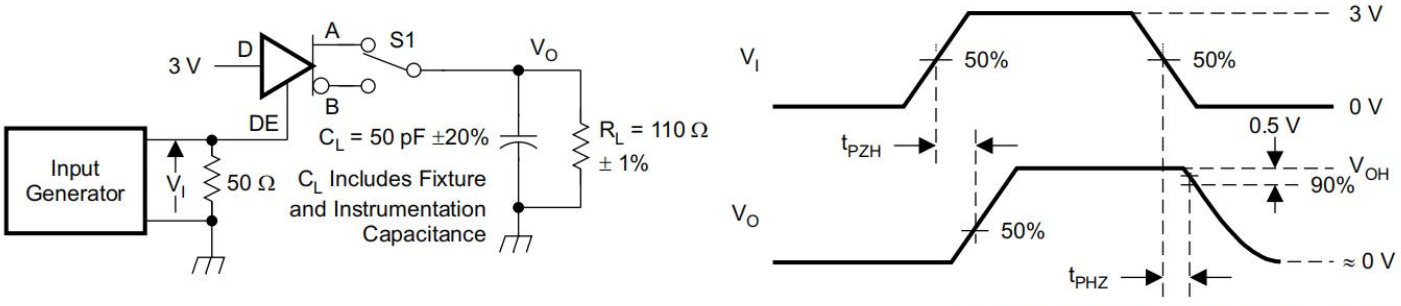
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Figure 7. Measurement of Driver Differential and Common-Mode Output With RS-485 Load



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Figure 8. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

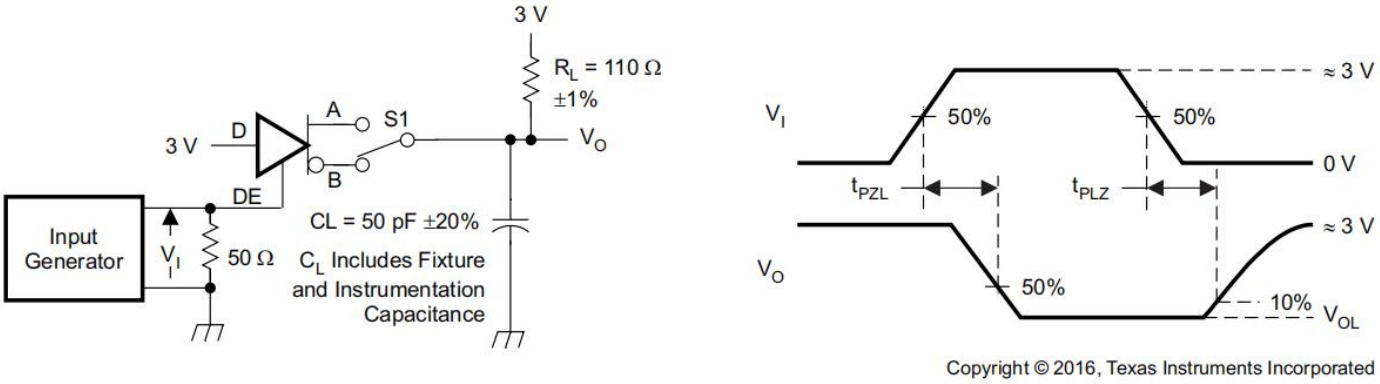


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NOTE: D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 9. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load

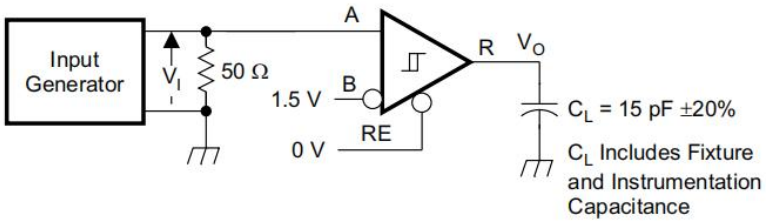
Parameter Measurement Information (continued)

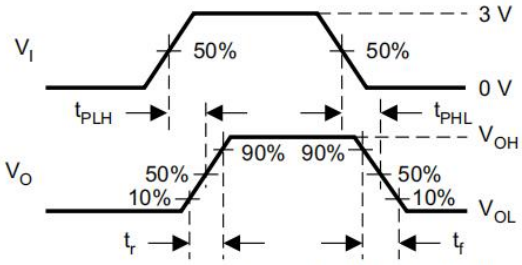


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NOTE: D at 0 V to test non-inverting output, D at 3 V to test inverting output.

Figure 10. Measurement of Driver Enable and Disable Times With Active-Low Output and Pullup Load

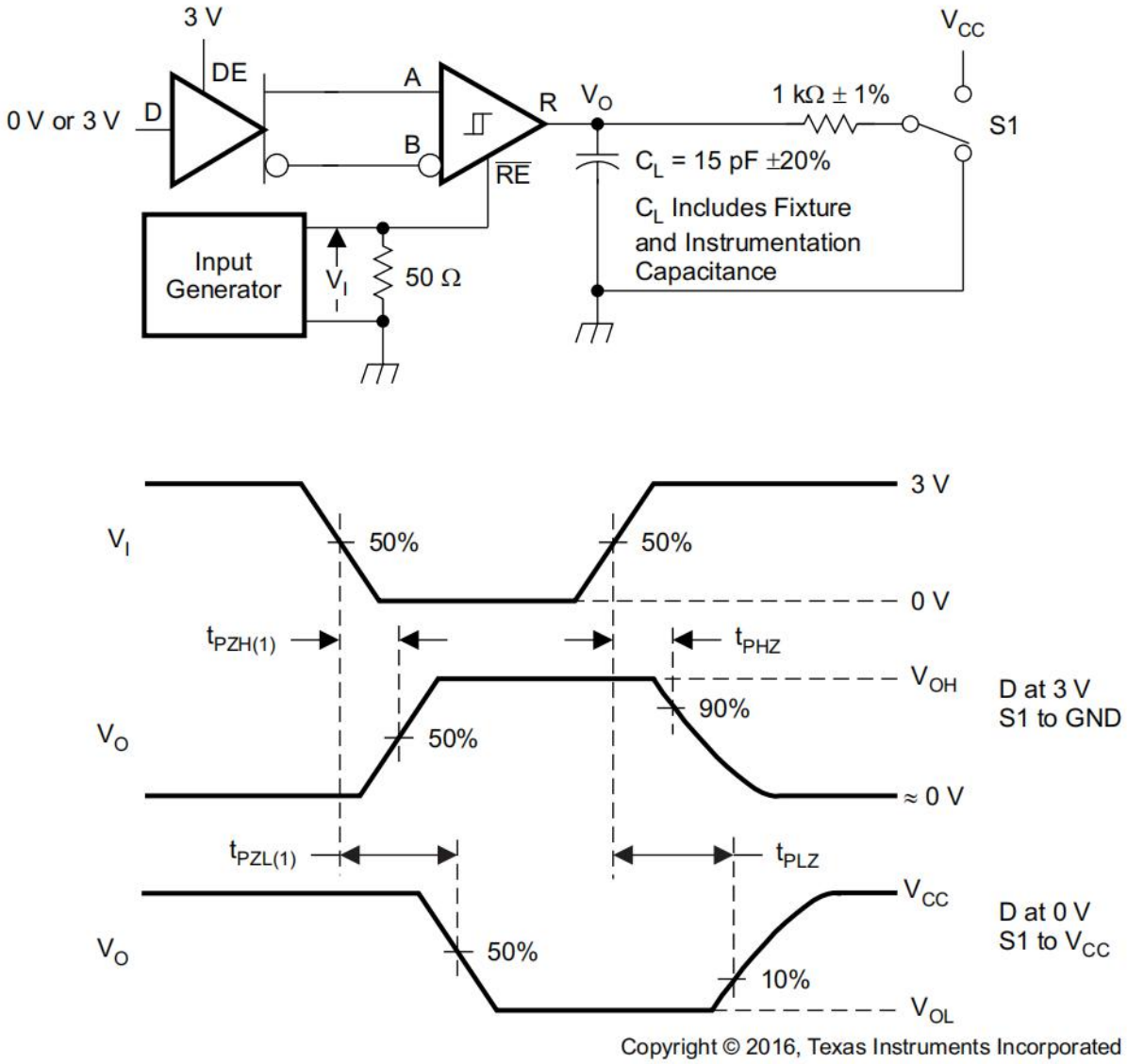




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Figure 11. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

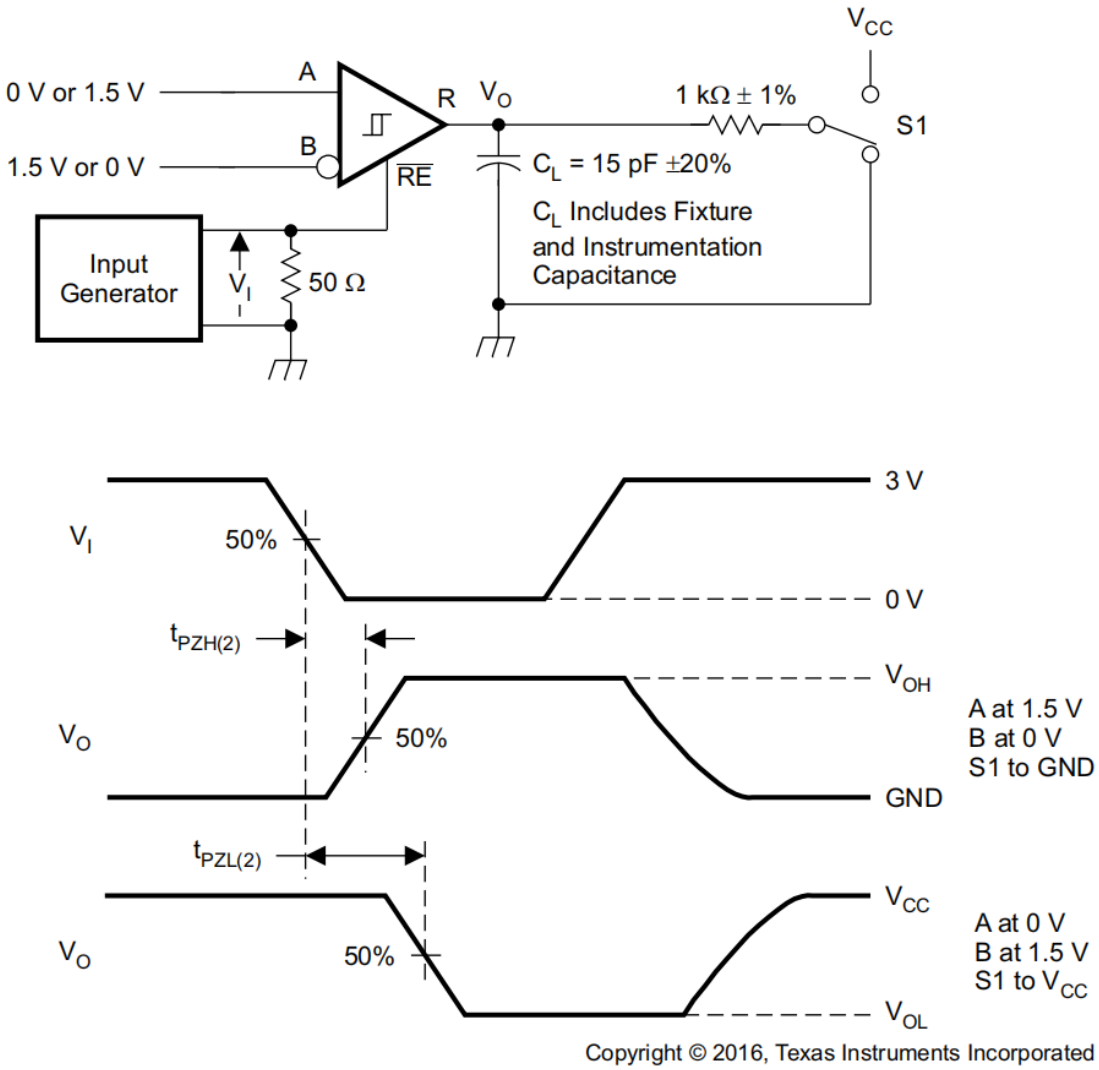
Parameter Measurement Information (continued)



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Figure 12. Measurement of Receiver Enable and Disable Times With Driver Enabled

Parameter Measurement Information (continued)



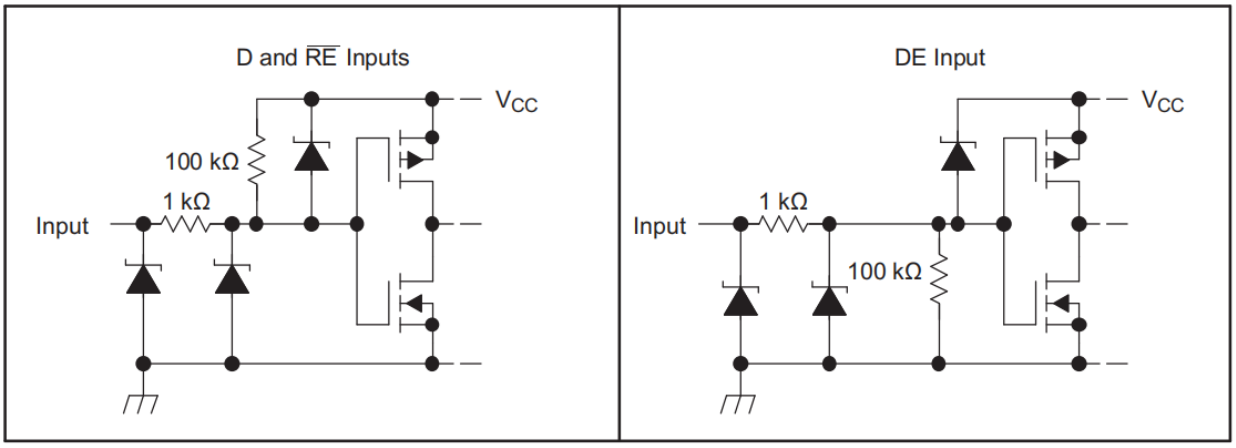
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Figure 13. SN65HVD1781 Measurement of Receiver Enable Times With Driver Disabled

Parameter Measurement Information (continued)

8.1 Equivalent Input Schematic

When the input digital pins float, internal high value resistors pull D/REB pins to V_{CC} and DE pin to GND to place the device into known states. If the voltage level of D/REB input pins is higher than that of power rail, input current can flow through the input resistor and pull up resistor to V_{CC}.



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Figure 14. Equivalent Input Schematic Diagrams

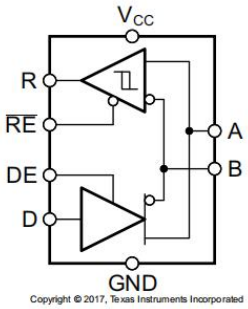
9 Detailed Description

9.1 Overview

The SN65HVD178x devices are half-duplex RS-485 transceivers available in three speed grades suitable for data transmission up to 115 kbps, 1 Mbps, and 10 Mbps.

These devices feature a wide common-mode operating range and bus-pin fault protection up to ±70 V. Each device has an active-HIGH driver enable and active-LOW receiver enable. A standby current of less than 1 µA can be achieved by disabling both driver and receiver.

9.2 Functional Block Diagram



9.3 Feature Description

Internal ESD protection circuits protect the transceiver bus terminals against ±16 kV human body model (HBM) electrostatic discharges.

Device operation is specified over a wide temperature range from –40°C to 125°C.

9.3.1 70-V Fault Protection

The SN65HVD178x family of RS-485 transceivers is designed to survive bus pin faults up to ±70 V. The SN65HVD1782 will not survive a bus pin fault with a direct short to voltages above 30 V when:

- The device is powered on, AND
- The driver is enabled (DE = HIGH), AND
  - D = HIGH AND the bus fault is applied to the A pin, OR
  - D = LOW AND the bus fault is applied to the B pin

Under other conditions, the device will survive shorts to bus pin faults up to ±70 V. Table 1 summarizes the conditions under which the device may be damaged, and the conditions under which the device will not be damaged.

Table 1. Device Conditions

POWER	DE	D	A	B	RESULTS
OFF	X	X	$-70\ V < V_A < 70\ V$	$-70\ V < V_B < 70\ V$	Device survives
ON	L	X	$-70\ V < V_A < 70\ V$	$-70\ V < V_B < 70\ V$	Device survives
ON	H	L	$-70\ V < V_A < 70\ V$	$-70\ V < V_B < 30\ V$	Device survives
ON	H	L	$-70\ V < V_A < 70\ V$	$30\ V < V_B$	Damage may occur
ON	H	H	$-70\ V < V_A < 30\ V$	$-70\ V < V_B < 30\ V$	Device survives
ON	H	H	$30\ V < V_A$	$-70\ V < V_B < 30\ V$	Damage may occur

9.3.2 Receiver Failsafe

The SN65HVD178x family of half-duplex transceivers provides internal biasing of the receiver input thresholds in combination with large input-threshold hysteresis. At a positive input threshold of V_{IT+} = –35 mV and an input hysteresis of V_{HYS} = 30 mV, the receiver output remains logic high under bus-idle, bus-short, or open bus conditions in the presence of up to 130 mV_{PP} differential noise without the need for external failsafe biasing resistors.

9.3.3 Hot-Plugging

These devices are designed to operate in "hot swap" or "hot pluggable" applications. Key features for hot-pluggable applications are power-up and power-down glitch-free operation, default disabled input and output pins, and receiver failsafe.

As shown in Figure 1, an internal power-on reset circuit keeps the driver outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no problems will occur on the bus pin outputs as the power supply turns on or turns off.

As shown in *Device Functional Modes*, the enable inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

9.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus, when left open, the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 2. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled (1)
X	OPEN	Z	Z	Driver disabled by default (1)
OPEN	H	H	L	Actively drive bus high by default

(1) When both the driver and receiver are disabled, the device enters a low-power standby mode.

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-}, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and V_{IT-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Table 3. Receiver Function Table

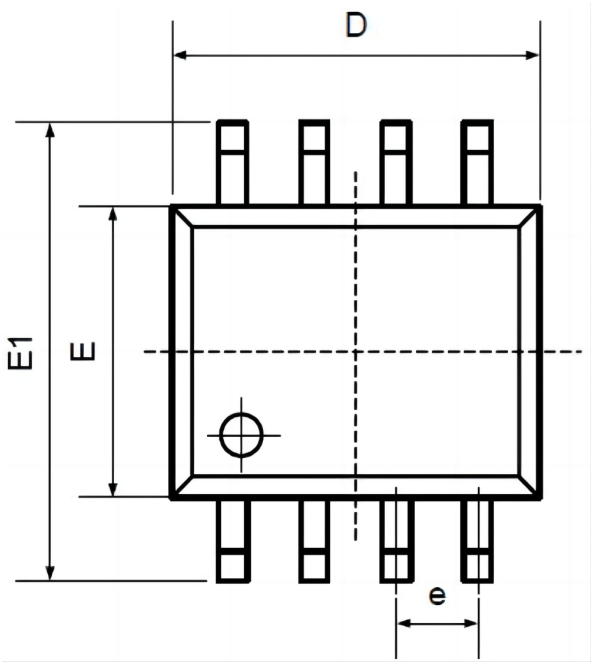
DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus high
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled (1)
X	OPEN	Z	Receiver disabled by default (1)
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

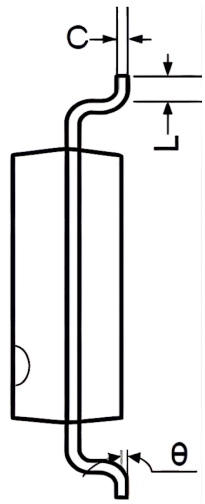
(1) When both the driver and receiver are disabled, the device enters a low-power standby mode.

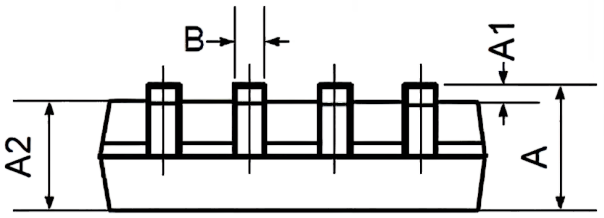
Order information

Order Number	Package	Package Quantity	Marking On The park
SN65HVD1780DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD1780DR
SN65HVD1781DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD1781DR
SN65HVD1782DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD1782DR

Package SOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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