

钍地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65HVD485E

Half-duplex RS-485 transceiver

网址 www.sztdbdt.com

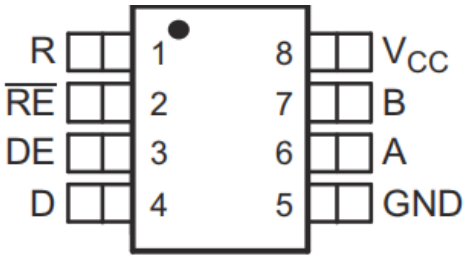
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- Up to 15kV bus pin ESD protection
- 1/2 unit load: up to 64 nodes on a single
- Bus fail-safe receiver
- Non-intrusive power-up and power-down bus inputs and outputs
- Small VSSOP-8 package
- Meets exceeds TIA/EIA-485A standard requirements
- Industry-standard SN75176 compatible package



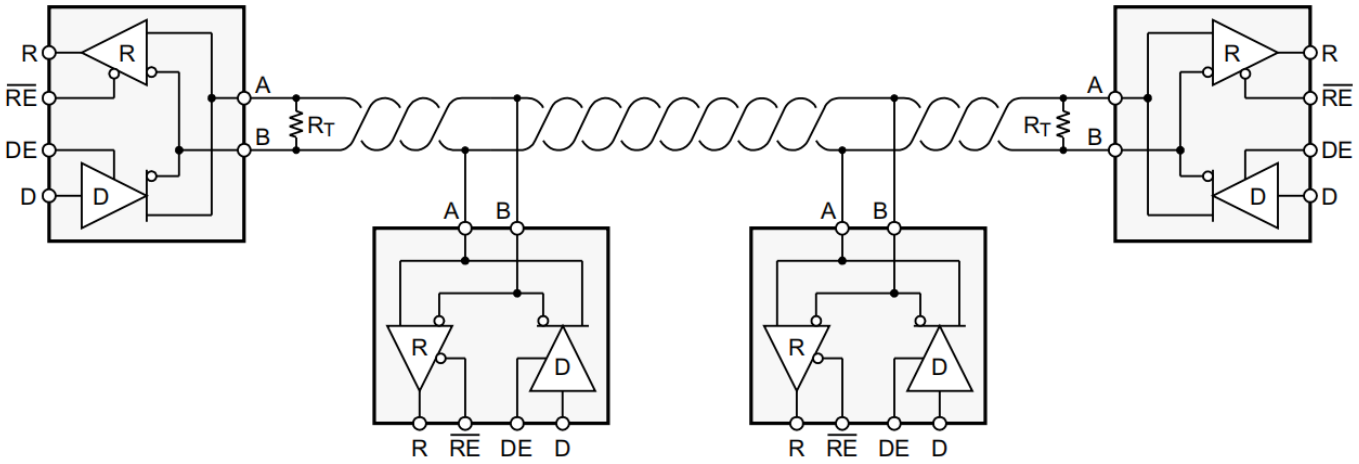
Applications

- Motor control
- Power inverters
- Industrial automation
- Building automation networks
- Industrial process control
- Battery-powered applications
- communications equipment

Description

The SN65HVD485E device is a half-duplex transceiver designed specifically for RS-48 data bus networks. The device is powered by a 5V supply and is fully compliant with the TIA/EIA-485A standard. It is suitable for transmitting at rates up to 10Mbps over long twisted-pair cables and is designed to operate at an exceptionally low supply current (typically less than 2mA, excluding load). the device is in the inactive shutdown mode, the supply current drops to less than 1mA. The device's wide common-mode range and high ESD protection level it suitable for demanding applications, such as electrical inverters, status/command signals on telecom racks, wired chassis interconnects, and industrial automation networks where noise immunity is critical . The 65HVD485E device is industry-standard pin-compatible with the SN75176 device. Anundervoltage lockout circuit keeps the outputs a high-impedance state until the supply voltage stabilizes. A thermal shutdown feature protects the device from damage caused by system fault conditions. The SN65HVD485 device can operate in ambient temperatures ranging from – 40 ° C to 85 ° C.

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典型应用原理图

5 Device Comparison Table

Improved Replacement for Devices

PART NUMBER	REPLACE WITH	BENEFITS
ADM485	SN65HVD485E	Better ESD protection (±15 kV versus unspecified) Faster signaling rate (10 Mbps versus 5 Mbps) More nodes on a bus (64 versus 32) Wider power supply tolerance (10% vs 5%)
SP485E	SN65HVD485E	More nodes on a bus (64 versus 32) Wider power supply tolerance (10% versus 5%)
LMS485E	SN65HVD485E	Higher signaling rate (10 Mbps versus 2.5 Mbps) More nodes on a bus (64 versus 32) Wider power supply tolerance (10% versus 5%)
DS485	SN65HVD485E	Higher signaling rate (10 Mbps versus 2.5 Mbps) Better ESD (±15 kV versus ±2 kV) More nodes on a bus (64 versus 32) Wider power supply tolerance (10% versus 5%)
LTC485	SN65HVD485E	Better ESD (±15 kV versus ±2 kV) Wider power supply tolerance (10% versus 5%)
MAX485E	SN65HVD485E	Higher signaling rate (10 Mbps versus 2.5 Mbps) More nodes on a bus (64 versus 32) Wider power supply tolerance (10% versus 5%)
ST485E	SN65HVD485E	Higher signaling rate (10 Mbps versus 5 Mbps) Wider power supply tolerance (10% versus 5%)
ISL8485E	SN65HVD485E	More nodes on a bus (64 versus 32) Faster signaling rate (10 Mbps versus 5 Mbps)

表 **6-1. Pin Functions**

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital input	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low
V_{CC}	8	Supply	4.5-V to 5.5-V supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	- 0.5	7	V
	Voltage range at A or B	- 9	14	V
	Voltage range at any logic pin	- 0.3	V_{CC} + 0.3	V
	Receiver output current	- 24	24	mA
	Voltage input range, transient pulse, A and B, through 100 Ω (see 图 8-13)	- 50	50	V
T_J	Junction temperature	170	170	°C
	Continuous total power dissipation	Refer to 节 7.11		
T_{stg}	Storage temperature	- 65	130	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 7.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus pins and GND	±15000	V
			All pins	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)		- 7		12	V
V_{IH}	High-level input voltage (D, DE, or RE inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (D, DE, or RE inputs)		0		0.8	V
V_{ID}	Differential input voltage		- 12		12	V
I_O	Output current	Driver	- 60		60	mA
		Receiver	- 8		8	
R_L	Differential load resistance		54	60		Ω
$1/t_{UI}$	Signaling rate		0		10	Mbps
T_A	Operating free-air temperature		- 40		85	°C
T_J	Junction temperature(2)		- 40		130	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.
(2) See 节 7.4 for information on maintenance of this specification for the DGK package.

7.4 Thermal Information

THERMAL METRIC(1)		SN65HVD485E			UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	116.7	137.8	84.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	31.2	65.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	71.7	62.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	0.6	31.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	70.5	60.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) See the *Package Thermal Characterization Methodologies* application note (SZZA003) for an explanation of this parameter.

7.5 Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$\lvert V_{OD}\rvert$	Differential output voltage	I_O = 0, No load	3	4.3		V
		R_L = 54 W (see 图 8-1)	1.5	2.3		
		V_{TEST} = −7 V to 12 V (see 图 8-2)	1.5			
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage	See 图 8-1 and 图 8-2	−0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See 图 8-3	1	2.6	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		−0.1	0	0.1	V
$V_{OC(PP)}$	Common-mode output voltage	See 图 8-3		500		mV
I_{OZ}	High-impedance output current	See receiver input currents				μA
I_I	Input current	D, DE	−100		100	μA
I_{OS}	Short-circuit output current	−7 V ≤ V_O ≤ 12 V (see 图 8-7)	−250		250	mA

(1) All typical values are at 25°C and with a 5-V supply.

7.6 Electrical Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = －8 mA		－85	－10	mV
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA	－200	－115		mV
V_{hys}	Hysteresis voltage (V_{IT+} － V_{IT-})			30		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = －8 mA (see 图 8-8)	4	4.6		V
V_{OL}	Low-level output voltage	V_{ID} = －200 mV, I_{OH} = 8 mA (see 图 8-8)		0.15	0.4	V
I_{OZ}	High-impedance-state output current	V_O = 0 to V_{CC}, $\overline{RE}$ = V_{CC}	－1		1	μA
I_I	Bus input current	V_{IH} = 12 V, V_{CC} = 5 V			0.5	mA
		V_{IH} = 12 V, V_{CC} = 0			0.5	
		V_{IH} = －7 V, V_{CC} = 5 V	－0.4			
		V_{IH} = －7 V, V_{CC} = 0	－0.4			
I_{IH}	High-level input current ($\overline{RE}$)	V_{IH} = 2 V	－60	－30		μA
I_{IL}	Low-level input current ($\overline{RE}$)	V_{IL} = 0.8 V	－60	－30		μA
C_{diff}	Differential input capacitance	V_I = 0.4 sin (4E6 π t) + 0.5 V, DE at 0 V		7		pF

(1) All typical values are at 25°C and with a 5-V supply.

7.7 Power Dissipation Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{(AVG)}$	Average power dissipation	R_L = 54 Ω, Input to D is a 10 Mbps 50% duty cycle square wave V_{CC} at 5.5 V, T_J = 130°C			219	mW
T_{SD}	Thermal shut-down junction temperature			165		°C

7.8 Supply Current

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{CC}	Driver and receiver enabled	D at V_{CC} or open or 0 V,	DE at V_{CC}, RE at 0 V, No load			2	mA
	Driver and receiver disabled	D at V_{CC} or open,	DE at 0 V, RE at V_{CC}			1	mA

(1) All typical values are at 25°C and with a 5-V supply.

7.9 Switching Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 54 Ω, C_L = 50 pF (see 图 8-4)			30	ns
t_{PHL}	Propagation delay time, high-to-low-level output				30	ns
t_r	Differential output signal rise time				25	ns
t_f	Differential output signal fall time				25	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)				5	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	R_L = 110 Ω, $\overline{RE}$ at 0 V (see 图 8-5)			150	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output				100	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	R_L = 110 Ω, $\overline{RE}$ at 0 V (see 图 8-6)			150	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output				100	ns
$t_{PZH(SHN)}$	Propagation delay time, shutdown-to-high-level output	R_L = 110 Ω, $\overline{RE}$ at VCC (see 图 8-5)			2600	ns
$t_{PZL(SHDN)}$	Propagation delay time, shutdown-to-low-level output	R_L = 110 Ω, $\overline{RE}$ at VCC (see 图 8-6)			2600	ns

7.10 Switching Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF (see 图 8-9)			200	ns
t_{PHL}	Propagation delay time, high-to-low-level output				200	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)			6		ns
t_r	Output signal rise time				3	ns
t_f	Output signal fall time				3	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, DE at 3 V, (see 图 8-10 and 图 8-11)			50	ns
t_{PZL}	Output enable time to low level				50	ns
t_{PHZ}	Output enable time from high level				50	ns
t_{PLZ}	Output enable time from low level				50	ns
$t_{PZH(SHDN)}$	Propagation delay time, shutdown-to-high-level output	C_L = 15 pF, DE at 0 V, (see 图 8-12)			3500	ns
$t_{PZL(SHDN)}$	Propagation delay time, shutdown-to-low-level output				3500	ns

7.11 Dissipation Ratings

PACKAGE(1)	JEDEC BOARD MODEL	T_A < 25°C POWER RATING	DERATING FACTOR(2) ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D (SIOC)	Low k(3)	507 mW	4.82 mW/°C	289 mW	217 mW
	High k(3)	824 mW	7.85 mW/°C	471 mW	353 mW
P (PDIP)	Low k(3)	686 mW	6.53 mW/°C	392 mW	294 mW
DGK (VSSOP)	Low k(3)	394 mW	3.76 mW/°C	255 mW	169 mW
	High k(4)	583 mW	5.55 mW/°C	333 mW	250 mW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(3) In accordance with the low-k thermal metric definitions of EIA/JESD51-3.
(4) In accordance with the high-k thermal metric definitions of EIA/JESDS1-7.

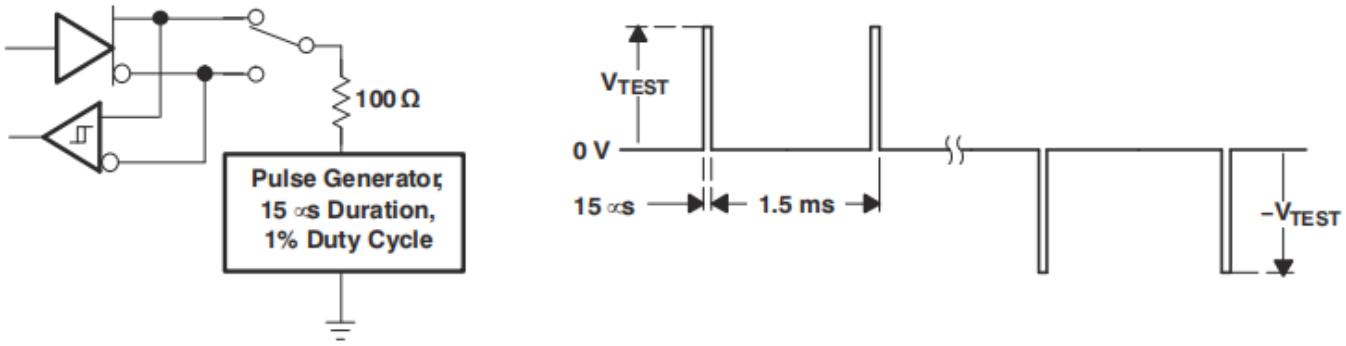


图 8-13. Test Circuit and Waveforms, Transient Over-Voltage Test

Parameter Measurement Information

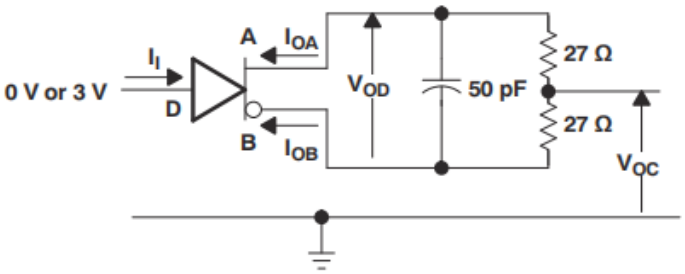


图 8-1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

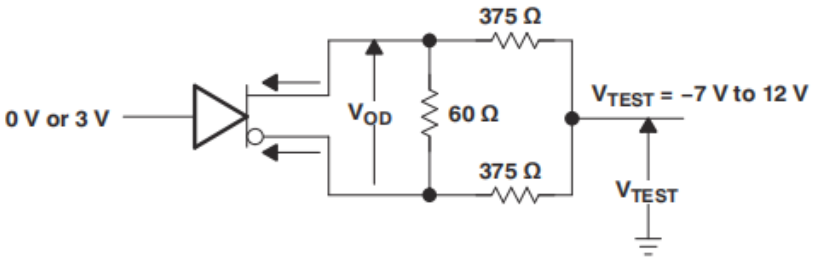


图 8-2. Driver Test Circuit, V_{OD} With Common-Mode Loading

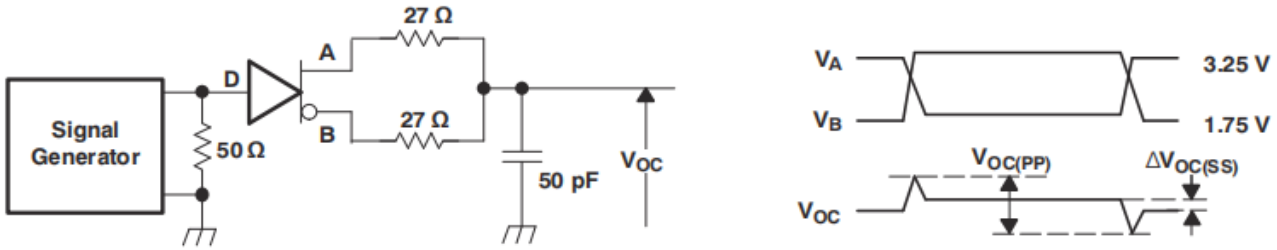


图 8-3. Driver V_{OC} Test Circuit and Waveforms

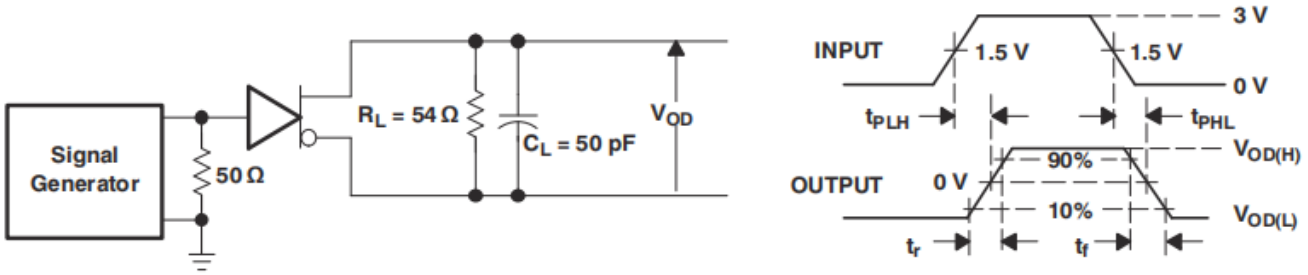
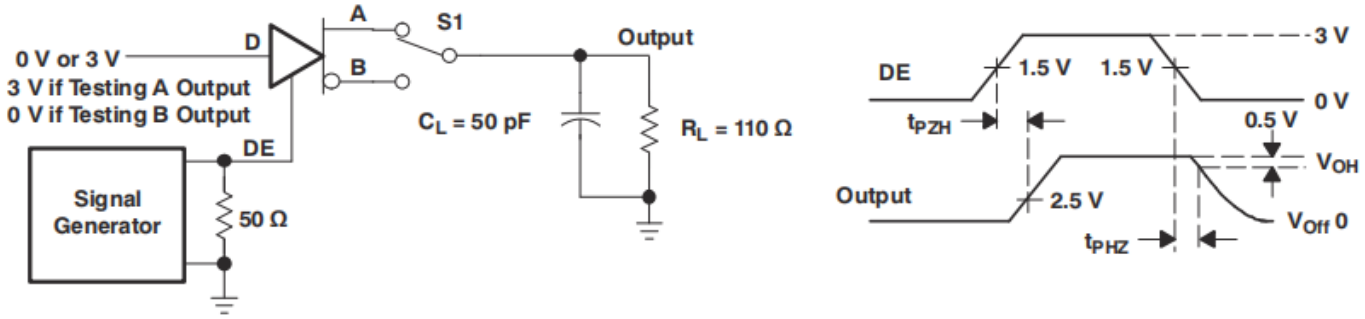


图 8-4. Driver Switching Test Circuit and Waveforms



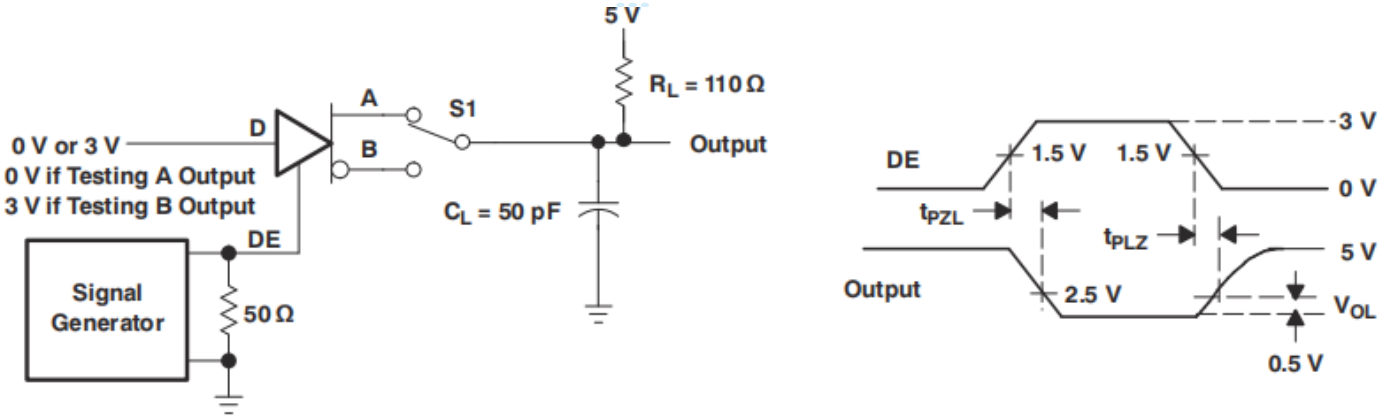


图 8-6. Driver Enable/Disable Test Circuit and Waveforms, Low Output

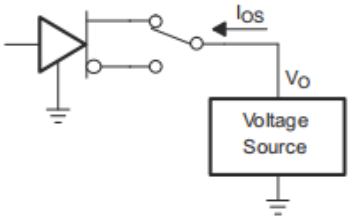


图 8-7. Driver Short-Circuit Test

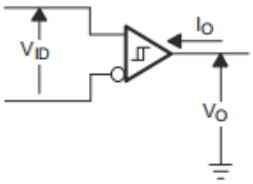


图 8-8. Receiver Parameter Definitions

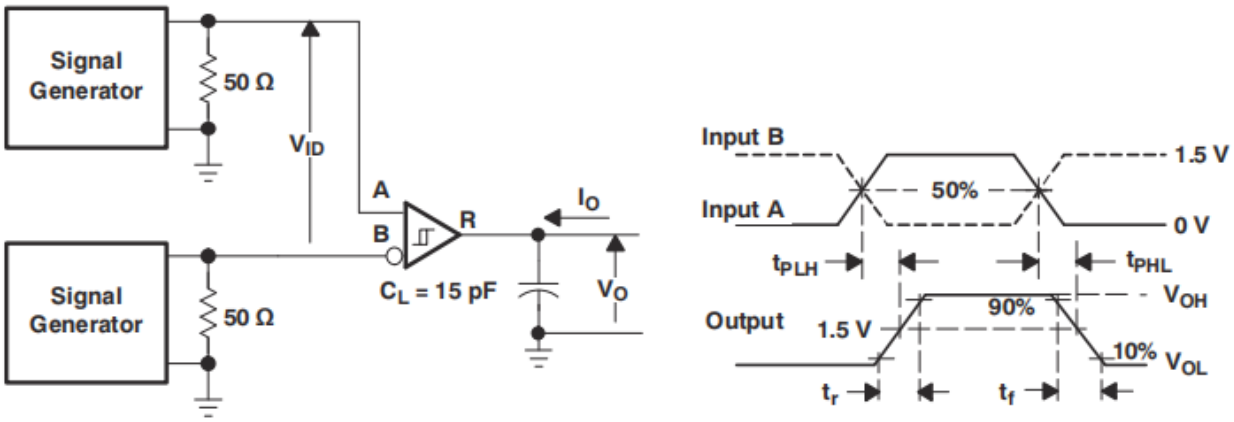


图 8-9. Receiver Switching Test Circuit and Waveforms

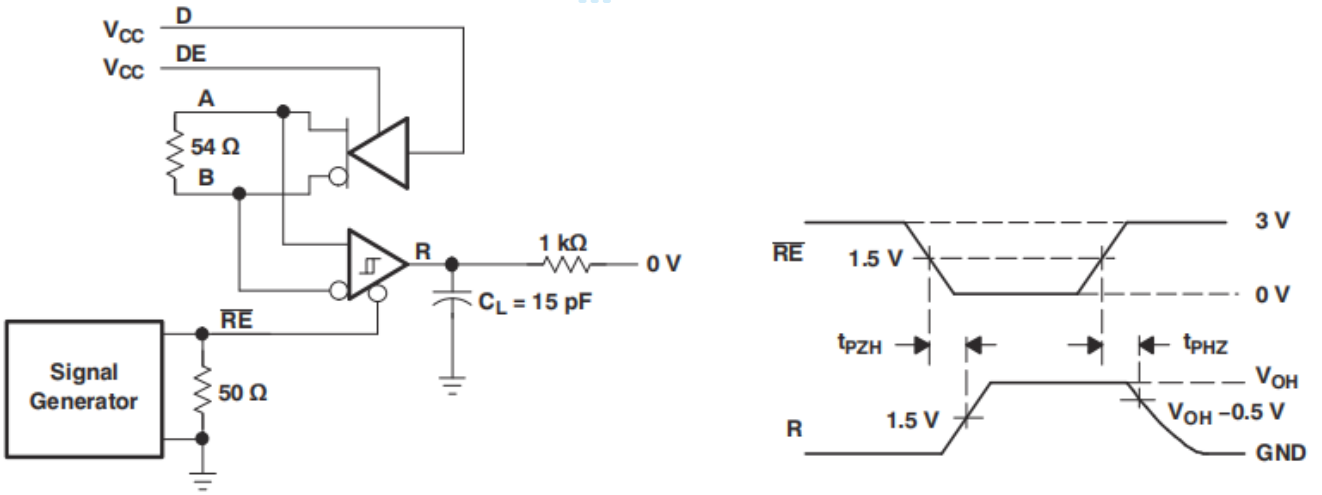


图 8-10. Receiver Enable/Disable Test Circuit and Waveforms, Data Output High

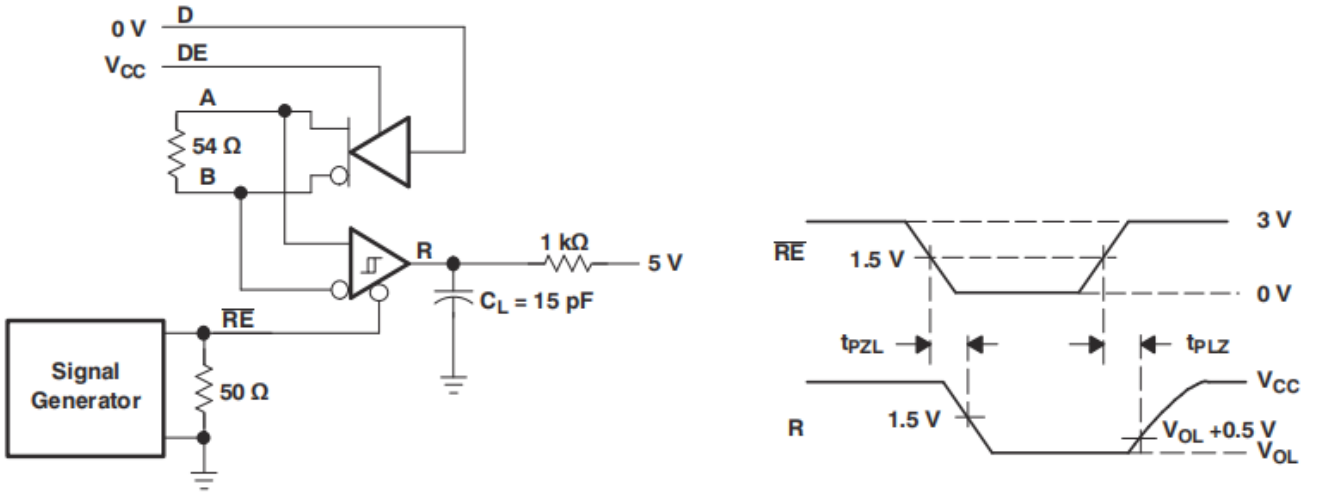


图 8-11. Receiver Enable/Disable Test Circuit and Waveforms, Data Output Low

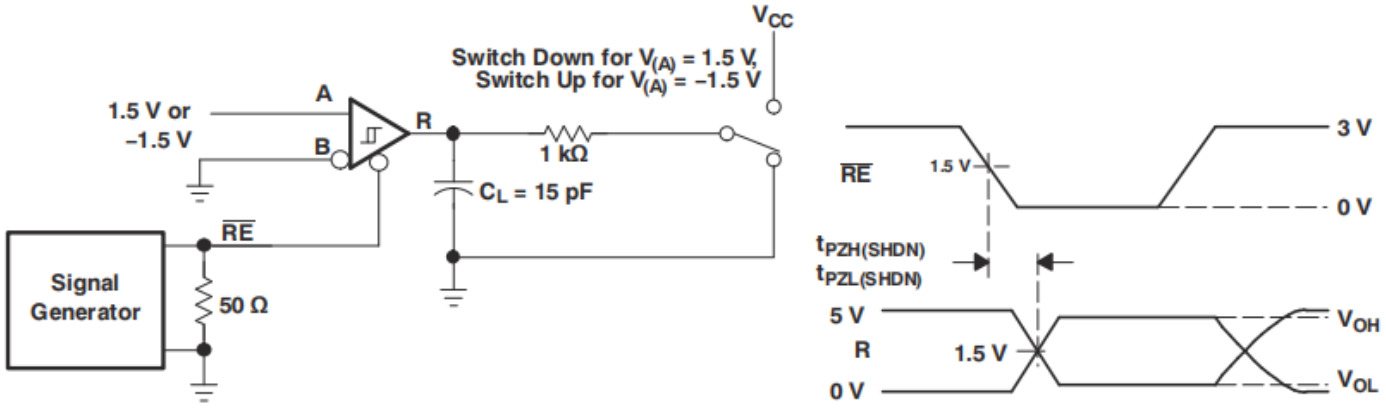


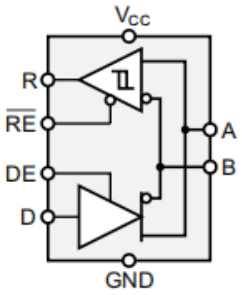
图 8-12. Receiver Enable From Shutdown Test Circuit and Waveforms

8 Detailed Description

8.1 Overview

The SN65HVD485E device is a half-duplex RS-485 transceiver suitable for data transmission at rates up to 10 Mbps over controlled-impedance transmission media (such as twisted-pair cabling). Up to 64 units of the SN65HVD485E device can share a common RS-485 bus due to the low bus-input currents of the device. The device also features a high degree of ESD protection and low standby current consumption of 1 mA (maximum).

8.2 Functional Block Diagram



8.3 Feature Description

The SN65HVD485E device provides internal biasing of the receiver input thresholds for open-circuit, bus-idle, or short-circuit failsafe conditions. It features a typical hysteresis of 30 mV to improve noise immunity. Internal ESD protection circuits protect the transceiver bus terminals against ±15-kV Human Body Model (HBM) electrostatic discharges.

8.4 Device Functional Modes

When the driver enable pin (DE) is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse, B turns high, A is low, and V_{OD} is negative.

When DE is low, both outputs turn high impedance. In this condition, the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground; thus when left open, the driver is disabled (high impedance) by default. The D pin has an internal pullup resistor to VCC; thus when left open while the driver is enabled, output A turns high and B turns low.

表 8-1. Driver Function Table

INPUT D	ENABLE DE	OUTPUTS		FUNCTION
		A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin ($\overline{RE}$) is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold (V_{IT+}) the receiver output (R) turns high. When V_{ID} is negative and lower than the negative input threshold (V_{IT-}), the receiver output (R) turns low. If V_{ID} is between V_{IT+} and V_{IT-}, the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

表 8-2. Receiver Function Table

DIFFERENTIAL INPUT $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R	FUNCTION
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

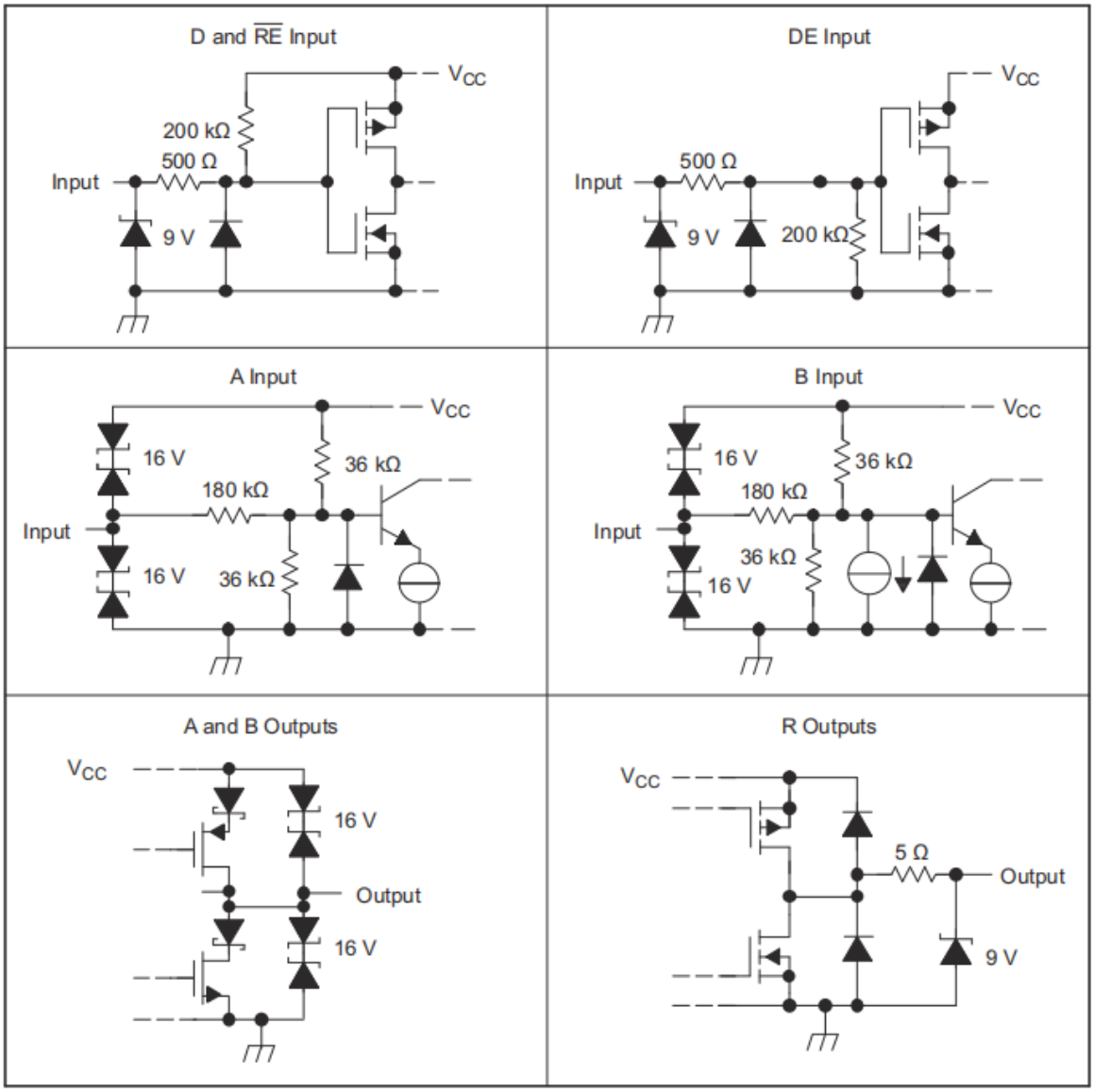


图 8-1. Equivalent Input and Output Schematic Diagrams

9.1 Application Information

The SN65HVD485E device is a half-duplex RS-485 transceiver commonly used for asynchronous data transmissions. The driver and receiver enable pins allow for configuration of different operating modes.

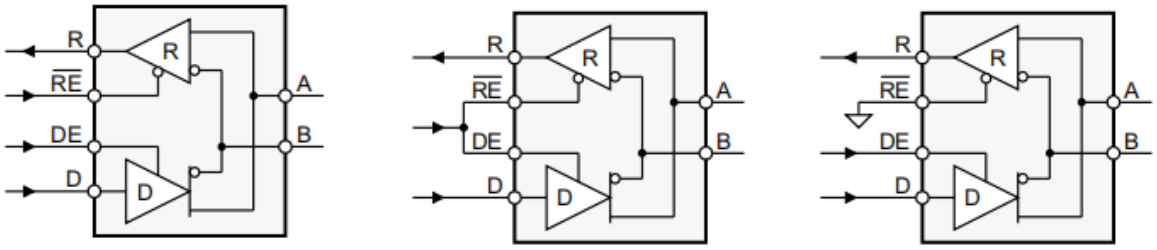


图 9-1. Half-Duplex Transceiver Configurations

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high and as a receiver when the direction-control line is low.

Additionally, only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node receives the data from the bus, receives the data it sends, and can verify that the correct data has been transmitted.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor (R_T) whose value matches the characteristic impedance (Z_0) of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

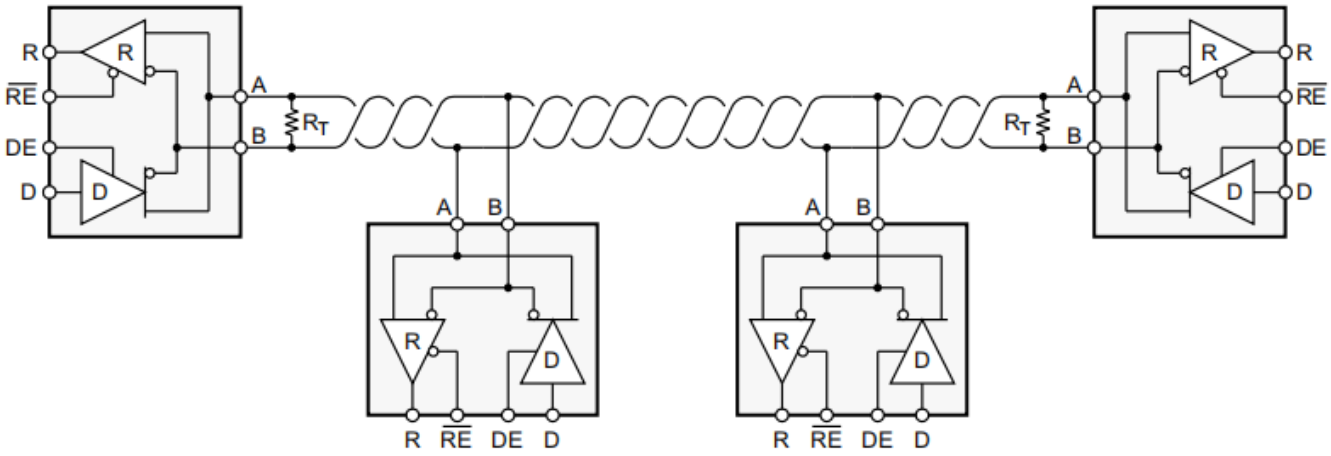


图 9-2. Typical RS-485 Network With Half-Duplex Transceivers

9.2.2 Detailed Design Procedure

To protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary.

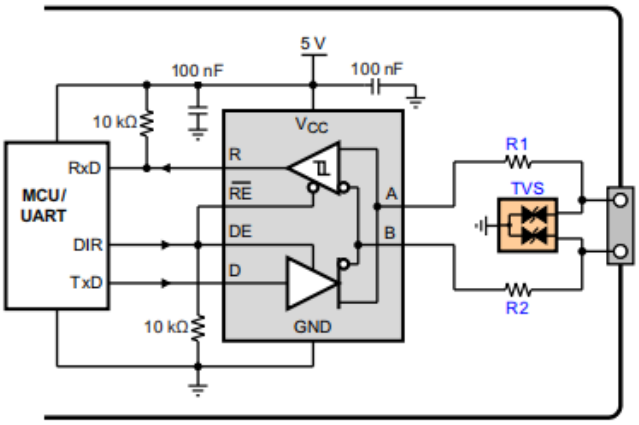


图 9-4. Transient Protection Against ESD, EFT, and Surge Transients

图 9-4 suggests a protection circuit against 10-kV ESD (IEC 61000-4-2), 4-kV EFT (IEC 61000-4-4), and 1-kV surge (IEC 61000-4-5) transients. 表 9-1 shows the associated bill of materials.

表 9-1. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	5-V, 10-Mbps RS-485 transceiver	SN65HVD485E	TI
R1, R2	10-Ω, pulse-proof thick-film resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400-W transient suppressor	CDSOT23-SM712	Bourns

9.2.2.1 Power Usage in an RS-485 Transceiver

Power consumption is a concern in many applications. Power supply current is delivered to the bus load and to the transceiver circuitry. For a typical RS-485 bus configuration, the load that an active driver must drive consists of all of the receiving nodes plus the termination resistors at each end of the bus.

The load presented by the receiving nodes depends on the input impedance of the receiver. The TIA/EIA-485-A standard defines a unit load as allowing up to 1 mA. With up to 32 unit loads allowed on the bus, the total current supplied to all receivers can be as high as 32 mA. The SN65HVD485E device is rated as a ½ unit load device, so up to 64 can be connected on one bus.

The current in the termination resistors depends on the differential bus voltage. The standard requires active drivers to produce at least 1.5 V of differential signal. For a bus terminated with one standard 120-Ω resistor at each end, this sums to 25-mA differential output current whenever the bus is active. Typically, the SN65HVD485E device can drive more than 25 mA to a 60-Ω load, which results in a differential output voltage higher than the minimum required by the standard (see 图 7-2).

Supply current increases with signaling rate primarily because of the totem pole outputs of the driver. When these outputs change state, there is a moment when both the high-side and low-side output transistors are conducting, which creates a short spike in the supply current. As the frequency of state changes increases, more power is used.

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, must be as short as possible. Stubs present a nonterminated piece of bus line that can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub must be less than one-tenth of the rise time of the driver; thus giving a maximum physical stub length as shown in 方程式 1.

$$L_{stub} \leqslant 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- *c* is the speed of light (3×10^8 m/s)
- *v* is the signal velocity of the cable or trace as a factor of *c*

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32-unit loads (UL), where 1-unit load represents a load impedance of approximately 12 kΩ. Because the SN65HVD485E device is a ½ UL transceiver, it is possible to connect up to 64 receivers to the bus.

9.2.1.4 Receiver Failsafe

The differential receiver of the SN65HVD485E device is failsafe to invalid bus states caused by the following:

- Open bus conditions such as a disconnected connector
- Shorted bus conditions such as cable damage shorting the twisted pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic-high state so that the output of the receiver is not indeterminate.

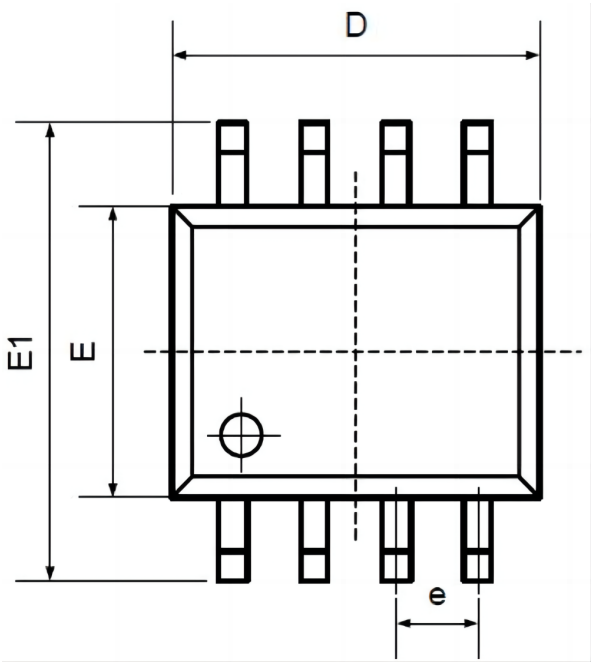
Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and it must output a Low when V_{ID} is more negative than －200 mV. The receiver parameters that determine the failsafe performance are V_{IT+}, V_{IT-}, and V_{hys} (the separation between V_{IT+} and V_{IT-}). As shown in the 节 7.6 table, differential signals more negative than －200 mV cause a low receiver output, and differential signals more positive than 200 mV cause a high receiver output.

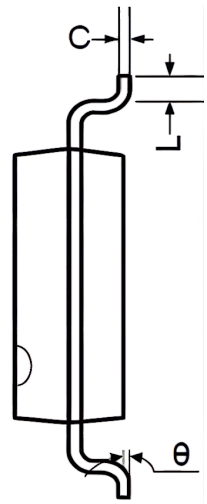
When the differential input signal is close to zero, it is still above the V_{IT+} threshold, and the receiver output is High. Only when the differential input is more than V_{hys} below V_{IT+} does the receiver output transition to a Low state. Therefore, the noise immunity of the receiver inputs during bus fault conditions includes the receiver hysteresis value (V_{hys}) as well as the value of V_{IT+}.

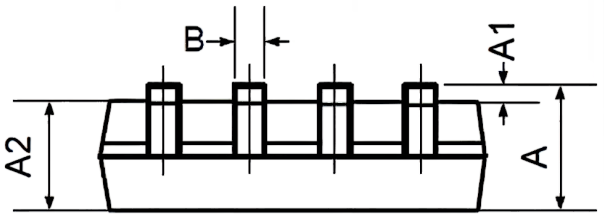
Order information

Order Number	Package	Package Quantity	Marking On The park
SN65HVD485EDGKR-TUDI	MSOP8	Tape,Reel,2500	SN65HVD485EDGKR
SN65HVD485EDR-TUDI	SOP8	Tape,Reel,2500	SN65HVD485EDR

Package SOP8

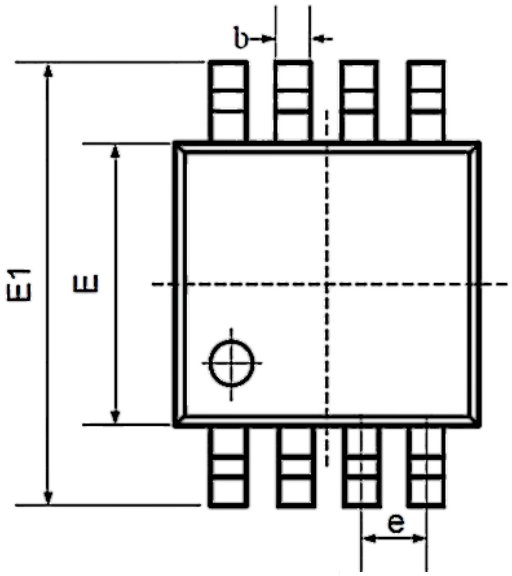


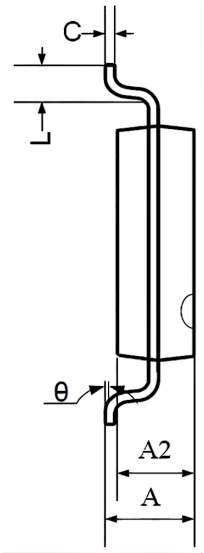


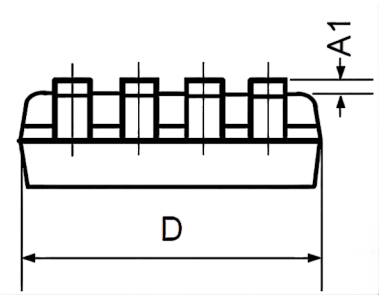


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package MSOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026 TYP	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

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