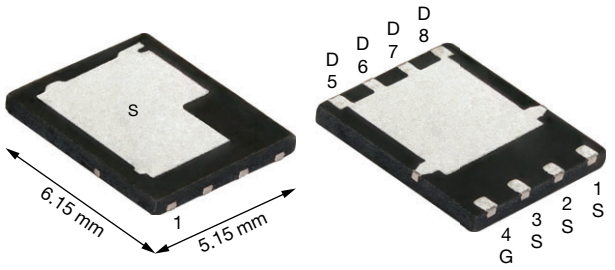
N-Channel 60 V (D-S) 175 °C MOSFET

PowerPAK® SO-8DC



Top View Bottom View

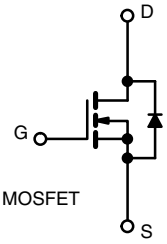
FEATURES

- TrenchFET® Gen IV power MOSFET
- Very low R_{DS} - Q_g figure of merit (FOM)
- Tuned for the lowest R_{DS} - Q_{oss} FOM
- 100 % R_g and UIS tested
- Top side cooling feature provides additional venue for thermal transfer
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Synchronous rectification
- Primary side switch
- DC/DC converter
- Solar micro inverter
- Motor drive switch
- Battery and load switch
- Industrial



N-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	60
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.00174
$R_{DS(on)}$ max. (Ω) at V_{GS} = 7.5 V	0.0021
Q_g typ. (nC)	51
I_D (A) [a]	227
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK® SO-8DC
Lead (Pb)-free and halogen-free	SIDR626EP-T1-RE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	60	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	227	A
	T_C = 70 °C		190	
	T_A = 25 °C		50.8 [b, c]	
	T_A = 70 °C		42.5 [b, c]	
Pulsed drain current (t = 100 µs)		I_{DM}	400	
Continuous source-drain diode current	T_C = 25 °C	I_S	136	
	T_A = 25 °C		6.8 [b, c]	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	50	
Single pulse avalanche energy		E_{AS}	125	mJ
Maximum power dissipation	T_C = 25 °C	P_D	150	W
	T_C = 70 °C		105	
	T_A = 25 °C		7.5 [b, c]	
	T_A = 70 °C		5.25 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) [d, e]			260	

Notes

a. T_C = 25 °C
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8DC is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

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THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction to ambient [a]	t ≤ 10 s	R_{thJA}	15	20	°C/W
Maximum junction to case (drain)	Steady state	R_{thJC}	0.8	1	
Maximum junction to case (source)	Steady state	R_{thJC}	1.1	1.4	

Notes

a. Surface mounted on 1" x 1" FR4 board

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	60	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = 10 mA	-	33	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 µA	-	-8.8	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2	-	4	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	-	-	100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 70 °C	-	-	15	
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A	-	0.00145	0.00174	Ω
		V_{GS} = 7.5 V, I_D = 20 A	-	0.00175	0.0021	
Forward transconductance [a]	g_{fs}	V_{DS} = 15 V, I_D = 20 A	-	78	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = 30 V, V_{GS} = 0 V, f = 1 MHz	-	5130	-	pF
Output capacitance	C_{oss}		-	1190	-	
Reverse transfer capacitance	C_{rss}		-	39	-	
Total gate charge	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 20 A	-	68	102	nC
		V_{DS} = 30 V, V_{GS} = 7.5 V, I_D = 20 A	-	51	77	
Gate-source charge	Q_{gs}		-	25	-	
Gate-drain charge	Q_{gd}		-	7.4	-	
Output charge	Q_{oss}	V_{DS} = 30 V, V_{GS} = 0 V	-	71	-	
Gate resistance	R_g	f = 1 MHz	0.2	0.62	1.1	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 1.5 Ω, $I_D \cong$ 20 A, V_{GEN} = 10 V, R_g = 1 Ω	-	20	40	ns
Rise time	t_r		-	10	20	
Turn-off delay time	$t_{d(off)}$		-	35	70	
Fall time	t_f		-	7	14	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 1.5 Ω, $I_D \cong$ 20 A, V_{GEN} = 7.5 V, R_g = 1 Ω	-	24	48	
Rise time	t_r		-	25	50	
Turn-off delay time	$t_{d(off)}$		-	30	60	
Fall time	t_f		-	10	20	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25 °C	-	-	136	A
Pulse diode forward current	I_{SM}		-	-	400	
Body diode voltage	V_{SD}	I_S = 5 A, V_{GS} = 0 V	-	0.74	1.1	V
Body diode reverse recovery time	t_{rr}	I_F = 20 A, di/dt = 100 A/µs, T_J = 25 °C	-	45	90	ns
Body diode reverse recovery charge	Q_{rr}		-	45	90	nC
Reverse recovery fall time	t_a		-	21	-	ns
Reverse recovery rise time	t_b		-	24	-	

Notes

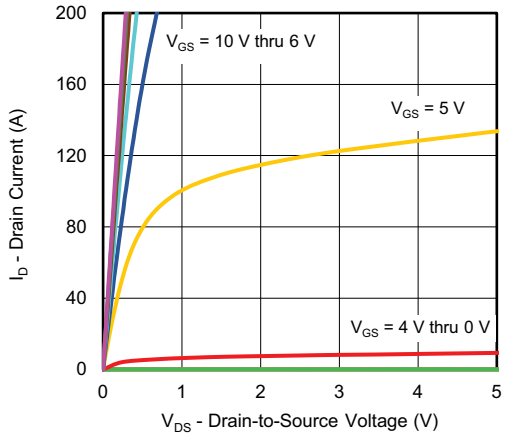
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing

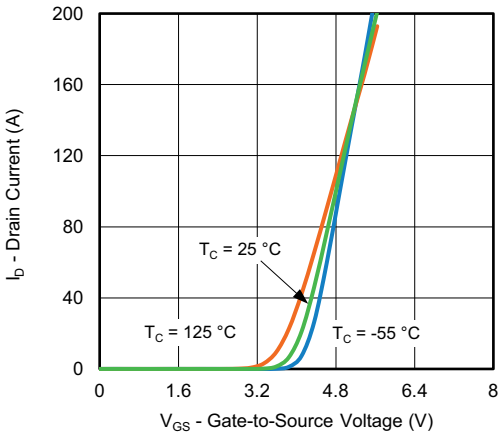
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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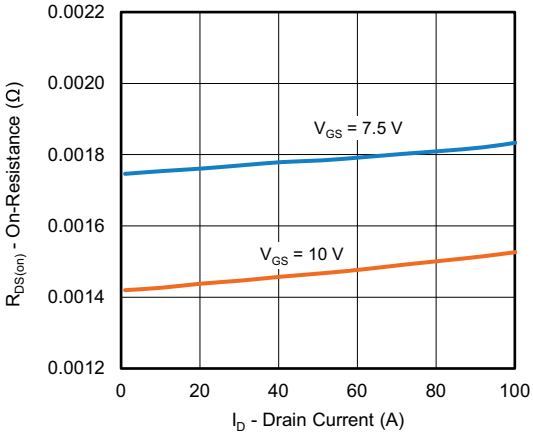
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



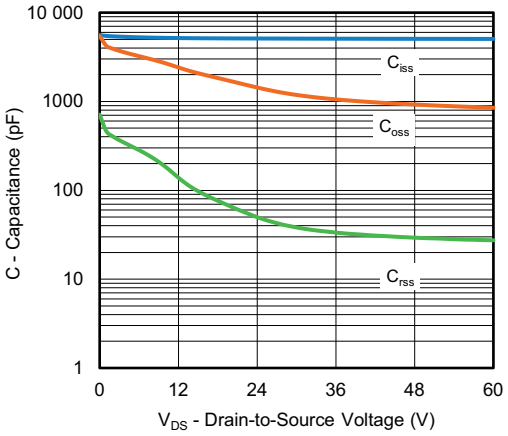
Output Characteristics



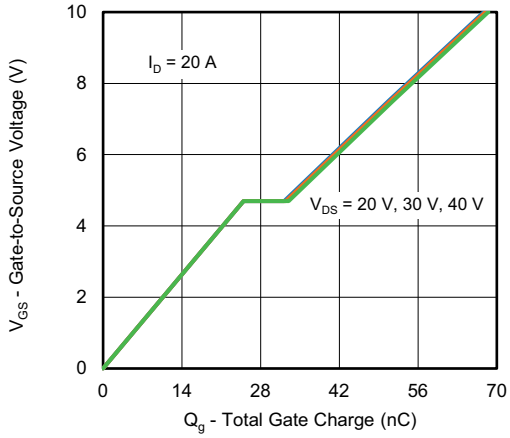
Transfer Characteristics



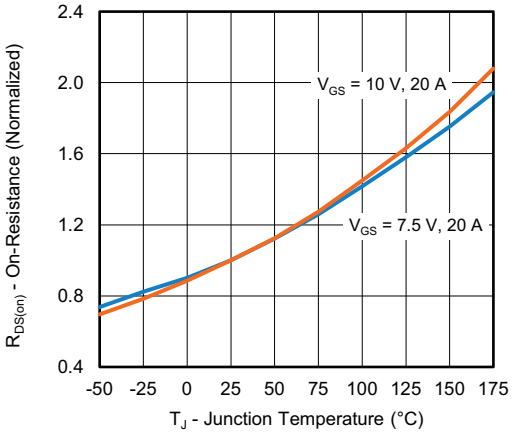
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



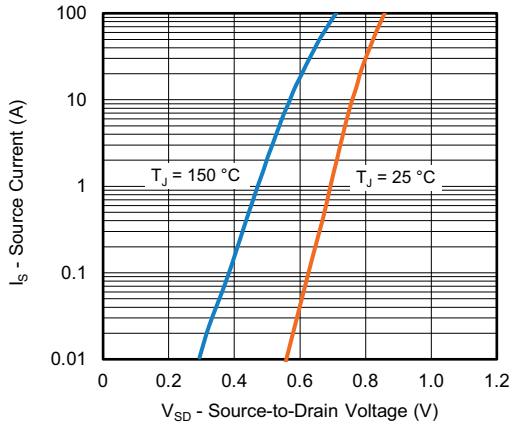
Gate Charge



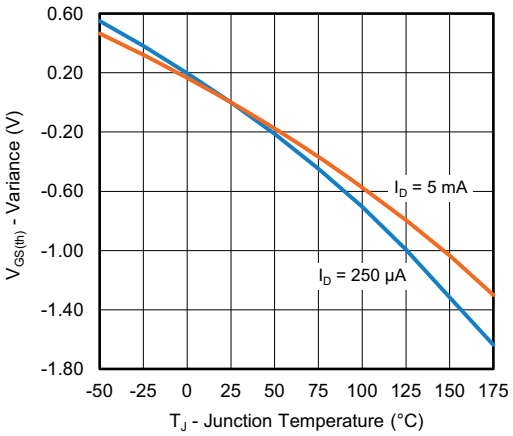
On-Resistance vs. Junction Temperature

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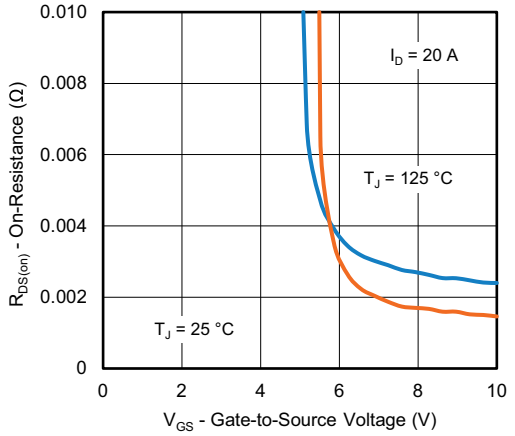
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



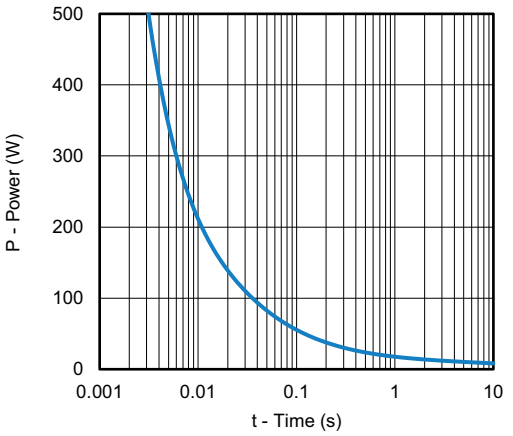
Source-Drain Diode Forward Voltage



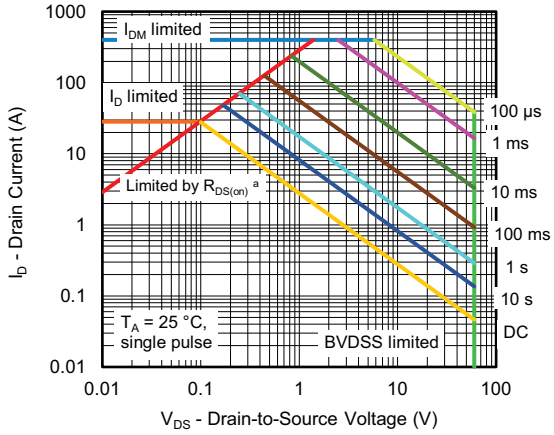
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



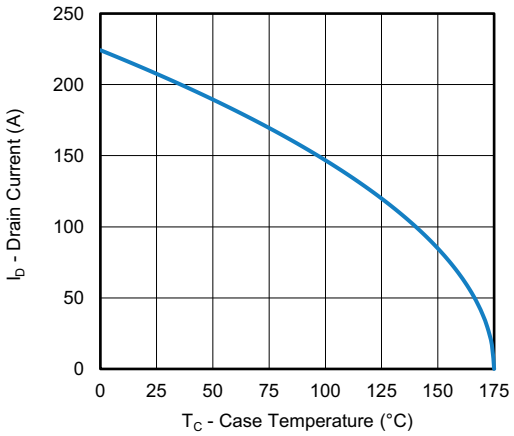
Safe Operating Area, Junction-to-Ambient

Note

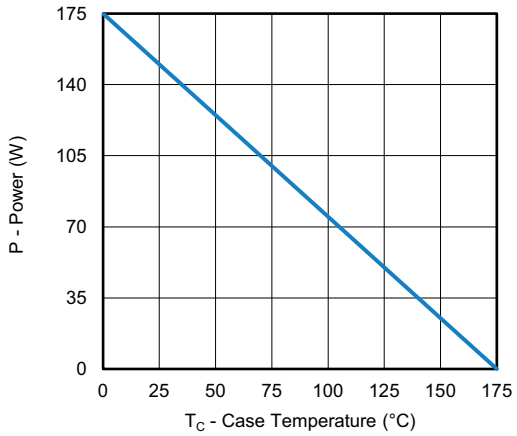
a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

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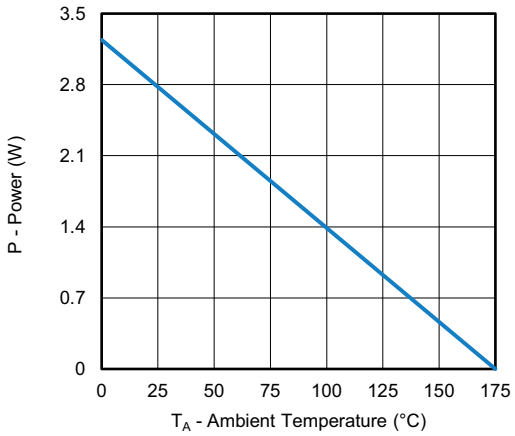
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]



Power, Junction-to-Case



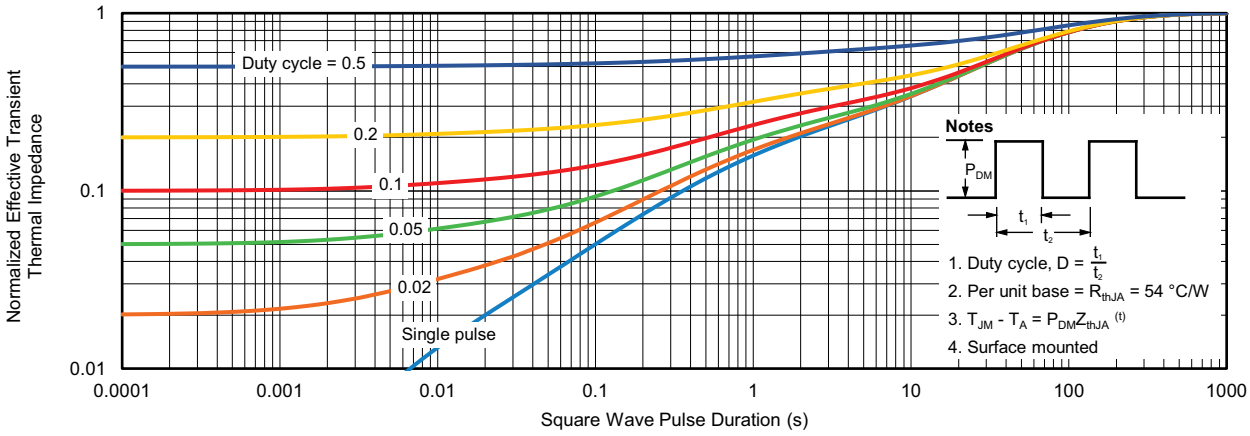
Power, Junction-to-Ambient

Note

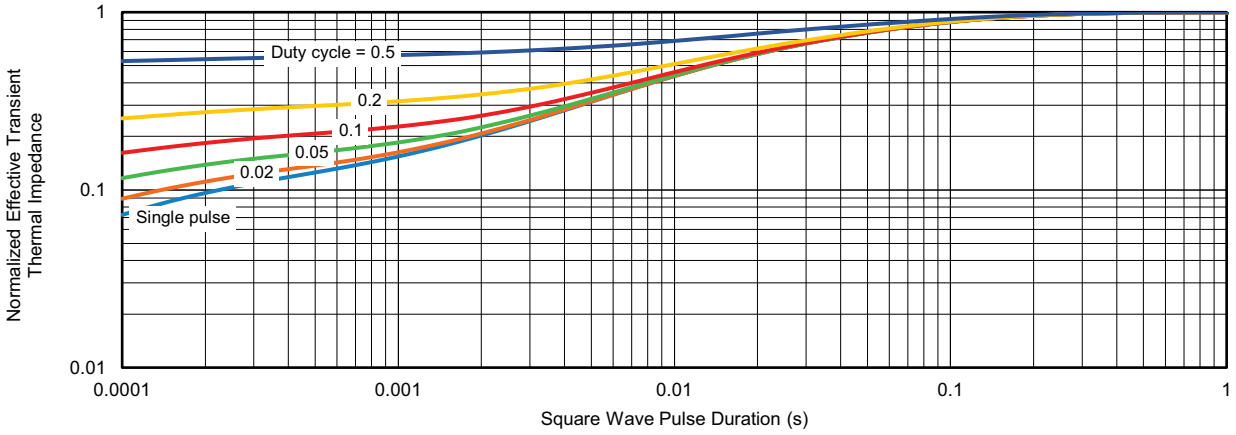
a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



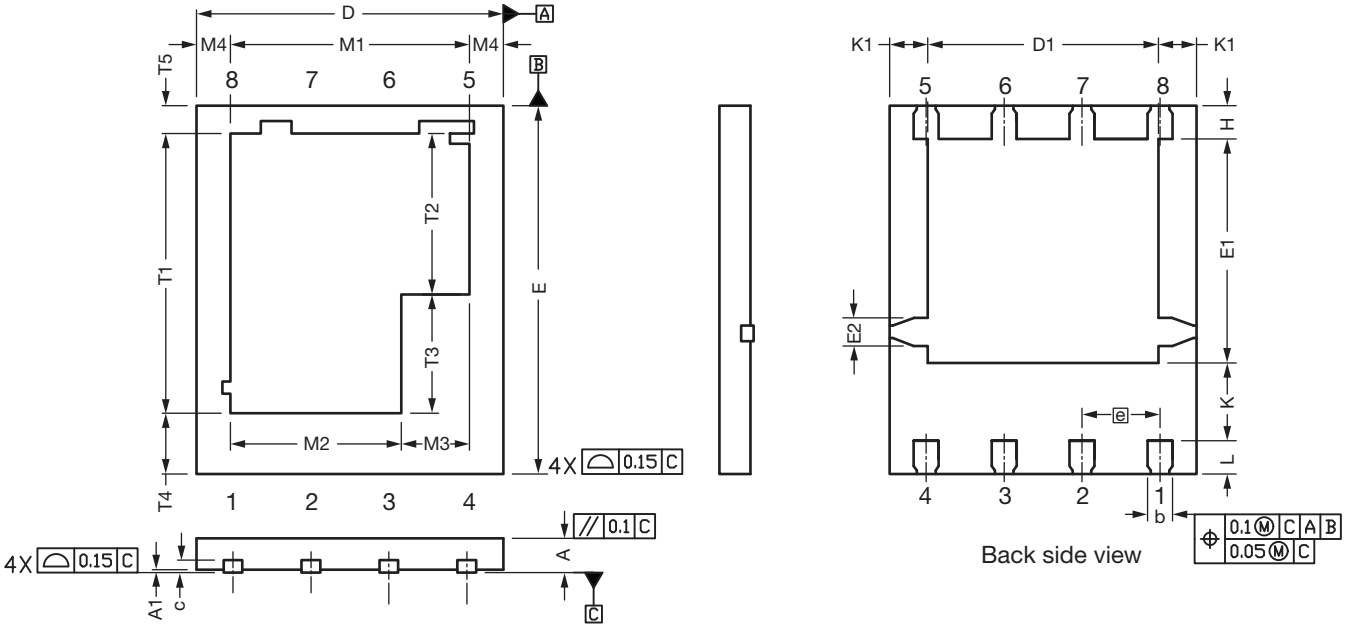
Normalized Thermal Transient Impedance, Junction-to-Case

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PowerPAK® SO-8 Double Cooling Case Outline

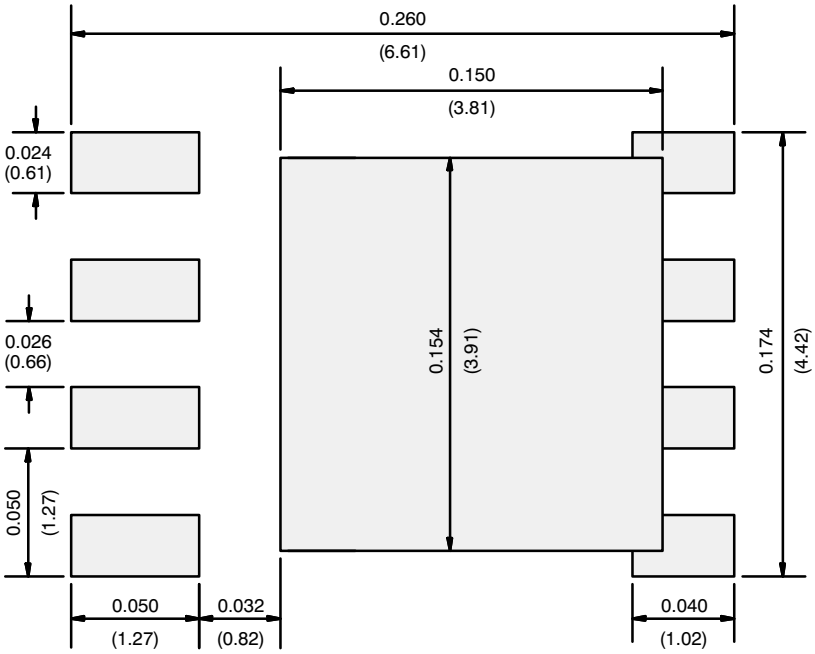


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.51	0.56	0.61	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.36	0.41	0.46	0.014	0.016	0.018
c	0.15	0.20	0.25	0.006	0.008	0.010
D	4.90	5.00	5.10	0.193	0.197	0.201
D1	3.71	3.76	3.81	0.146	0.148	0.150
e		1.27 BSC			0.050 BSC	
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	3.60	3.65	3.70	0.142	0.144	0.146
E2		0.46 typ.			0.018 typ.	
H	0.49	0.54	0.59	0.019	0.021	0.023
K	1.22	1.27	1.32	0.048	0.050	0.052
K1		0.64 typ.			0.025 typ.	
L	0.49	0.54	0.59	0.019	0.021	0.023
M1	3.8	3.90	4.00	0.150	0.154	0.158
M2	2.69	2.79	2.89	0.106	0.110	0.114
M3	1.01	1.11	1.21	0.040	0.044	0.048
M4		0.56 typ.			0.022 typ.	
N		8			8	
T1	4.46	4.56	4.66	0.176	0.180	0.184
T2	2.53	2.63	2.73	0.100	0.104	0.108
T3	1.83	1.93	2.03	0.072	0.076	0.080
T4		0.97 typ.			0.038 typ.	
T5		0.48 typ.			0.019 typ.	
ECN: T24-0304-Rev. C, 29-Jul-2024 DWG: 6048						

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RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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APPLICATION NOTE

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WSL2512R0300FTB WSL27265L000FEB ISOA200R11003JT RS0105R000FE12 SE20DLGHM3/I
SQD50P08-28_GE3 SUD50P04-08-GE3 1.5SMC91A-E3/57T CRCW2512150RFKEGHP
PR02000204709JA100 PTCCL05H280HTE CRCW08051M00FKEA ILHB1806ER600V
PR01000101603JR500 VS-50RIA60 LTO150H470R0JTE3 PR03000204700JAC00 SM8S43AHE3_A/I
SS2FN6HM3/H BRT13-H-X006 293D337X96R3D2T-E3 CCF5510K0FKE36 CRCW040213K0FKTD
MSS2P3-M3/89A RCL12183R30FKEK