

钍地半导体
Tudi Semiconductor

# Product Specification

## TUDI- SN65HVD08/SN75HVD08

Wide supply voltage range RS-485 transceiver

网址 www.sztdbdt.com

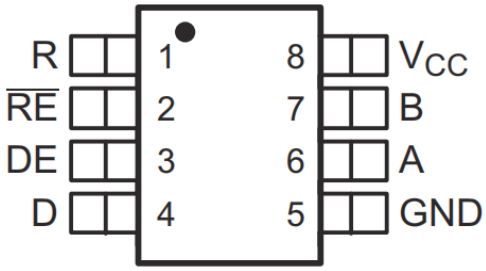
**用芯智造·卓越品质**

**semiconductor device manufacturer**

- Design
- research and development
- production
- and sales

## Features

- Powered by 3V to 5.5V supply
- Static power dissipation less than 90mW
- Fail-safe for open, short, and bus idle conditions
- 1/8 unit load (up to 256 nodes on the bus)
- Bus pin ESD protection exceeds 16kV H
- Limits driver output voltage slew rate at 10Mbps for excellent signal quality
- Electrical characteristics comply with ANSI TIA/EIA-485




D or P Package, 8-Pin SOIC or PDIP
(Top View)

## Applications

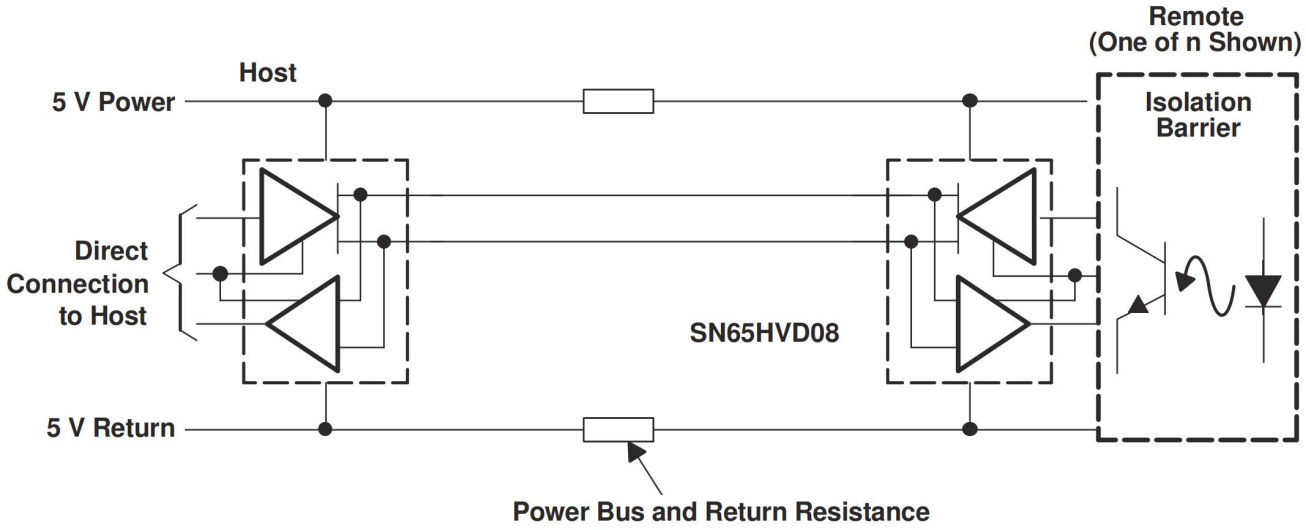
- Data transmission with host-powered remote sites
- Isolated multi-point data bus
- Industrial process control networks
- Point-of-sale
- Electric metering

## Description

The SN65HVD08 combines a three-state differential line driver and a differential line receiver to enable balanced data transmission andability with devices compliant with ANSI TIA/EIA-485-A and ISO-8482E standards.

The SN65HVD08 features wide supply voltage range and low static current requirements, allowing it to be powered by a 5V power bus in the cable and tolerate up to a 2V line voltage drop The bus power in the cable can reduce the need to generate isolated power at each connection on a ground-isolated bus.

The driver's differential outputs and the receiver's differential are internally connected to form a differential input/output (I/O) bus port, which provides a minimum load to the bus when the driver is disabled or unpowered. The and receiver have active-high and active-low enable pins, respectively, which can be externally connected to serve as direction control.




典型应用原理图

表 **5-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| A | 6 | Bus input / output | Driver output and receiver input (complementary to B) |
| B | 7 | Bus input / output | Driver output and receiver input (complementary to A) |
| D | 4 | Digital input | Driver data input |
| DE | 3 | Digital input | Driver enable high |
| GND | 5 | Reference potential | Local device ground |
| R | 1 | Digital output | Receive data output |
| $\overline{RE}$ | 2 | Digital input | Receiver enable low |
| $V_{CC}$ | 8 | Supply | 3-V to 5.5-V supply |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1) (2)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage, $V_{CC}$ | - 0.3 | 6 | V |
| Voltage at A or B | - 9 | 14 | V |
| Input voltage at D, DE, R or $\overline{RE}$ | - 0.5 | $V_{CC}$ + 0.5 | V |
| Voltage input, transient pulse, A and B, through 100 Ω | - 25 | 25 | V |
| Receiver output current, $I_O$ | - 11 | 11 | mA |
| Maximum Junction Temperature, $T_J$ | | 150 | °C |
| Storage Temperature, $T_{STG}$ | - 65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | A, B, and GND | 16000 | V |
| | | All pins | 4000 | |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | | 1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 3 | | 5.5 | V |
| Input voltage at any bus terminal (separately or common mode), $V_I$ (1) | | - 7 | | 12 | V |
| High-level input voltage, $V_{IH}$ | Driver, driver enable, and receiver enable inputs | 2.25 | | $V_{CC}$ | V |
| Low-level input voltage, $V_{IL}$ | | 0 | | 0.8 | |
| Differential input voltage, $V_{ID}$ | | - 12 | | 12 | |
| High-level output current, $I_{OH}$ | Driver | - 60 | | | mA |
| | Receiver | - 8 | | | |
| Low-level output current, $I_{OL}$ | Driver | | | 60 | mA |
| | Receiver | | | 8 | |
| Operating free-air temperature, $T_A$ | SN75HVD08 | 0 | | 70 | °C |
| | SN65HVD08 | - 40 | | 85 | |

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | D (SOIC) SN75 Version | D (SOIC) SN65 Version | P (PDIP) | UNIT |
|---|---|---|---|---|---|
| | | 8 PINS | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 175.4 | 116.7 | 125 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 53.6 | 56.3 | 34.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 45.1 | 63.4 | 23.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 10.1 | 8.8 | 12.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 44.4 | 62.6 | 23.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

over recommended operating conditions unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\lvert V_{OD}\rvert$ | Driver differential output voltage magnitude | $R_L$= 60 Ω, 375 Ω on each output to -7 V to 12 V, See 图 7-1 | 1.5 | | $V_{CC}$ | V |
| $\Delta\lvert V_{OD}\rvert$ | Change in magnitude of driver differential output voltage | $R_L$= 54 Ω | - 0.2 | | 0.2 | V |
| $V_{OC(PP)}$ | Peak-to-peak driver common-mode output voltage | Center of two 27-Ω load resistors, See 图 7-2 | | 0.5 | | V |
| $V_{IT+}$ | Positive-going receiver differential input voltage threshold | | | | - 10 | mV |
| $V_{IT-}$ | Negative-going receiver differential input voltage threshold | | - 200 | | | mV |
| $V_{hys}$ | Receiver differential input voltage threshold hysteresis($V_{IT+}$ - $V_{IT-}$) | | | 35 | | mV |
| $V_{OH}$ | Receiver high-level output voltage | $I_{OH}$ = -8 mA | 2.4 | | | V |
| $V_{OL}$ | Receiver low-level output voltage | $I_{OL}$ = 8 mA | | | 0.4 | V |
| $I_{IH}$ | Driver input, driver enable, and receiver enable high-level input current | | - 100 | | 100 | μA |
| $I_{IL}$ | Driver input, driver enable, and receiver enable low-level input current | | - 100 | | 100 | μA |

## 6.5 Electrical Characteristics (continued)

over recommended operating conditions unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{OS}$ | Driver short-circuit output current | 7 V < $V_O$ < 12 V | - 265 | | 265 | mA |
| $I_I$ | Bus input current (disabled driver) | $V_I$ = 12 V | | | 130 | μA |
| | | $V_I$ = -7 V | - 100 | | | |
| | | $V_I$ = 12 V, $V_{CC}$ = 0 V | | | 130 | |
| | | $V_I$ = -7 V. $V_{CC}$ = 0 V | - 100 | | | |
| $I_{CC}$ | Supply current | Receiver enabled, driver disabled, no load | | | 10 | mA |
| | | Driver enabled, receiver disabled, no load | | | 16 | |
| | | Both disabled | | | 5 | μA |
| | | Both enabled, no load | | | 16 | mA |

## 6.6 Driver Switching Characteristics

over recommended operating conditions unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PHL}$ | Driver high-to-low propagation delay time | $R_L$ = 54 Ω, $C_L$ = 50 pF,See 图 7-3 | 18 | | 40 | ns |
| $t_{PLH}$ | Driver low-to-high propagation delay time | | 18 | | 40 | |
| $t_r$ | Driver 10%-to-90% differential output rise time | | 10 | | 55 | |
| $t_f$ | Driver 90%-to-10% differential output fall time | | 10 | | 55 | |
| $t_{SK(P)}$ | Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$ | | | | 2.5 | |
| $t_{en}$ | Driver enable time | Receiver enabled, See Figures 4 and 5 | | | 55 | ns |
| | | Receiver disabled, See Figures 4 and 5 | | | 6 | μs |
| $t_{dis}$ | Driver disable time | Receiver enabled, See Figures 4 and 5 | | | 90 | ns |

## 6.7 Receiver Switching Characteristics

over recommended operating conditions unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PHL}$ | Receiver high-to-low propagation delay time | $C_L$ = 15 pF, See 图 7-6 | | | 70 | ns |
| $t_{PLH}$ | Receiver low-to-high propagation delay time | | | | 70 | |
| $t_r$ | Receiver 10%-to-90% differential output rise time | | | | 5 | |
| $t_f$ | Receiver 90%-to-10% differential output fall time | | | | 5 | |
| $t_{SK(P)}$ | Receiver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$ | | | | 4.5 | |
| $t_{en}$ | Receiver enable time | Driver enabled, See 图 7-7 | | | 15 | ns |
| | | Driver disabled, See 图 7-8 | | | 6 | μs |
| $t_{dis}$ | Receiver disable time | Driver enabled, See 图 7-7 | | | 20 | ns |

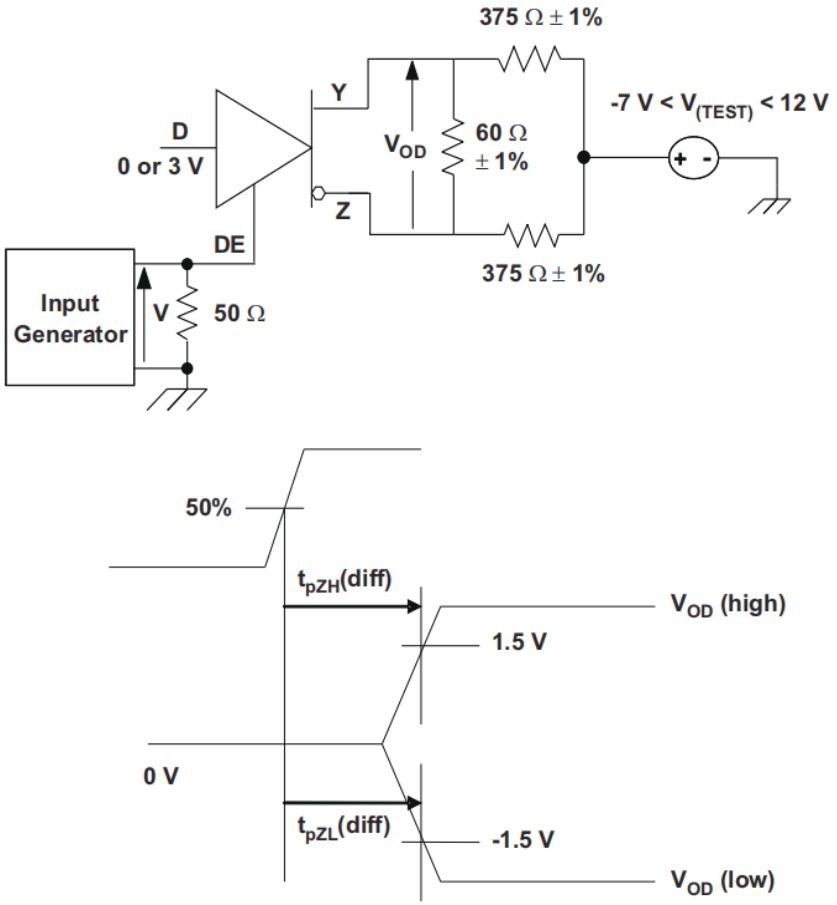



**图 6-1. Driver Enable Time From DE to $V_{OD}$**

The time $t_{pZL}(x)$ is the measure from DE to $V_{OD}(x)$. $V_{OD}$ is valid when it is greater than 1.5 V.

## 7 Parameter Measurement Information

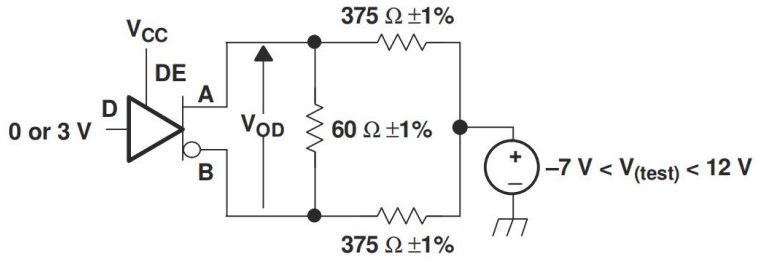
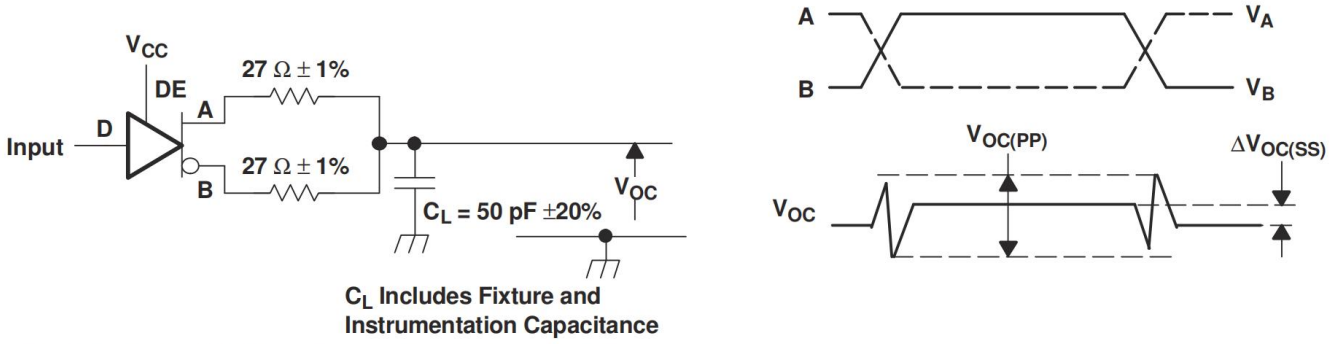
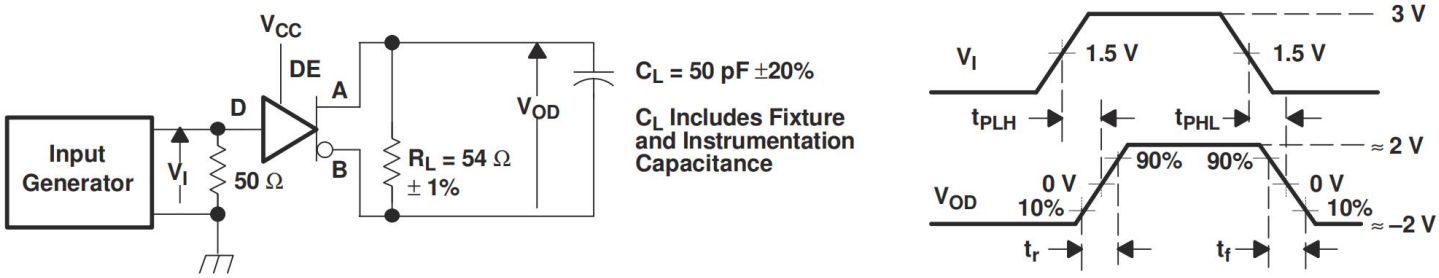



图 7-1. Driver $V_{OD}$ With Common-Mode Loading Test Circuit



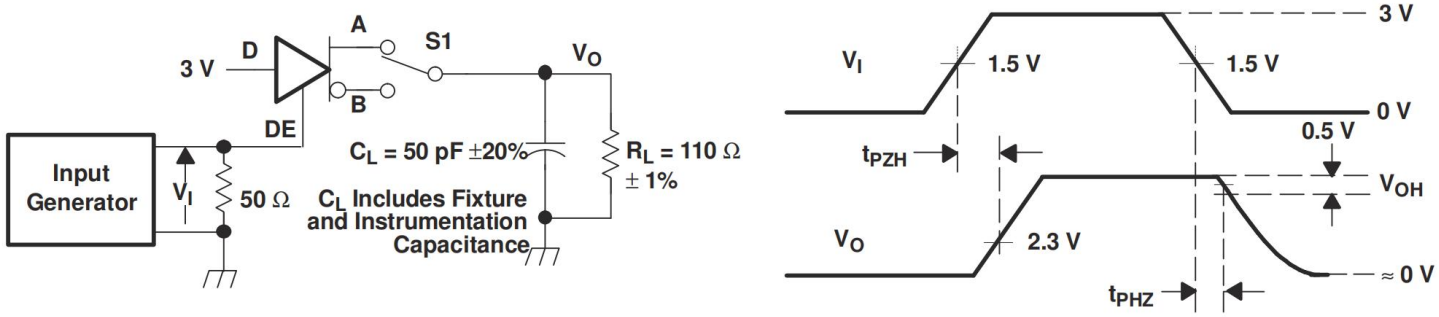

Input: PRR = 500 kHz, 50% Duty Cycle,$t_r$<6ns, $t_f$<6ns, $Z_O$ = 50 Ω

图 7-2. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



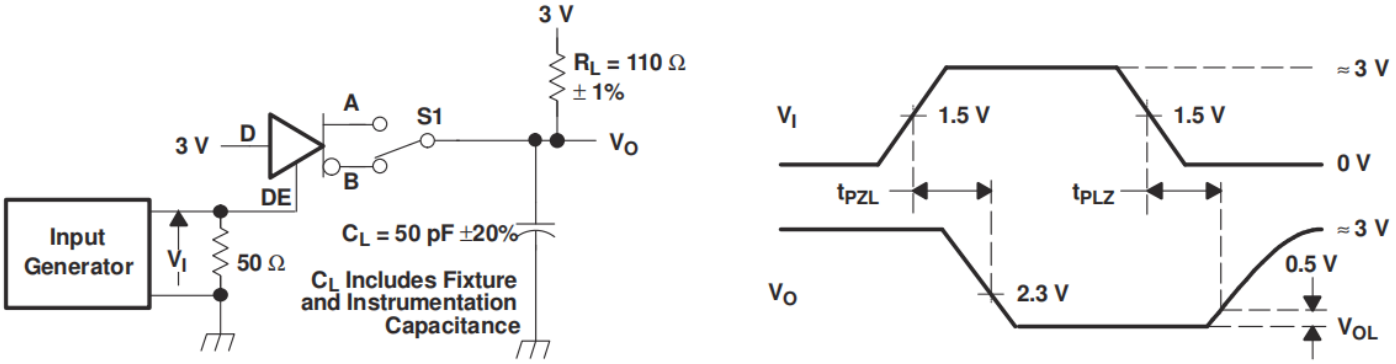

Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r$ <6 ns, $t_f$ <6 ns, $Z_o$ = 50 Ω

图 7-3. Driver Switching Test Circuit and Voltage Waveforms



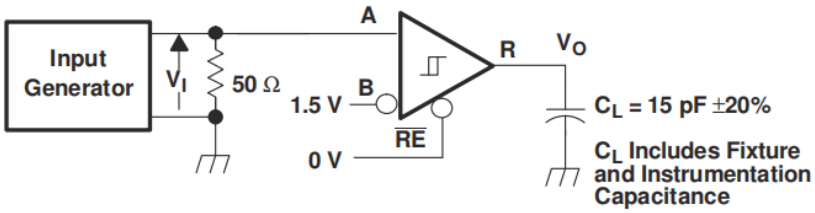

Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r$ <6 ns, $t_f$ <6 ns, $Z_o$ = 50 Ω

图 7-4. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms




Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r$ <6 ns, $t_f$ <6 ns, $Z_o$ = 50 Ω

图 7-5. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms




Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r$ <6 ns, $t_f$ <6 ns, $Z_o$ = 50 Ω

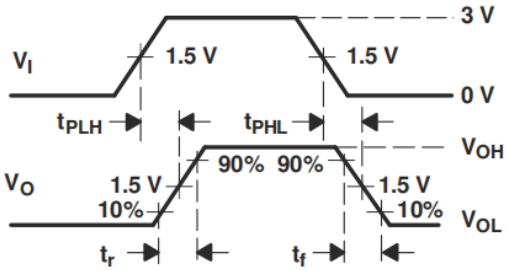
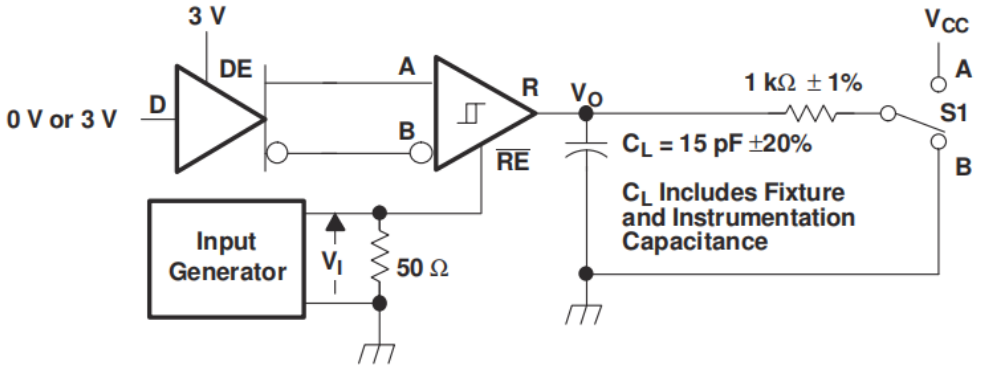



图 7-6. Receiver Switching Test Circuit and Voltage Waveforms




Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r$ <6 ns, $t_f$ <6 ns, $Z_o$ = 50 Ω

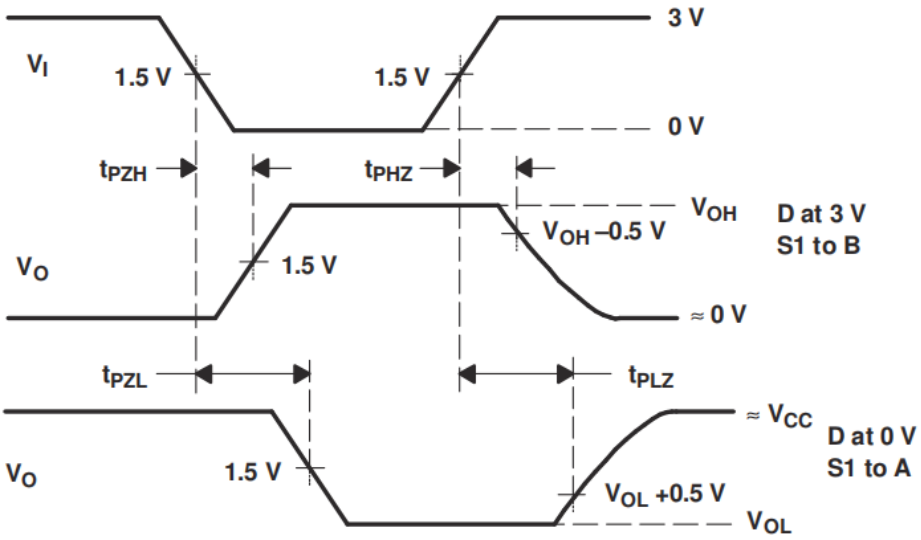
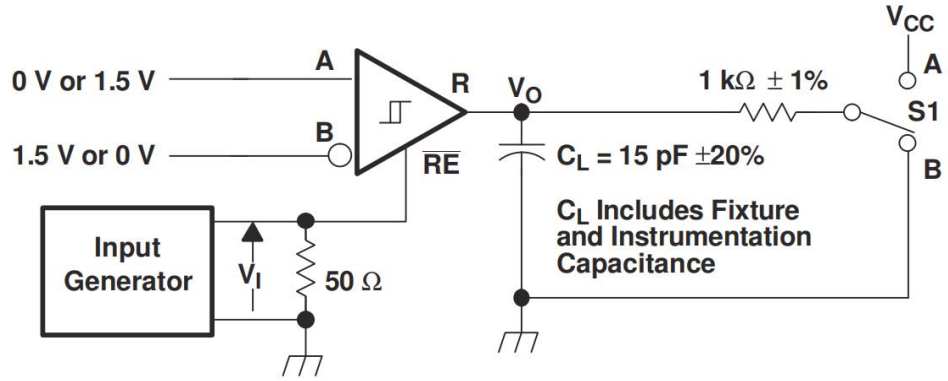



**图 7-7. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled**




Generator: PRR = 100 kHz, 50% Duty Cycle, $t_r$ <6 ns, $t_f$ <6 ns, $Z_o$ = 50 Ω

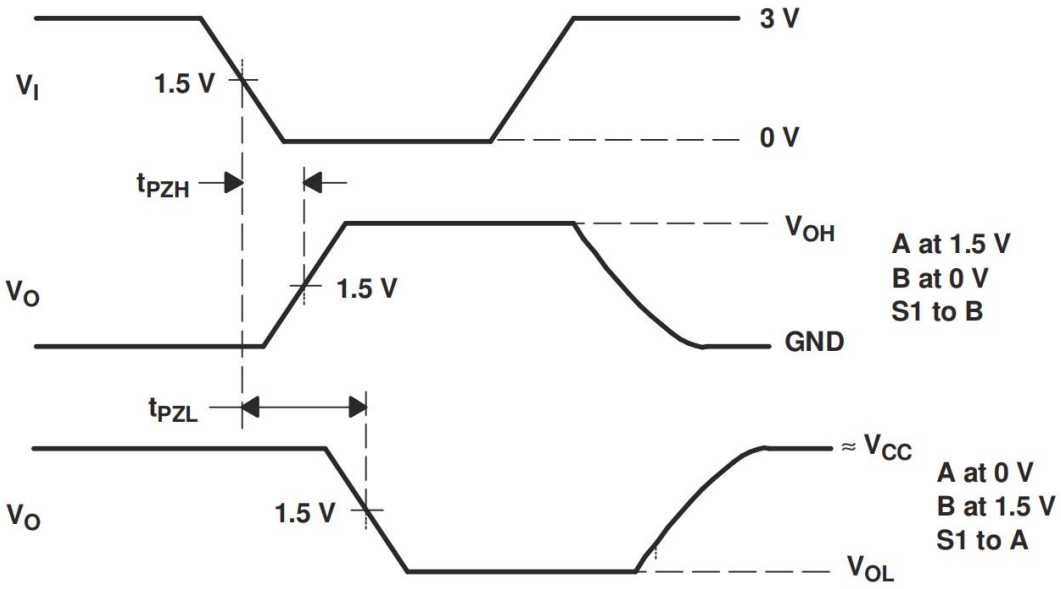



图 7-8. Receiver Enable Time From Standby (Driver Disabled)

# 8 Detailed Description

## 8.1 Overview

The SNx5HVD08 is a 3-V to 5.5-V, half-duplex, RS-485 transceiver suitable for data transmission up to 10 Mbps.

This device has an active-high driver enable and active-low receiver enable. A standby current of less than 5 µA can be achieved by disabling both driver and receiver.

Device operation is specified over a wide temperature range from -40°C to +85°C.

## 8.2 Functional Block Diagram

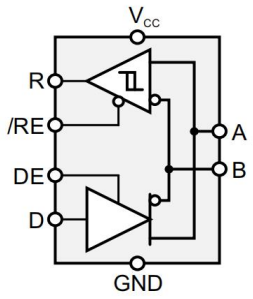



图 **8-1. Logic Diagram (Positive)**

## 8.3 Feature Description

Internal ESD protection circuits protect the transceiver bus terminals against ±16 kV Human Body Model (HBM) electrostatic discharges and all other pins up to ±4 kV.

The SNx5HVD08 provides internal biasing of the receiver input thresholds for open-circuit, bus-idle, or short-circuit failsafe conditions, and a typical receiver hysteresis of 35 mV.

## 8.4 Device Functional Modes

表 **8-1. Function Table: Driver**

| INPUT | ENABLE | OUTPUTS | |
|---|---|---|---|
| D | DE | A | B |
| H | H | H | L |
| L | H | L | H |
| X | L | Z | Z |
| Open | H | H | L |

表 **8-2. Function Table: Receiver**

| DIFFERENTIAL INPUTS | ENABLE(1) | OUTPUT(1) |
|---|---|---|
| $V_{ID} = V_A - V_B$ | $\overline{RE}$ | R |
| $V_{ID} \leq$ -0.2 V | L | L |
| -0.2 V < $V_{ID}$ < -0.01 V | L | ? |
| -0.01 V $\leq V_{ID}$ | L | H |
| X | H | Z |
| Open Circuit | L | H |
| Short Circuit | L | H |

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

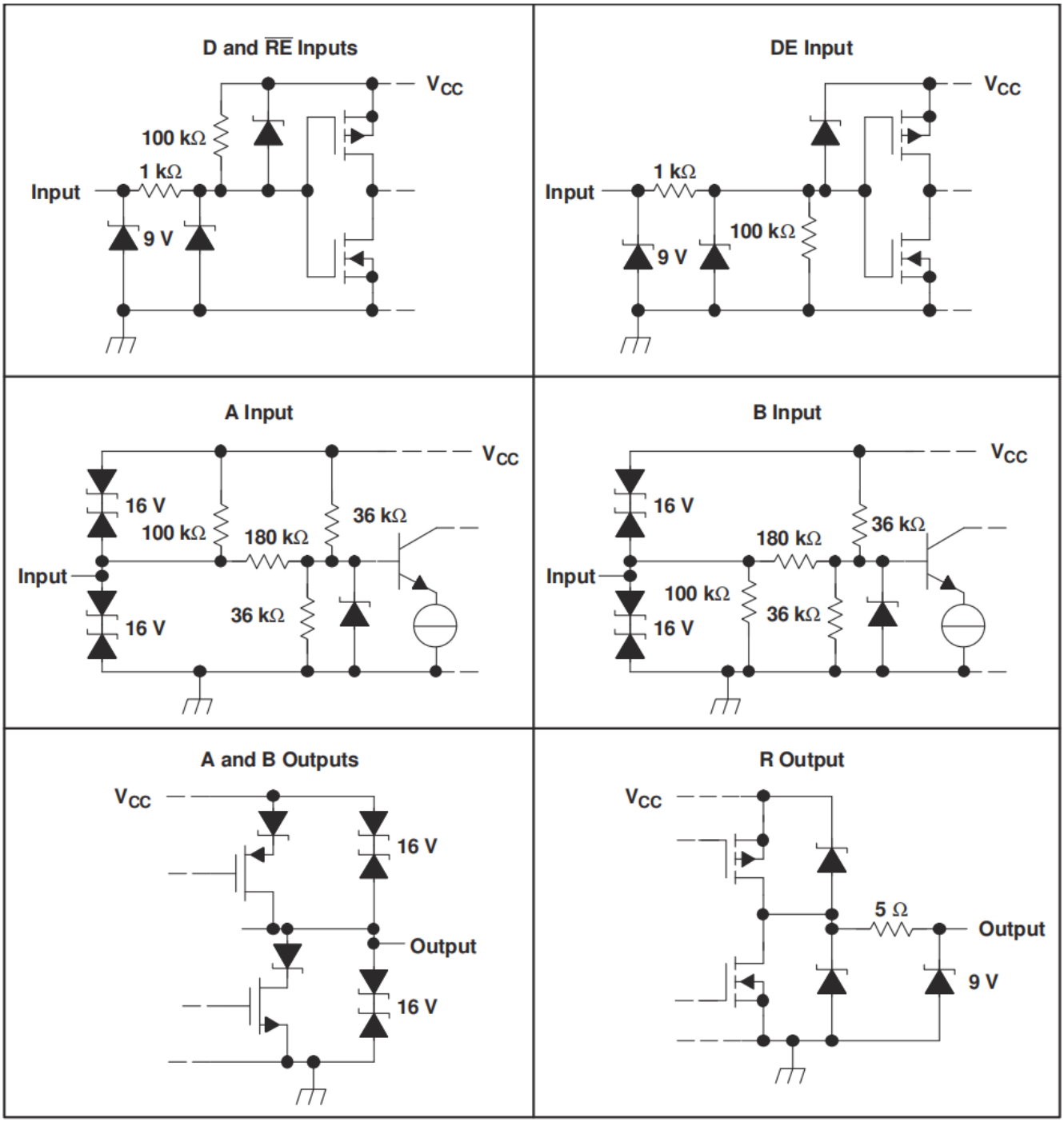



图 8-2. Equivalent Input and Output Schematic Diagrams

## 9.1 Application Information

As electrical loads are physically distanced from their power source, the effects of supply and return line impedance and the resultant voltage drop must be accounted. If the supply regulation at the load cannot be maintained to the circuit requirements, it forces the use of remote sensing, additional regulation at the load, bigger or shorter cables, or a combination of these. The SN65HVD08 eases this problem by relaxing the supply requirements to allow for more variation in the supply voltage over typical RS-485 transceivers.

### 9.1.1 Supply Source Impedance

In the steady state, the voltage drop from the source to the load is simply the wire resistance times the load current as modeled in 图 9-1.

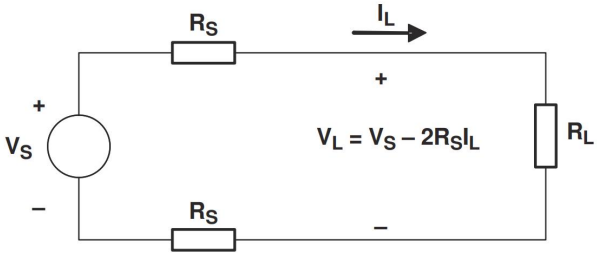



图 **9-1. Steady-State Circuit Model**

For example, if you were to provide 5-V ±5% supply power to a remote circuit with a maximum load requirement of 0.1 A (one SN65HVD08), the voltage at the load would fall below the 4.5-V minimum of most 5-V circuits with as little as 5.8 m of 28-GA conductors. 表 9-1 summarizes wire resistance and the length for 4.5 V and 3 V at the load with 0.1 A of load current. The maximum lengths would scale linearly for higher or lower load currents.

表 **9-1. Maximum Cable Lengths for Minimum Load Voltages at 0.1 A Load**

| WIRE SIZE | RESISTANCE | 4.5-V LENGTH AT 0.1 A | 3-V LENGTH AT 0.1 A |
|---|---|---|---|
| 28 Gauge | 0.213 Ω/m | 5.8 m | 41.1 m |
| 24 Gauge | 0.079 Ω/m | 15.8 m | 110.7 m |
| 22 Gauge | 0.054 Ω/m | 23.1 m | 162.0 m |
| 20 Gauge | 0.034 Ω/m | 36.8 m | 257.3 m |
| 18 Gauge | 0.021 Ω/m | 59.5 m | 416.7 m |

Under dynamic load requirements, the distributed inductance and capacitance of the power lines may not be ignored and decoupling capacitance at the load is required. The amount depends upon the magnitude and frequency of the load current change but, if only powering the SN65HVD08, a 0.1 µF ceramic capacitor is usually sufficient.

### 9.1.2 Opto-Isolated Data Buses

Long RS-485 circuits can create large ground loops and pick up common-mode noise voltages in excess of the range tolerated by standard RS-485 circuits. A common remedy is to provide galvanic isolation of the data circuit from earth or local grounds.

Transformers, capacitors, or phototransistors most often provide isolation of the bus and the local node. Transformers and capacitors require changing signals to transfer the information over the isolation barrier and phototransistors (opto-isolators) can pass steady-state signals. Each of these methods incurs additional costs and complexity, the former in clock encoding and decoding of the data stream and the latter in requiring an isolated power supply.

Quite often, the cost of isolated power is repeated at each node connected to the bus as shown in 图 9-2. The possibly lower-cost solution is to generate this supply once within the system and then distribute it along with the data line(s) as shown in 图 9-3.

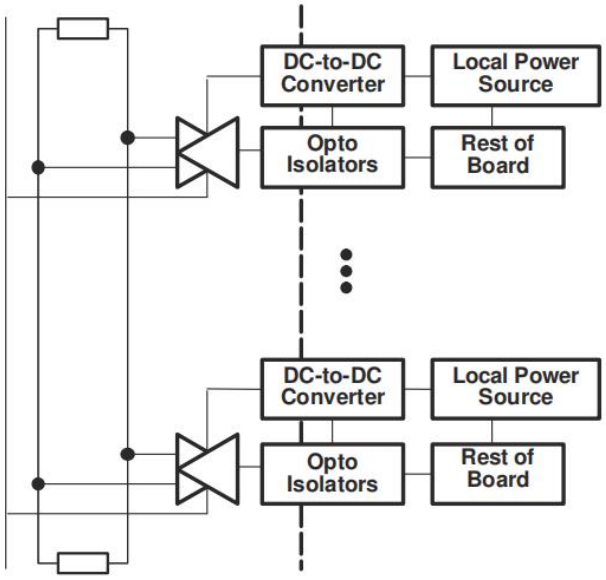



图 9-2. Isolated Power at Each Node

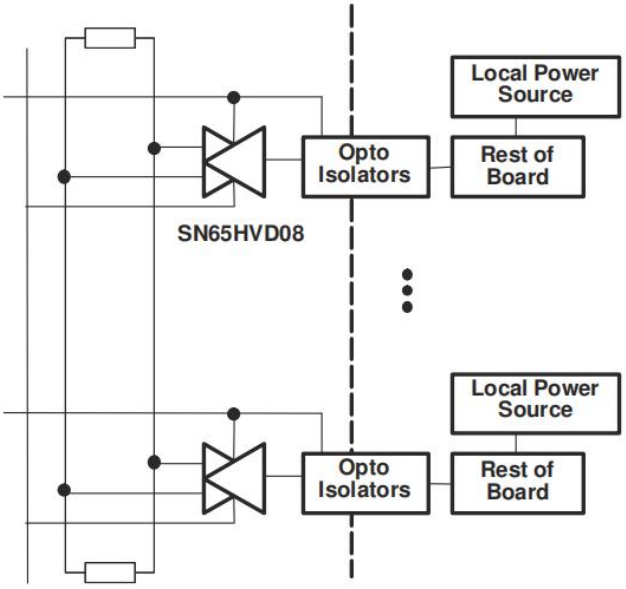



图 9-3. Distribution of Isolated Power

The features of the SN65HVD08 are particularly good for the application of 图 9-3. Due to added supply source impedance, the low quiescent current requirements and wide supply voltage tolerance allow for the poorer load regulation.

### 9.1.3 Opto Alternative

The ISO150 is a two-channel, galvanically isolated data coupler capable of data rates of 80 Mbps. Each channel can be individually programmed to transmit data in either direction.

Data is transmitted across the isolation barrier by coupling complementary pulses through high-voltage 0.4-pF capacitors. Receiver circuitry restores the pulses to standard logic levels. Differential signal transmission rejects isolation-mode voltage transients up to 1.6 kV/ms.

ISO150 avoids the problems commonly associated with opto-couplers. Optically-isolated couplers require high current pulses and allowance must be made for LED aging. The ISO150's Bi-CMOS circuitry operates at 25 mW per channel with supply voltage range matching that of the SN65HVD08 of 3 V to 5.5 V.

图 9-4 shows a typical circuit.

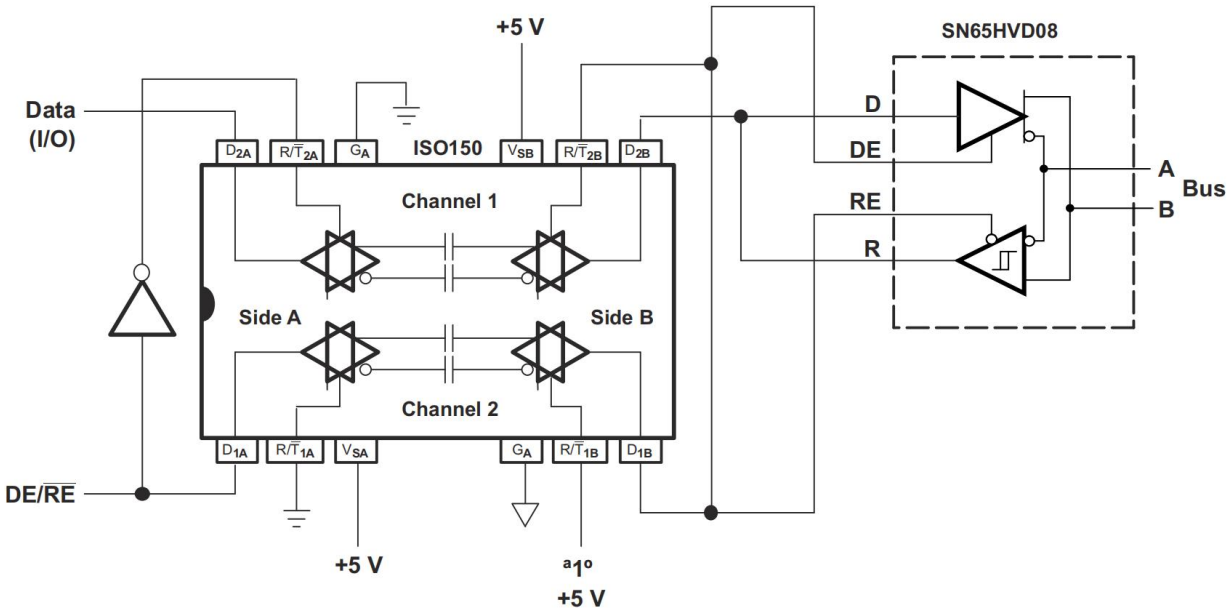



图 9-4. Isolated RS-485 Interface

### 9.2.2 Detailed Design Procedure

In order to protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary.

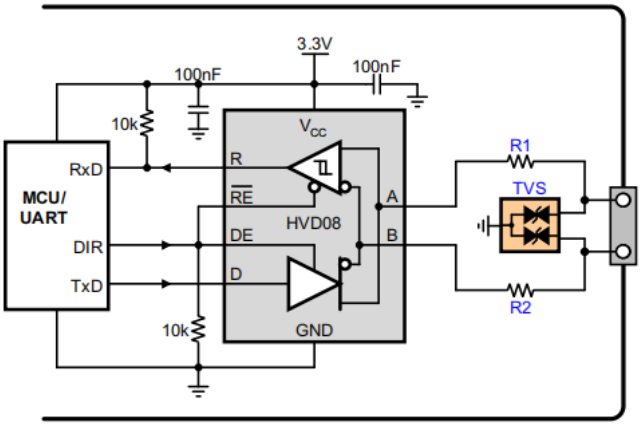



图 9-7. Transient protection against ESD, EFT, and Surge transients

#### *9.2.1.2 Stub Length*

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 方程式 1.

$$L_{stub} \leqslant 0.1 \times t_r \times v \times c \quad (1)$$

Where:

- $t_r$ is the 10/90 rise time of the driver
- c is the speed of light ($3 \times 10^8$ m/s)
- v is the signal velocity of the cable or trace as a factor of c

Per 方程式 1, the maximum recommended stub length for the minimum driver output rise time of the SNx5HVD08 for a signal velocity of 78% is 0.23 meters (0.75 feet).

#### *9.2.1.3 Bus Loading*

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the SN65HVD08 and SN75HVD08 are each 1/8 UL transceivers, it is possible to connect up to 256 receivers to the bus.

#### *9.2.1.4 Receiver Failsafe*

The differential receivers of the SNx5HVD08 family are “failsafe” to invalid bus states caused by:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic High state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the “input indeterminate” range does not include zero volts differential.

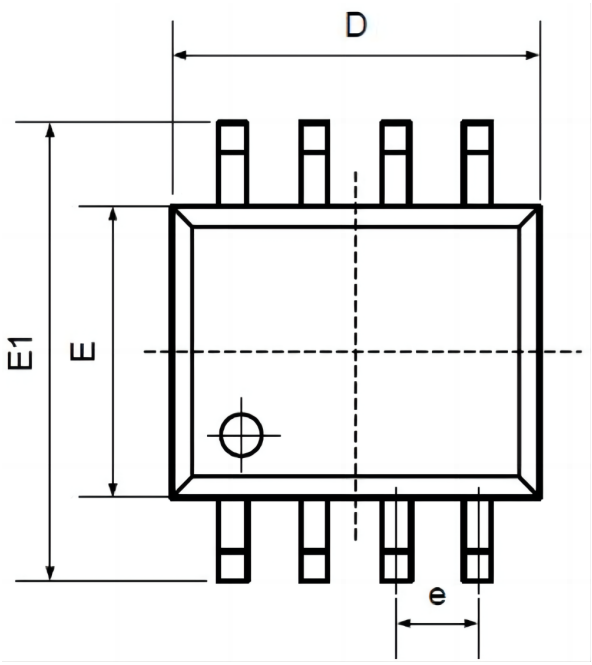
In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input VID is more positive than +200 mV, and must output a Low when VID is more negative than -200 mV. The receiver parameters which determine the failsafe performance are VIT(+) and VIT(-).

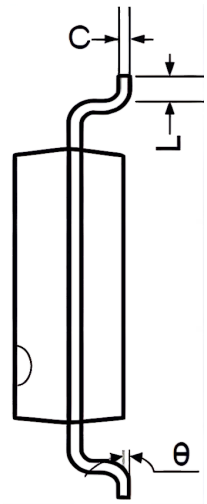
As shown in the Electrical Characteristics table, differential signals more negative than -200 mV will always cause a Low receiver output, and differential signals more positive than -10 mV will always cause a High receiver output. Thus, when the differential input signal is close to zero, it is still above the maximum VIT(+) threshold of -10 mV, and the receiver output will be High.

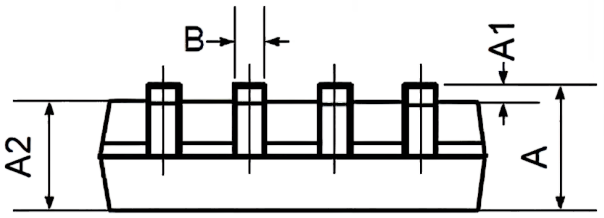
# Order information

| Order Number | Package | Package Quantity | Marking On The park |
|---|---|---|---|
| SN75HVD08DR-TUDI | SOP8 | Tape,Reel,2500 | SN75HVD08DR |
| SN75HVD08P-TUDI | DIP8 | Tube,50,A box of 2000 | SN75HVD08P |
| SN65HVD08DR-TUDI | SOP8 | Tape,Reel,2500 | SN65HVD08DR |
| SN65HVD08P-TUDI | DIP8 | Tube,50,A box of 2000 | SN65HVD08P |

# Package SOP8

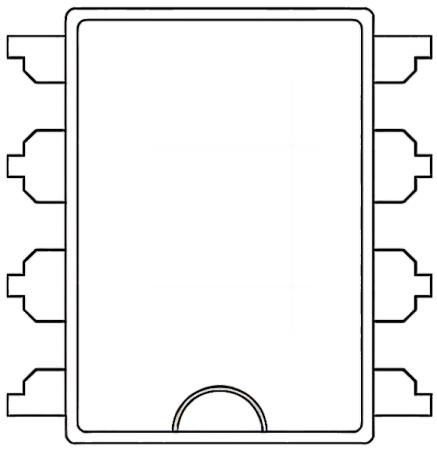


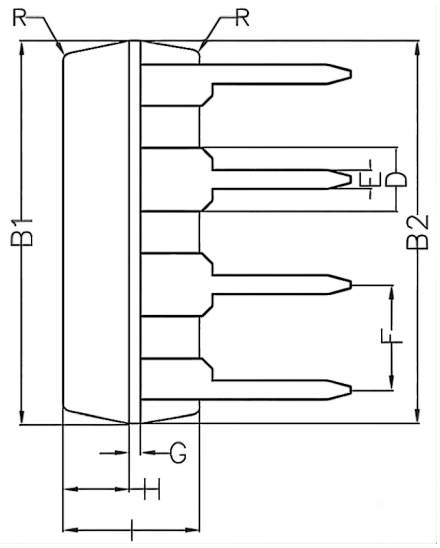



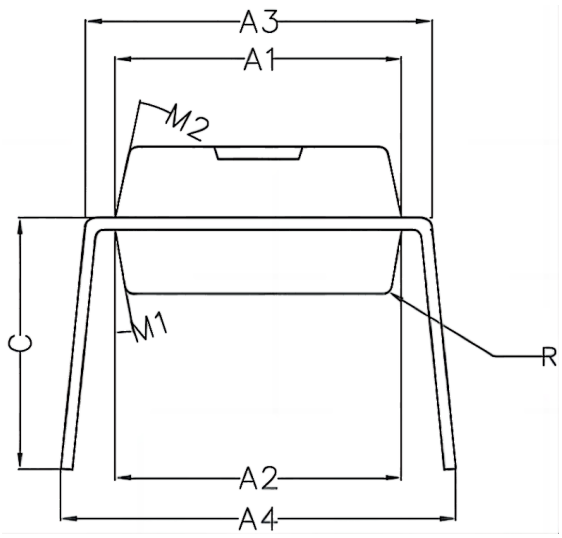




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| B | 0.330 | 0.510 | 0.013 | 0.020 |
| C | 0.190 | 0.250 | 0.007 | 0.010 |
| D | 4.780 | 5.000 | 0.188 | 0.197 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.300 | 0.228 | 0.248 |
| e | 1.270TYP | | 0.050TYP | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

# Package DIP8






| Symbol | Min | Non | Max |
|---|---|---|---|
| A1 | 6.28 | 6.33 | 6.38 |
| A2 | 6.33 | 6.38 | 6.43 |
| A3 | 7.52 | 7.62 | 7.72 |
| A4 | 7.80 | 8.40 | 9.00 |
| B1 | 9.15 | 9.20 | 9.25 |
| B2 | 9.20 | 9.25 | 9.30 |
| C | | 5.57 | |
| D | | 1.52 | |
| E | 0.43 | 0.45 | 0.47 |
| F | | 2.54 | |
| G | | 0.25 | |
| H | 1.54 | 1.59 | 1.64 |
| 工 | 3.22 | 3.27 | 3.32 |
| R | | 0.20 | |
| M1 | 9° | 10° | 11° |
| M2 | 11° | 12° | 13° |

# Important statement:

●TUDI Semiconductor reserves the right to modify the product manual without prior notice! Before placing an order, customers need to confirm whether the obtained information is the latest version and verify the completeness of the relevant information.

●Any semi-guide product is subject to failure or malfunction under specified conditions. It is the buyer's responsibility to comply with safety standards when using TUDI Semiconductor products for system design and whole machine manufacturing.And take the appropriate safety measures to avoid the potential in the risk of loss of personal injury or loss of property situation!

●TUDI Semiconductor products have not been licensed for life support, military, and aerospace applications,and therefore TUDI Semiconductor is not responsible for any consequences arising from the use of this product in these areas.

●If any or all TUDI Semiconductor products (including technical data, services) described or contained in this document are subject to any applicable local export control laws and regulations, they may not be exported without an export license from the relevant authorities in accordance with such laws.

●The specifications of any and all TUDI Semiconductor products described or contained in this document specify the performance, characteristics, and functionality of said products in their standalone state, but do not guarantee the performance, characteristics, and functionality of said products installed in Customer's products or equipment. In order to verify symptoms and conditions that cannot be evaluated in a standalone device, the Customer should ultimately evaluate and test the device installed in the Customer's product device.

●TUDI Semiconductor documentation is only allowed to be copied without any alteration of the content and with the relevant authorization.TUDI Semiconductor assumes no responsibility or liability for altered documents.

●TUDI Semiconductor is committed to becoming the preferred semiconductor brand for customers, and TUDI Semiconductor will strive to provide customers with better performance and better quallity products.