SUD70090E-VB Datasheet
N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
100	0.0085 at V_{GS} = 10 V	85
	0.0105 at V_{GS} = 4.5 V	70

FEATURES

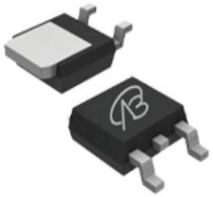
- Trench Power MOSFET
- 100 % Rg Tested
- 100 % UIS Tested

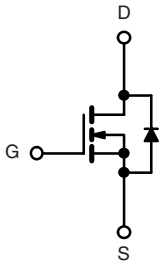
RoHS COMPLIANT

APPLICATIONS

- Primary Side Switch
- Isolated DC/DC Converter

TO-252





N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	85	A
	T_C = 125 °C		75 [a]	
Pulsed Drain Current		I_{DM}	300	
Avalanche Current	L = 0.1 mH	I_{AS}	75	
Single Pulse Avalanche Energy[b]		E_{AS}	280	mJ
Maximum Power Dissipation[b]	T_C = 25 °C	P_D	176	W
	T_A = 25 °C		3.75	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b]	Steady State	R_{thJA}	40	50	°C/W
Maximum Junction-to-Case		R_{thJC}	0.85	1.1	

Notes:
a. Package limited.
b. Surface mounted on 1" x 1" FR4 board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	100			V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1		4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			1	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125 °C			50	
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 175°C			250	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = ≥ 5 V, V_{GS} = 10 V	50			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A		0.0085		Ω
		V_{GS} = 4.5 V, I_D = 20 A		0.0105		
		V_{GS} = 10 V, I_D =20 A, T_J = 125 °C		0.017		
		V_{GS} = 10 V, I_D = 20 A, T_J = 175 °C		0.022		
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 20A	25			S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		4000		pF
Output Capacitance	C_{oss}			565		
Reverse Transfer Capacitance	C_{rss}			205		
Total Gate Charge[c]	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 45 A		105	160	nC
Gate-Source Charge[c]	Q_{gs}			17		
Gate-Drain Charge[c]	Q_{gd}			23		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 20 V, R_L = 0.6 Ω I_D ≅ 45 A, V_{GEN} = 10 V, R_g = 2.5 Ω		12	25	ns
Rise Time[c]	t_r			90	135	
Turn-Off DelayTime[c]	$t_{d(off)}$			55	85	
Fall Time[c]	t_f			130	195	
Source-Drain Diode Ratings and Characteristics T_C = 25 °C[b]						
Continuous Current	I_S				85	A
Pulsed Current	I_{SM}				140	
Forward Voltage[a]	V_{SD}	I_F = 45 A, V_{GS} = 0 V		1.0	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 50 A, dI/dt = 100 A/µs		85	140	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			4.5	7	A
Reverse Recovery Charge	Q_{rr}			0.17	0.35	µC

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

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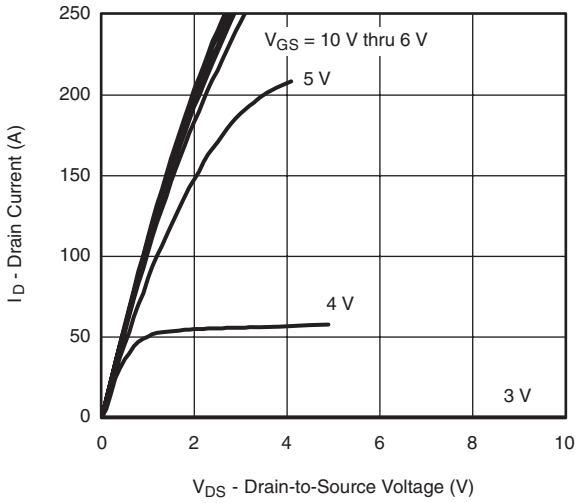
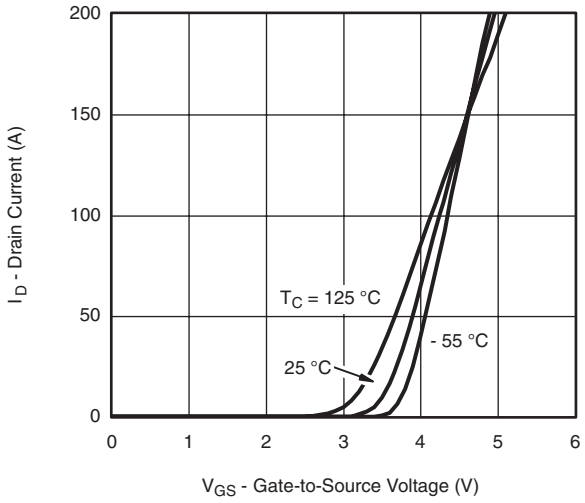
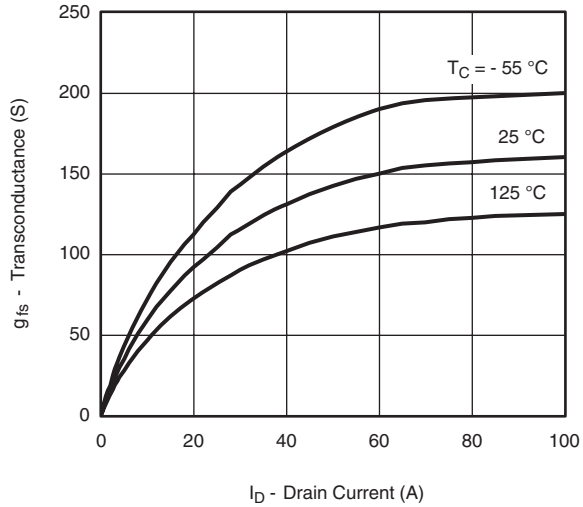
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



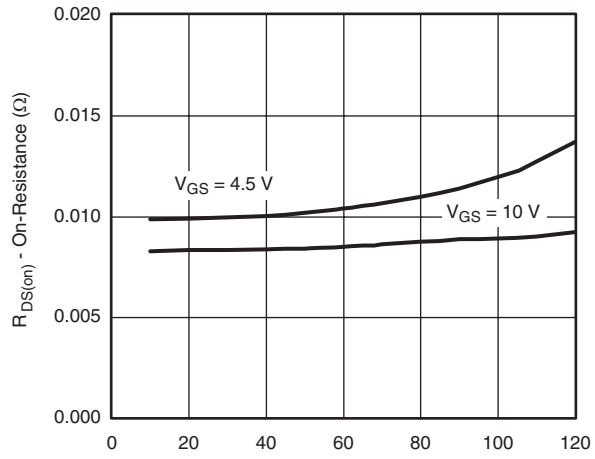
Output Characteristics



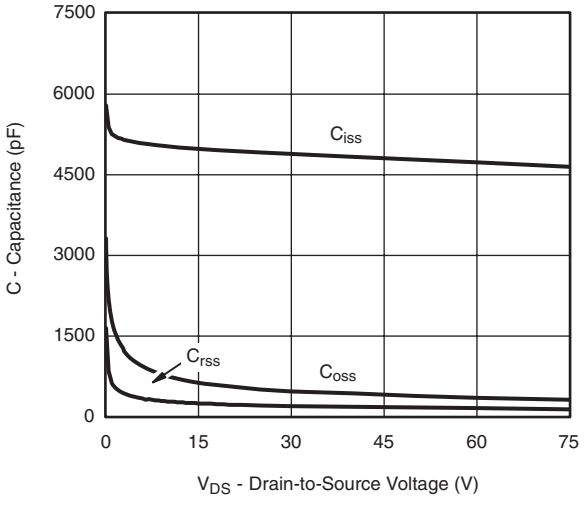
Transfer Characteristics



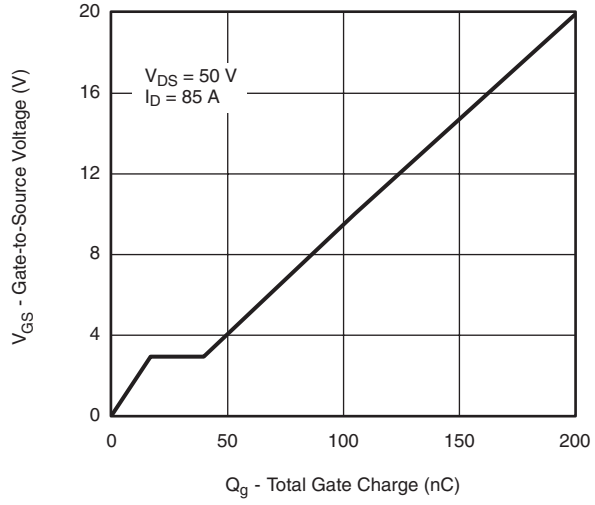
Transconductance



On-Resistance vs. Drain Current

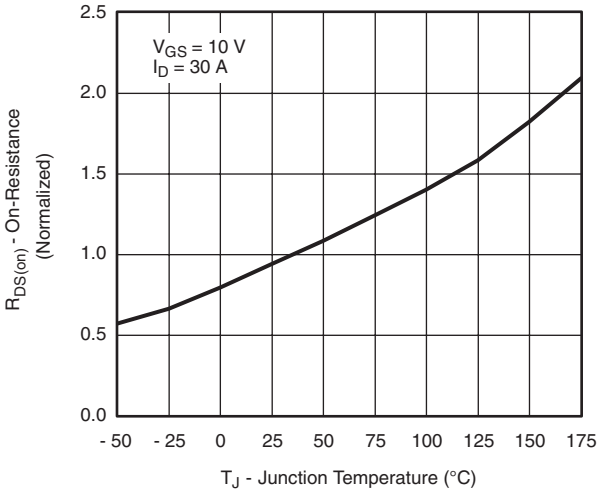


Capacitance

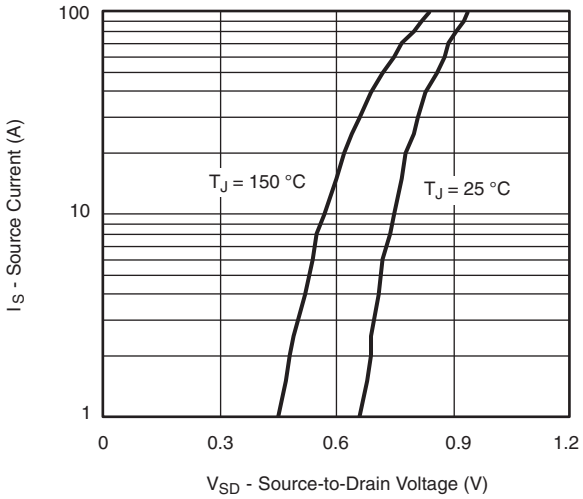


Gate Charge

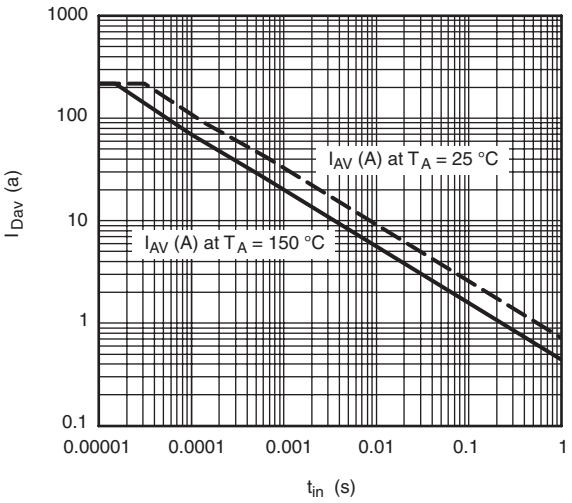
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



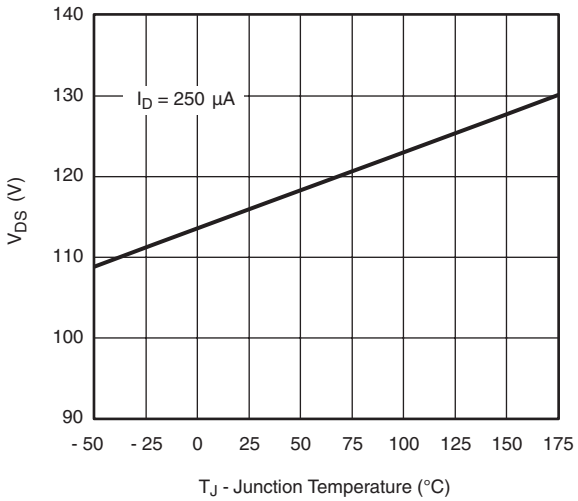
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

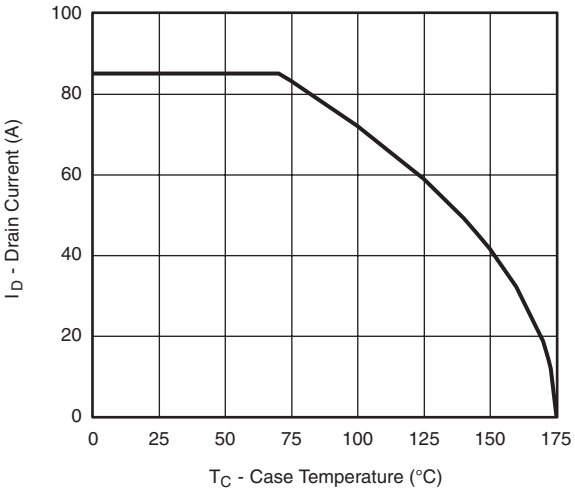


Avalanche Current vs. Time

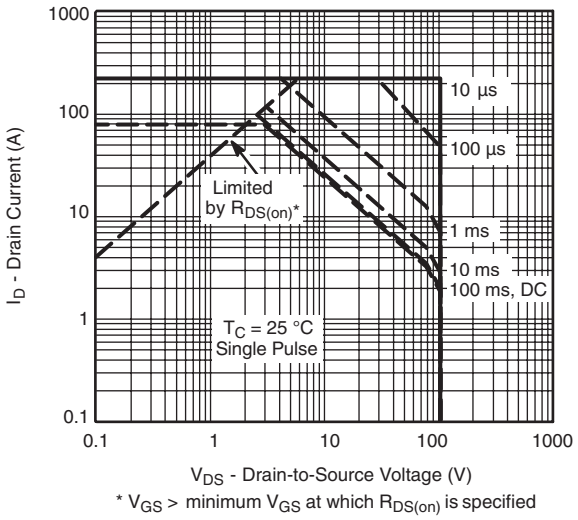


T_J - Drain-Source Breakdown vs. Junction-Temperature

THERMAL RATINGS

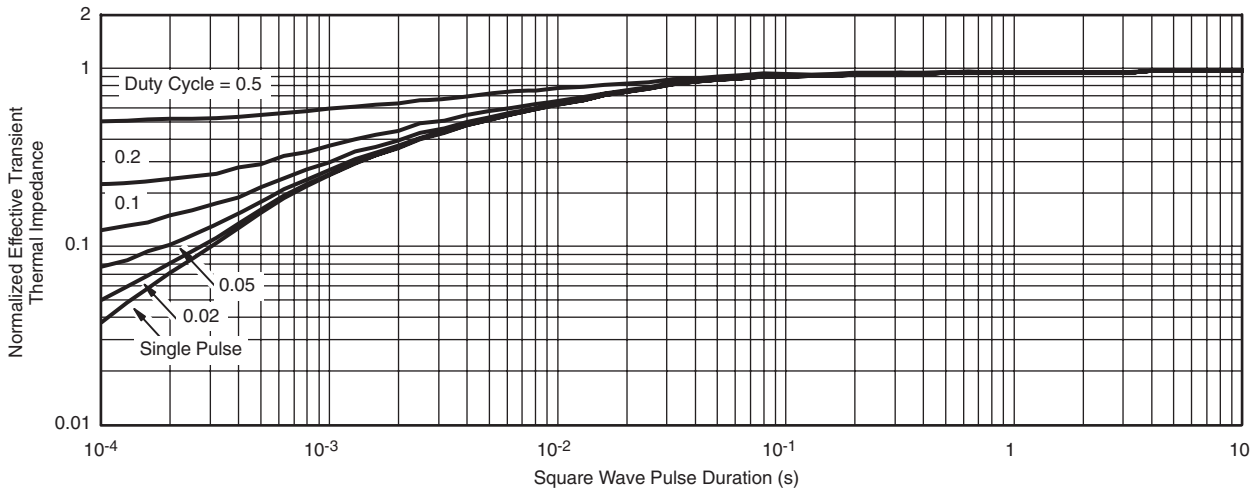


Maximum Avalanche and Drain Current vs. Case Temperature



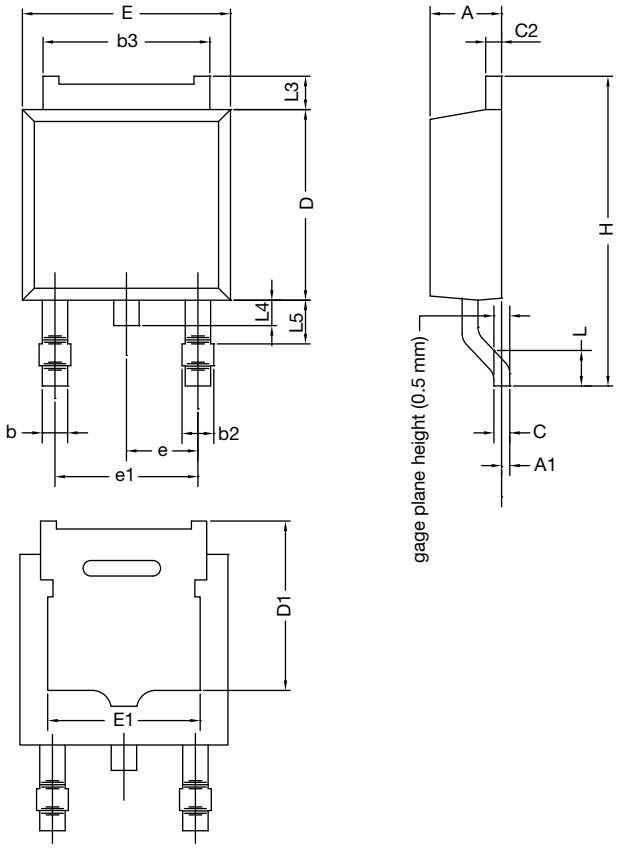
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

TO-252AA CASE OUTLINE

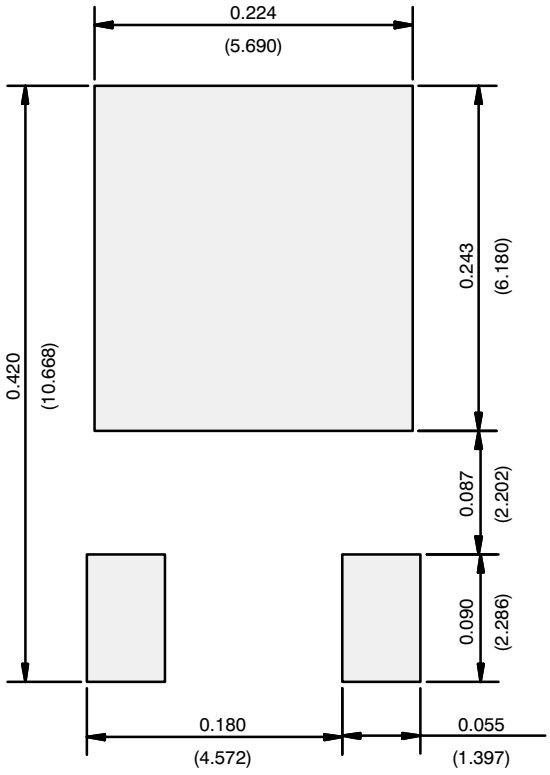


	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.14	1.52	0.045	0.060
ECN: X12-0247-Rev. M, 24-Dec-12 DWG: 5347				

Note

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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