# TPS3808 Series-TP

## Low Quiescent Programmable-Delay Supervisory



## Features

- Power-On Reset Generator with Adjustable Delay Time: 1.25ms to 10s.
- Very Low Quiescent Current: 2.8μA Typical
- High Threshold Accuracy: 0.5% Typ.
- Fixed Threshold Voltages for Standard Voltage Rails from 0.9V to 5V and Adjustable Voltage Down to 0.4V are available.
- Manual Reset ( $\overline{MR}$ ) Input.
- Open-Drain $\overline{RESET}$ Output.
- Temperature Range: -40°C to +125°C
- Package:
  SOT23-6L (TPS3808xxxDBVR-TP)
  DFN2x2-6L(TPS3808xxxDRVR-TP)

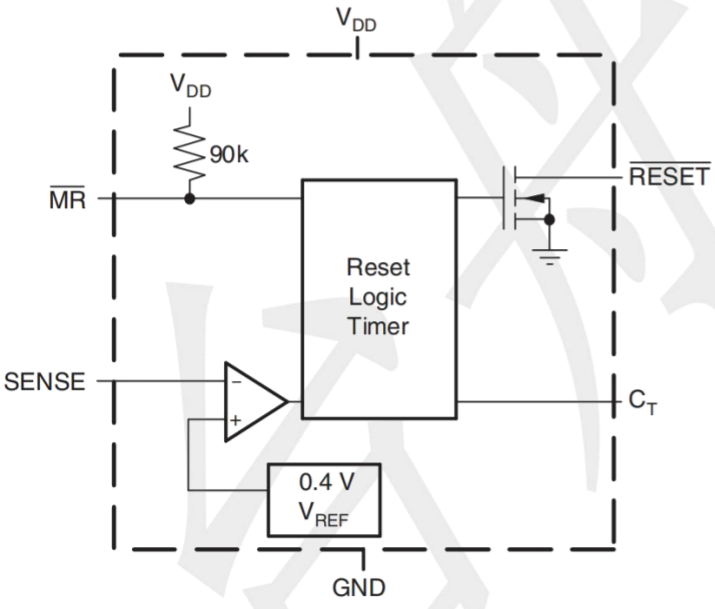
## Description

The family of microprocessor supervisory circuits monitor system voltage form 0.4V to 5.0V, asserting an open-drain $\overline{RESET}$ signal when the SENSE voltage drops below a preset threshold or when the manual reset ( $\overline{MR}$ ) pin drops to a logic low. The $\overline{RESET}$ output remains low for the user-adjustable delay time after the SENSE voltage and manual reset ( $\overline{MR}$ ) return above the respective thresholds.

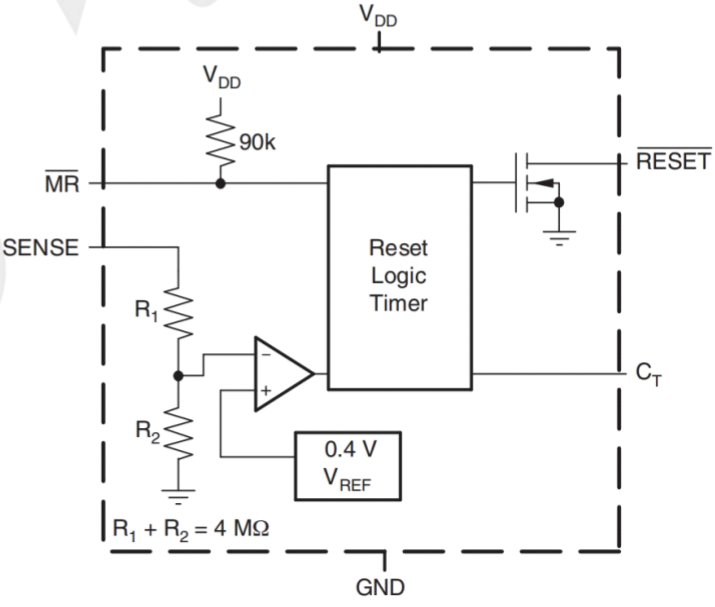
## Applications

- DSP or Microcontroller Applications capacitor.
- Notebook/Desktop Computers
- FPGA/ASIC Applications
- Portable/Battery-Powered Products
- PDAs/Hand-Held Products
  battery-powered applications.

## Block Diagram




Adjustable-Voltage Version



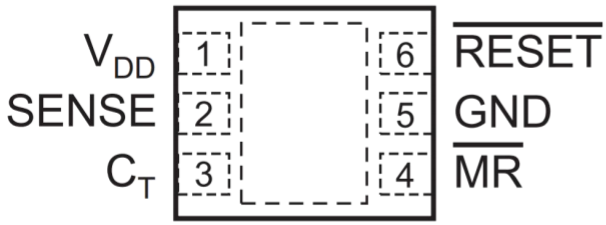

Fixed-Voltage Version

## Device Voltage Thresholds

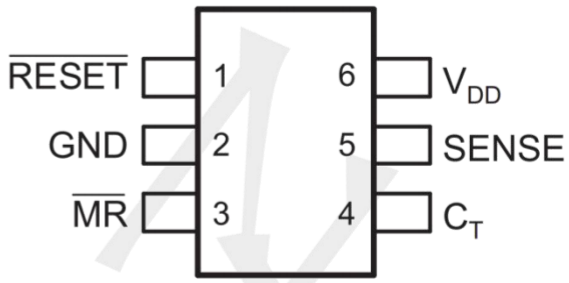
| PART NUMBER | NOMINAL SUPPLY VOLTAGE | THRESHOLD VOLTAGE ($V_{IT}$) | PACKAGE DESCRIPTION |
|---|---|---|---|
| TPS3808G01DBVR-TP | Adjustable | 0.405 V | SOT23-6L |
| TPS3808G09DBVR-TP | 0.9 V | 0.84 V | SOT23-6L |
| TPS3808G12DBVR-TP | 1.2 V | 1.12 V | SOT23-6L |
| TPS3808G125DBVR-TP | 1.25 V | 1.16 V | SOT23-6L |
| TPS3808G15DBVR-TP | 1.5 V | 1.40 V | SOT23-6L |
| TPS3808G18DBVR-TP | 1.8 V | 1.67 V | SOT23-6L |
| TPS3808G19DBVR-TP | 1.9 V | 1.77 V | SOT23-6L |
| TPS3808G25DBVR-TP | 2.5 V | 2.33 V | SOT23-6L |
| TPS3808G30DBVR-TP | 3 V | 2.79 V | SOT23-6L |
| TPS3808G33DBVR-TP | 3.3 V | 3.07 V | SOT23-6L |
| TPS3808G50DBVR-TP | 5 V | 4.65 V | SOT23-6L |
| TPS3808G01DRVR-TP | Adjustable | 0.405 V | DFN2x2-6L |
| TPS3808G09DRVR-TP | 0.9 V | 0.84 V | DFN2x2-6L |
| TPS3808G12DRVR-TP | 1.2 V | 1.12 V | DFN2x2-6L |
| TPS3808G125DRVR-TP | 1.25 V | 1.16 V | DFN2x2-6L |
| TPS3808G15DRVR-TP | 1.5 V | 1.40 V | DFN2x2-6L |
| TPS3808G18DRVR-TP | 1.8 V | 1.67 V | DFN2x2-6L |
| TPS3808G19DRVR-TP | 1.9 V | 1.77 V | DFN2x2-6L |
| TPS3808G25DRVR-TP | 2.5 V | 2.33 V | DFN2x2-6L |
| TPS3808G30DRVR-TP | 3 V | 2.79 V | DFN2x2-6L |
| TPS3808G33DRVR-TP | 3.3 V | 3.07 V | DFN2x2-6L |
| TPS3808G50DRVR-TP | 5 V | 4.65 V | DFN2x2-6L |

**Note:** table shows the nominal rail to be monitored and the corresponding threshold voltage of the device.

## Pin Definition




DFN2X2-6L




SOT23-6L

## PIN CONFIGURATION

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOT-23-6L | DFN2X2-6L | | |
| $C_T$ | 4 | 3 | I | Reset period programming pin. Connecting this pin to VDD through a 40-kΩ to 200-kΩ resistor or leaving it open results in fixed delay times (see Electrical Characteristics). Connecting this pin to a ground referenced capacitor ≥ 100 pF gives user-programmable delay time. See the Selecting the Reset Delay Time for more information. |
| GND | 2 | 5 | — | Ground |
| $\overline{MR}$ | 3 | 4 | I | Manual reset. Driving this pin low asserts $\overline{RESET}$. $\overline{MR}$ is internally tied to $V_{DD}$ by a 90-kΩ pullup resistor. |
| $\overline{RESET}$ | 1 | 6 | O | Reset. This is an open-drain output that is driven to a low impedance state when $\overline{RESET}$ is asserted (either the SENSE input is lower than the threshold voltage ($V_{IT}$) or the $\overline{MR}$ pin is set to a logic low). $\overline{RESET}$ remains low (asserted) for the reset period after both SENSE is above $V_{IT}$ and $\overline{MR}$ is set to a logic high. A pullup resistor from 10 kΩ to 1 MΩ must be used on this pin and allows the reset pin to attain voltages higher than $V_{DD}$. |
| SENSE | 5 | 2 | I | Voltage sense. This pin is connected to the voltage to be monitored. If the voltage at this terminal drops below the threshold voltage ($V_{IT}$), $\overline{RESET}$ is asserted. |
| VDD | 6 | 1 | I | Supply voltage. It is good analog design practice to place a 0.1-μF ceramic capacitor close to this pin. |
| Thermal Pad | — | Pad | — | Thermal pad; connect to ground plan to enhance thermal performance of the package. |

## Absolute Maximum Ratings

**over operating free-air temperature range (unless otherwise noted)**

| SYMBOL | PARAMETER | RATINGS | UNIT |
|---|---|---|---|
| $V_{DD}$ | Input Voltage Range | -0.3 ~ +7V | V |
| $V_{CT}$ | $C_T$ Voltage Range | -0.3 ~ $V_{DD}$+0.3V | V |
| $V_{RESET}$ | Other Voltage Range | -0.3 ~ +7V | V |
| $V_{MR}$ | Other Voltage Range | -0.3 ~ +7V | V |
| $V_{SENSE}$ | Other Voltage Range | -0.3 ~ +7V | V |
| $I_{RESET}$ | RESET pin Current | 5mA | mA |
| $T_J$ | Operating Junction Temperature Range | -40 ~ +125 | ℃ |
| Tstg | Storage temperature range | -65～150 | ℃ |

## Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condi- tions above those indicated in the operational sec- tions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended Operation Conditions

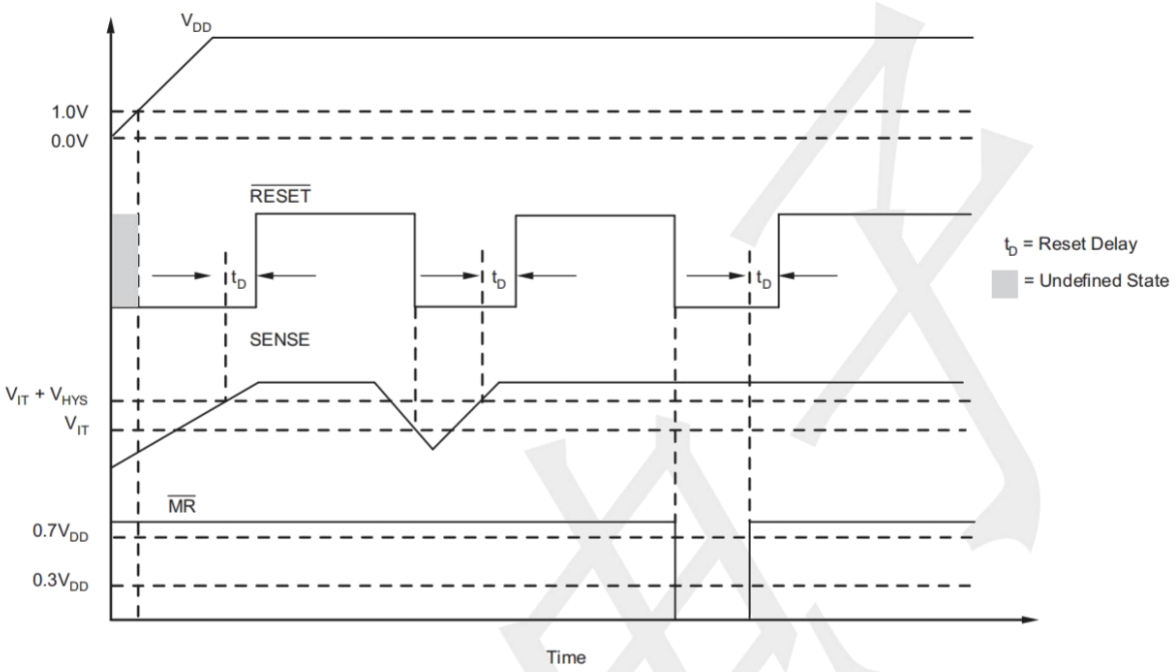
| SYMBOL | PARAMETER | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VDD | Supply Voltage | -- | 1.7 | -- | 6.5 | V |
| $V_{IH}$ | Input High Voltage MR | -- | -- | -- | VDD | V |
| | Input High Voltage for Open-drain RESET, SENSE | -- | 0 | -- | 6.5 | V |
| $V_{IL}$ | Input Low Voltage MR. | -- | -- | -- | VDD+0.3 | V |
| $T_A$ | Operating Temperature | -- | -40 | -- | 125 | °C |

# Electrical Characteristics

**Unless otherwise specified, -40°C≤$T_A$≤125°C, 1.7V≤$V_{DD}$≤6.5V, $R_{RESET}$=100kΩ, $C_{RESET}$=50Pf, Typical values are at $T_A$=+25°C**

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | Input supply range | | | 1.7 | | 6.5 | V |
| $I_{DD}$ | Supply current (into $V_{DD}$ pin) | $V_{DD}$ = 3.3 V, RESET not asserted, MR, RESET, $C_T$ open | | | 2.8 | 5 | µA |
| | | $V_{DD}$ = 6.5 V, RESET not asserted, MR, RESET, $C_T$ open | | | 3.0 | 6 | |
| $V_{OL}$ | Low-level output voltage | 1.3 V ≤ $V_{DD}$ < 1.8 V, $I_{OL}$ = 0.4 mA | | | | 0.3 | V |
| | | 1.3 V ≤ $V_{DD}$ ≤ 6.5 V, $I_{OL}$ = 1 mA | | | | 0.4 | V |
| | Power-up reset voltage(1) | $V_{OL}$ (max) = 0.2 V, $I_{\overline{RESET}}$ = 15 µA | | | | 1.0 | V |
| $V_{IT}$ | Negative-going input threshold accuracy | TPAX3808G01 | | –2 | ±1 | 2 | % |
| | | $V_{IT}$ ≤ 3.3 V | | –1.5 | ±0.5 | 1.5 | |
| | | 3.3 V < $V_{IT}$ ≤ 5 V | | –2 | ±1 | 2 | |
| | | $V_{IT}$ ≤ 3.3 V | –40°C < $T_J$ < 85°C | –1.25 | ±0.5 | 1.25 | |
| | | 3.3 V < $V_{IT}$ ≤ 5 V | | –1.5 | ±0.5 | 1.5 | |
| $V_{HYS}$ | Hysteresis on $V_{IT}$ pin | TPAX3808G01 | | | 1.5 | | %$V_{IT}$ |
| | | –40°C < $T_J$ < 85°C | | | 1 | 2 | |
| $R_{\overline{RM}}$ | $\overline{MR}$ internal pullup resistance | $V_{SENSE}$ = $V_{IT}$ | | 70 | 90 | | kΩ |
| $I_{SENSE}$ | Input current at SENSE pin | TPAX3808G01 | | –25 | | 25 | nA |
| | | $V_{SENSE}$ = 6.5 V | | | 1.7 | | µA |
| $I_{OH}$ | $\overline{RESET}$ leakage current | $V_{\overline{RESET}}$ = 6.5 V, $\overline{RESET}$ not asserted | | | | 300 | nA |
| $C_{IN}$ | Input capacitance, any pin | $C_T$ pin | $V_{IN}$ = 0 V to $V_{DD}$ | | 5 | | pF |
| | | Other pins | $V_{IN}$ = 0 V to 6.5 V | | 5 | | |
| $V_{IL}$ | $\overline{MR}$ logic low input | | | 0 | | 0.3 $V_{DD}$ | V |
| $V_{IH}$ | $\overline{MR}$ logic high input | | | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| $t_d$ | RESET delay time | $C_T$ = Open | See Timing Diagram | 12 | 20 | 28 | ms |
| | | $C_T$ = $V_{DD}$ | | 180 | 300 | 420 | |
| | | $C_T$ = 100 pF | | 0.75 | 1.25 | 1.75 | |
| | | $C_T$ = 180 nF | | 0.7 | 1.2 | 1.7 | S |
| $t_{pHL}$ | Propagation delay | MR to RESET | $V_{IH}$ = 0.7 $V_{DD}$, $V_{IL}$ = 0.3 $V_{DD}$ | | 150 | | nS |
| | High-level to low-level $\overline{RESET}$ delay | SENSE to $\overline{RESET}$ | $V_{IH}$ = 1.05 $V_{IT}$, $V_{IL}$ = 0.95 $V_{IT}$ | | 20 | | uS |
| $t_w$ | Maximum transient duration | SENSE | $V_{IH}$ = 1.05 $V_{IT}$, $V_{IL}$ = 0.95 $V_{IT}$ | | 20 | | uS |
| | | MR | $V_{IH}$ = 0.7 $V_{DD}$, $V_{IL}$ = 0.3 $V_{DD}$ | | 0.001 | | uS |

## Timing Diagram

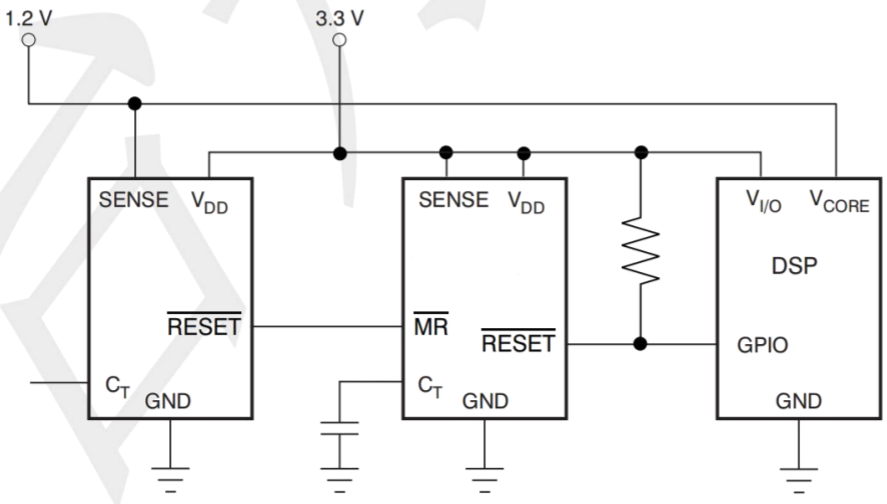



**MR and SENSE Reset Timing Diagram**

**Truth Table**

| MR | SENSE>VIT | RESET |
|---|---|---|
| L | 0 | L |
| L | 1 | L |
| H | 0 | L |
| H | 1 | H |

## Typical Application Schematic



## Functional Description

The microprocessor supervisory product family is designed to assert a $\overline{\text{RESET}}$ signal when either the SENSE pin voltage drops below $V_{IT}$ or the manual reset ( $\overline{\text{MR}}$ ) is driven low. The $\overline{\text{RESET}}$ output remains asserted for a user-adjustable time after both the manual reset ( $\overline{\text{MR}}$ ) and SENSE voltages return above the respective thresholds. A broad range of the voltage threshold and reset delay time adjustments are available, allowing these devices to be used in a wide array of applications. Reset threshold voltages can be factory-set from 0.82V to 3.3V or from 4.4V to 5.0V, while the can be set to any voltage above 0.405V using an external resistor divider. Two preset delay times are also user-selectable: connecting the $C_T$ pin to $V_{DD}$results in a 300ms reset delay, while leaving the $C_T$ pin open yields a 20ms reset delay. In addition, connecting a capacitor between $C_T$ and GND allows the designer to select any reset delay period from 1.25ms to 10s.

## RESET Output

The open-drain $\overline{\text{RESET}}$ output is typically connected to the $\overline{\text{RESET}}$ input of a microprocessor. A pull-up resistor must be used to hold this line high when $\overline{\text{RESET}}$ is not asserted. The $\overline{\text{RESET}}$ output is undefined for voltage below 1.0V, but this is normally not a problem since most microprocessors do not function below this voltage. $\overline{\text{RESET}}$ remains high (unasserted) as long as SENSE is above its threshold($V_{IT}$) and the manual reset ( $\overline{\text{MR}}$ ) is logic high. If either SENSE falls below $V_{IT}$ or $\overline{\text{MR}}$ is driven low, $\overline{\text{RESET}}$ is asserted, driving the $\overline{\text{RESET}}$ pin to low impedance.

Once $\overline{\text{MR}}$ is again logic high and SENSE is above $V_{IT}$ + VHYS (the threshold hysteresis), a delay circuit is enabled which holds $\overline{\text{RESET}}$ low for a specified reset delay period. Once the reset delay has expired, the $\overline{\text{RESET}}$ pin goes to a high impedance state. The pull-up resistor from the open-drain $\overline{\text{RESET}}$ to the supply line can be used to allow the reset signal for the microprocessor to have a voltage higher than $V_{DD}$ (up to 6.5V). The pull-up resistor should be no smaller than 10kΩ as a result of the finite impedance of the $\overline{\text{RESET}}$ line.

## SENSE Input

The SENSE input provides a pin at which any system voltage can be monitored. If the voltage on this pin drops below $V_{IT}$, then $\overline{\text{RESET}}$ is asserted. The comparator has a built-in hysteresis to ensure smooth $\overline{\text{RESET}}$ assertions and de-assertions. It is good analog design practice to put a 1nF to 10nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitic.
The can be used to monitor any voltage rail down to 0.405V by resister divider.

## Manual Reset ( $\overline{\text{MR}}$ ) Input

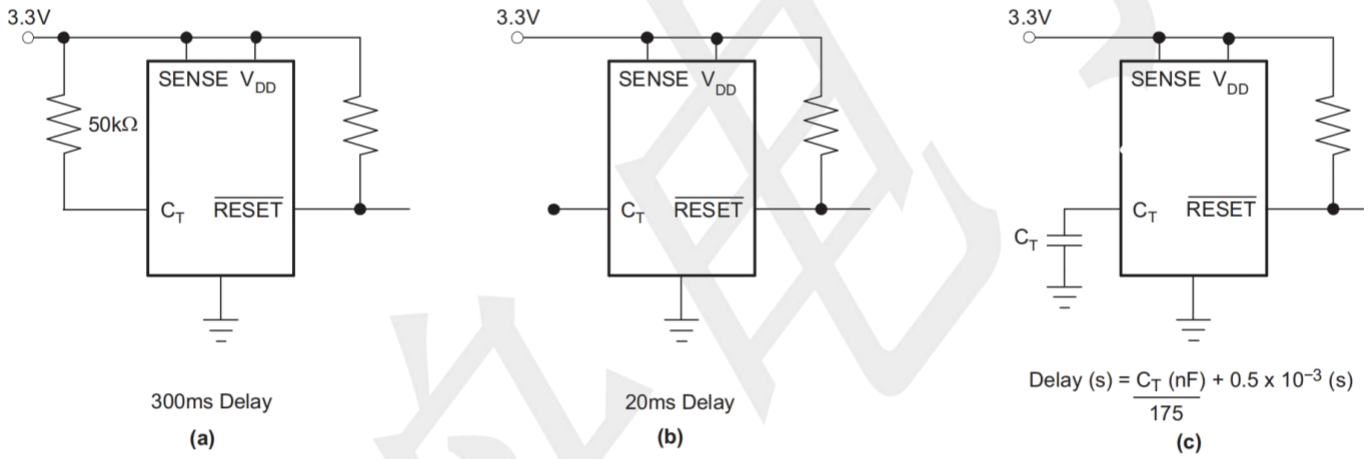
The manual reset ( $\overline{\text{MR}}$ ) input allows a processor or other logic circuits to initiate a reset. A logic low ($0.3V_{DD}$) on $\overline{\text{MR}}$ will cause $\overline{\text{RESET}}$ to assert. After $\overline{\text{MR}}$ returns to a logic high and SENSE is above its reset threshold, $\overline{\text{RESET}}$ is de-asserted after the user defined reset delay expires. Note that $\overline{\text{MR}}$ is internally tied to $V_{DD}$ using a 90kohm resistor so this pin can be left unconnected if $\overline{\text{MR}}$ will not be used. Do not apply voltage level over VDD.

## Selecting the RESET Delay Time

The has three options for setting the $\overline{\text{RESET}}$ delay time.

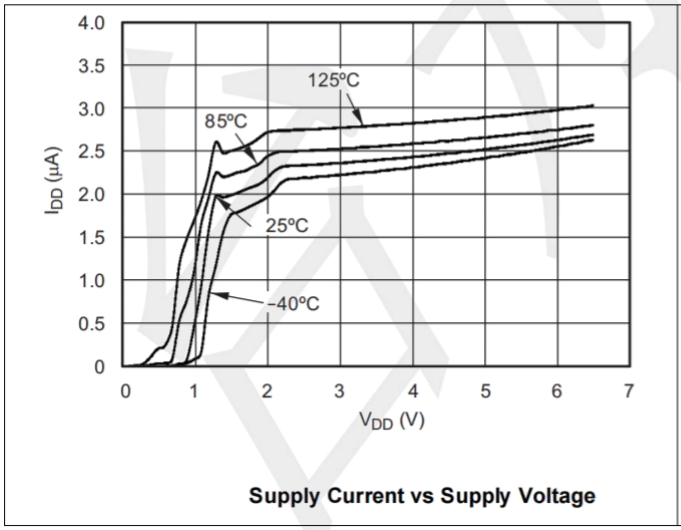
1. A fixed 300ms typical delay time by tying $C_T$ to $V_{DD}$ through a resistor from 40kΩ to 200kΩ. As below Figure (a) shown.
2. A fixed 20ms delay time by leaving the $C_T$ pin open. As below Figure (b) shown.
3. A ground referenced capacitor connected to $C_T$ for a user-defined program time between 1.25ms and 10s. The capacitor $C_T$ should be ≥ 100pF nominal value in order for the to recognize that the capacitor is present. The capacitor value for a given delay time can be calculated using the following equation: $C_T(nF)=[t_D(s)-0.5x10^{-3}(s)]x175$. As below Figure (c) shown.

The reset delay time is determined by the time it takes an on-chip precision 220nA current source to charge the external capacitor to 1.23V. When a $\overline{\text{RESET}}$ is asserted the capacitor is discharged. When the $\overline{\text{RESET}}$ conditions are cleared, the internal current source is enabled and begins to charge the external capacitor. When the voltage on this capacitor reaches 1.23V, $\overline{\text{RESET}}$ is de-asserted. Note that a low leakage type capacitor such as a ceramic should be used and the stray capacitance around this pin may cause errors in the reset delay time.

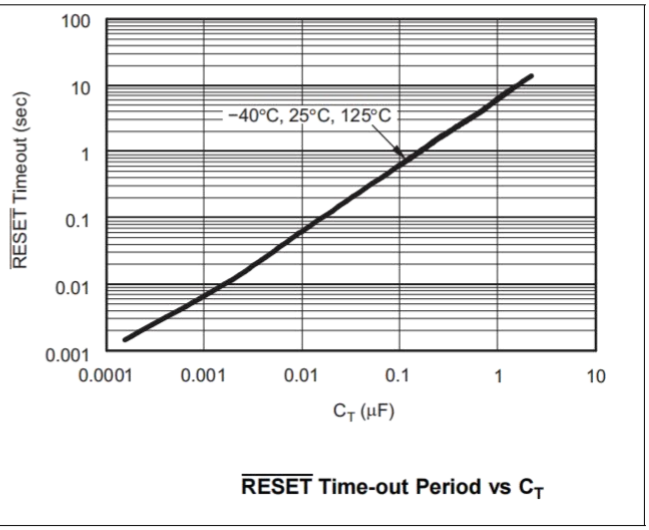



**Configuration Used to Set the $\overline{\text{RESET}}$ Delay Time**

## Application Curves



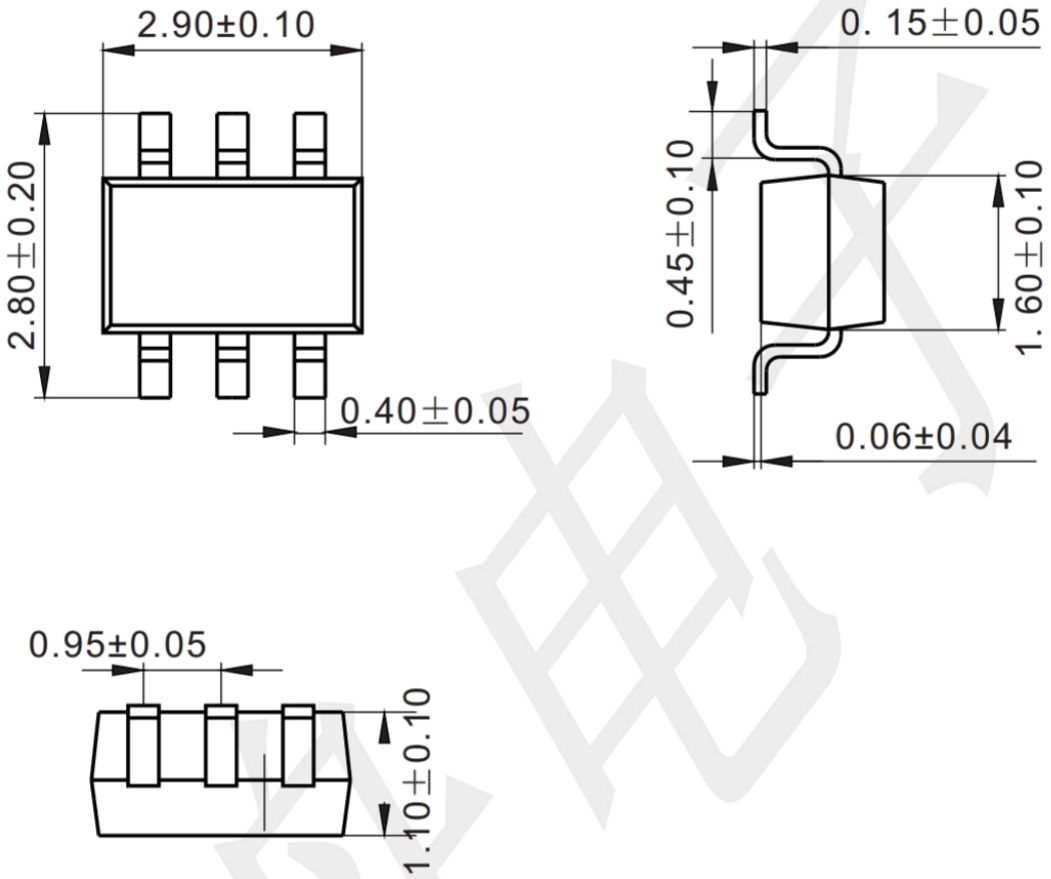

**Supply Current vs Supply Voltage**



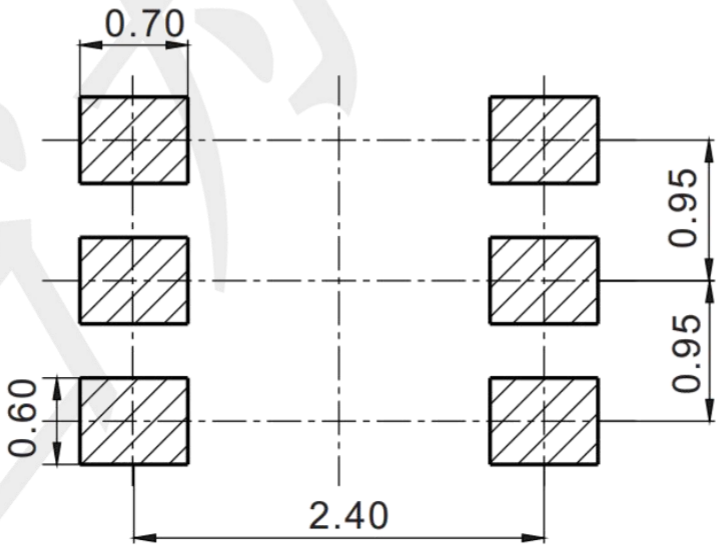

**$\overline{\text{RESET}}$ Time-out Period vs $C_T$**

## Package Outline Dimensions (unit: mm)

**SOT23-6L**

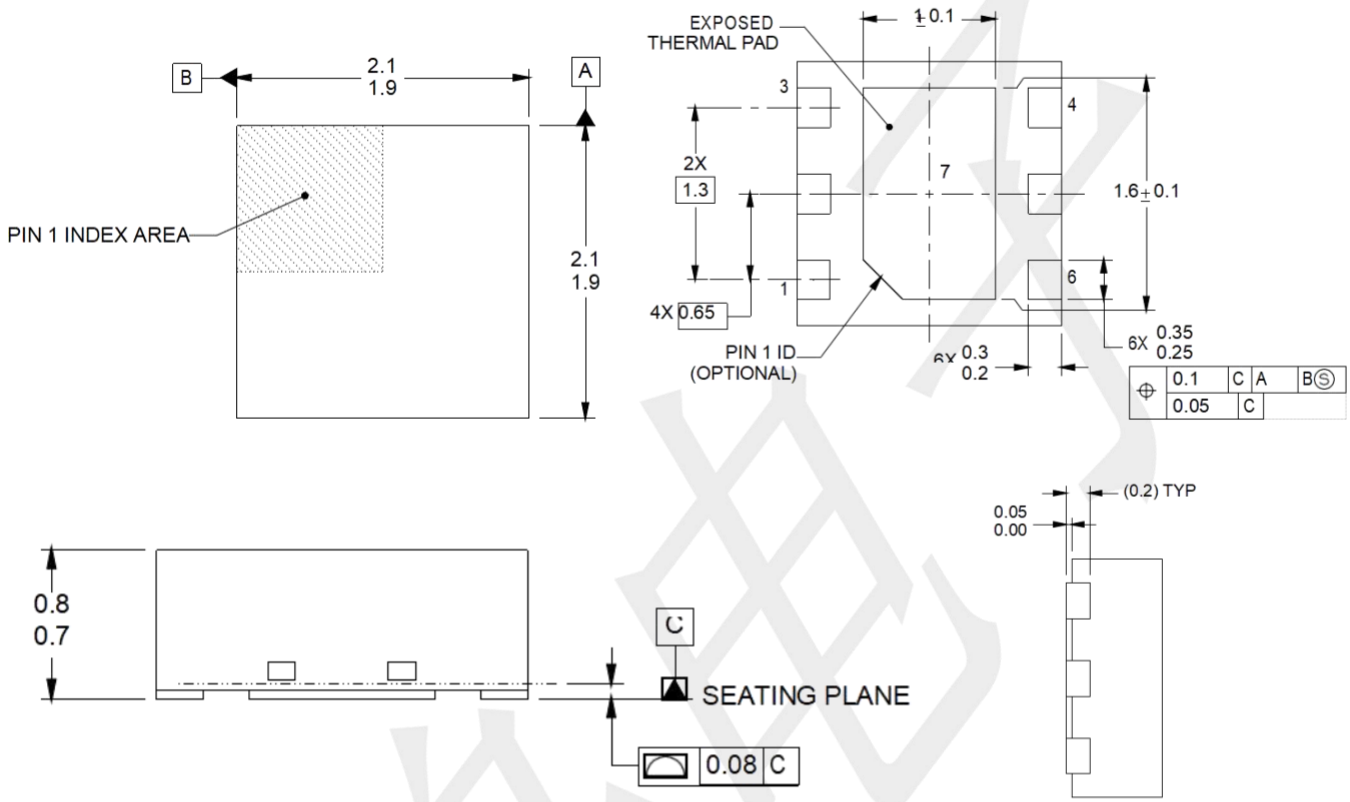



## Mounting Pad Layout (unit: mm)

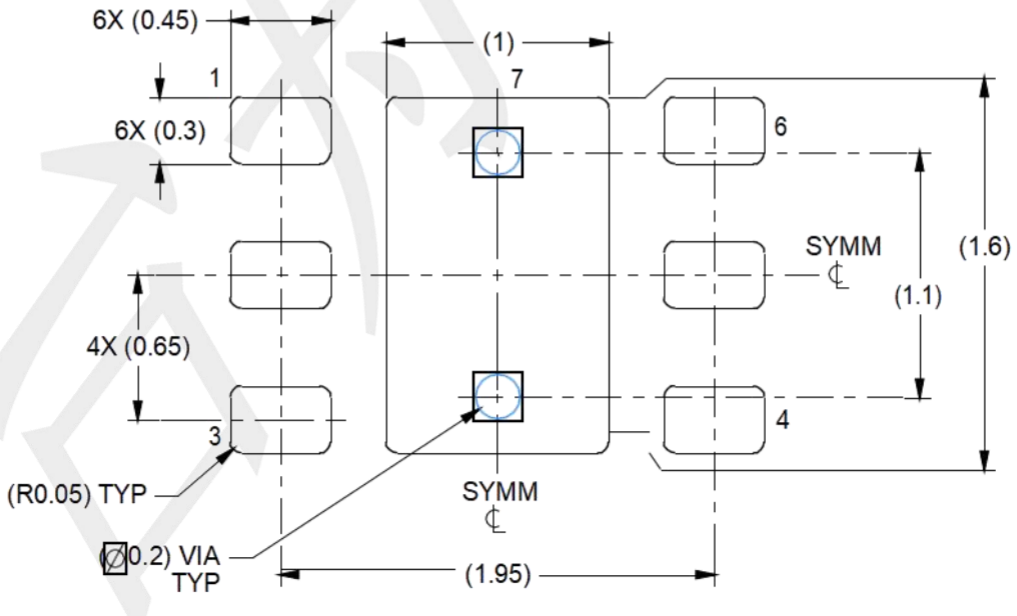


## Package Outline Dimensions (unit: mm)

### DFN2X2-6L




## Mounting Pad Layout (unit: mm)



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