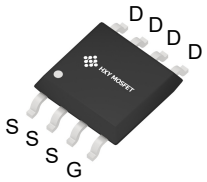
DMN2009USS

N-Channel Enhancement Mode MOSFET

Description

The DMN2009USS uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

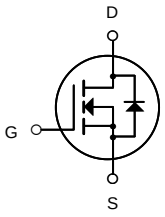


SOP-8
(SO-8)

General Features

V_{DS} = 20V I_D =20 A

$R_{DS(ON)}$ < 5.5mΩ @ V_{GS}=4.5 V



N-Channel MOSFET

Application

Battery protection

Load switch

Uninterruptible power supply

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
DMN2009USS	SOP-8(SO-8)	HXY MOSFET	3000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	±12	V
I_D	Drain Current – Continuous (T_C=25℃)	20	A
	Drain Current – Continuous (T_C=70 ℃)	16	A
I_{DM}	Drain Current – Pulsed[1]	140	A
EAS	Single Pulse Avalanche Energy[2]	162	mJ
IAS	Single Pulse Avalanche Current[2]	57	A
P_D	Power Dissipation (T_C=25℃)	3.1	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
$R_{\theta JA}$	Thermal Resistance Junction to ambient	40	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{DSS}	I_D=250 uA, V_{GS}=0V	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V, V_{GS}=0V			1	uA
		V_{DS}=20V, V_{GS}=0V, T_J=55℃			5	
Gate-Body Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±12V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} , I_D=250uA	0.5		1.6	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=20A			5.5	mΩ
		V_{GS}=4.5V, I_D=20A T_J=125℃			7	
		V_{GS}=2.5V, I_D=18A			7	
On State Drain Current	$I_{D(ON)}$	V_{GS}=10V, V_{DS}=5V	140			A
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D=20A		105		S
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=10V, f=1MHz	3080		4630	pF
Output Capacitance	C_{oss}		520		960	
Reverse Transfer Capacitance	C_{rss}		350		810	
Gate Resistance	R_g	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.6		2.1	Ω
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=10V, I_D=20A	28		43	nC
Gate Source Charge	Q_{gs}		7		11	
Gate Drain Charge	Q_{gd}		7		17	
Turn-On DelayTime	$t_{d(on)}$	V_{GS}=10V, V_{DS}=10V, R_L=0.5Ω, R_{GEN}=3Ω		7		ns
Turn-On Rise Time	t_r			8		
Turn-Off DelayTime	$t_{d(off)}$			70		
Turn-Off Fall Time	t_f			18		
Body Diode Reverse Recovery Time	t_{rr}	I_F= 20A, dI/dt= 500A/us	13		20	nC
Body Diode Reverse Recovery Charge	Q_{rr}		29		43	
Maximum Body-Diode Continuous Current	I_S				4	A
Diode Forward Voltage	V_{SD}	I_S=1A,V_{GS}=0V			1	V

Note : The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

Typical Characterisitics

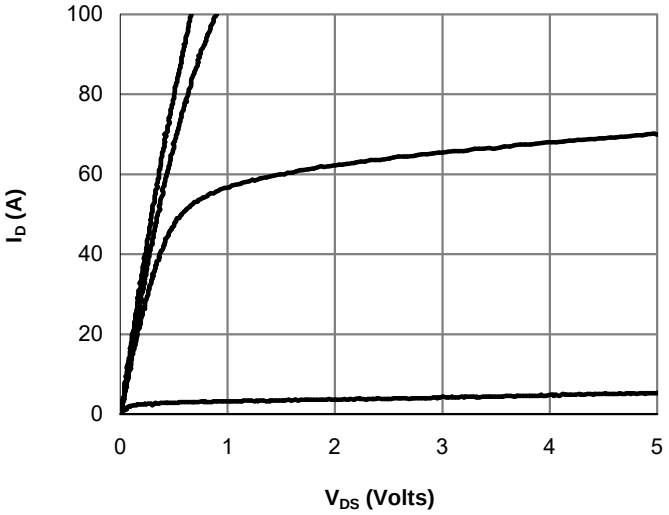


Fig 1: On-Region Characteristics (Note E)

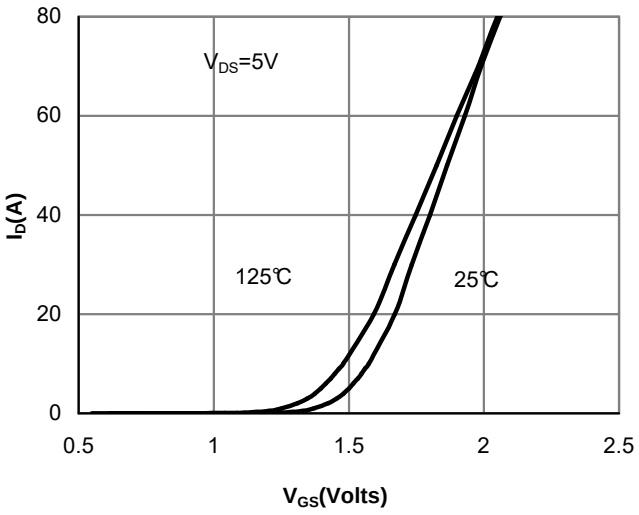


Figure 2: Transfer Characteristics (Note E)

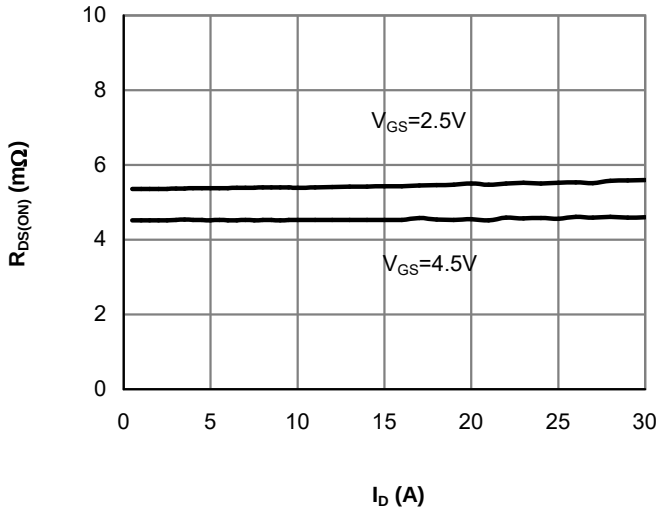


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

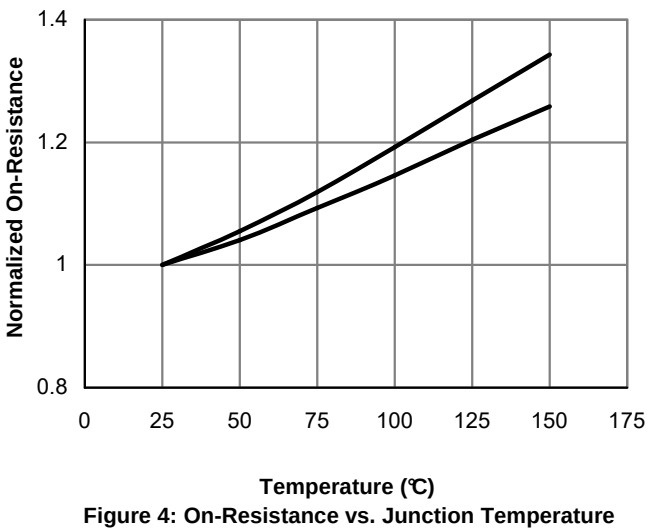


Figure 4: On-Resistance vs. Junction Temperature (Note E)

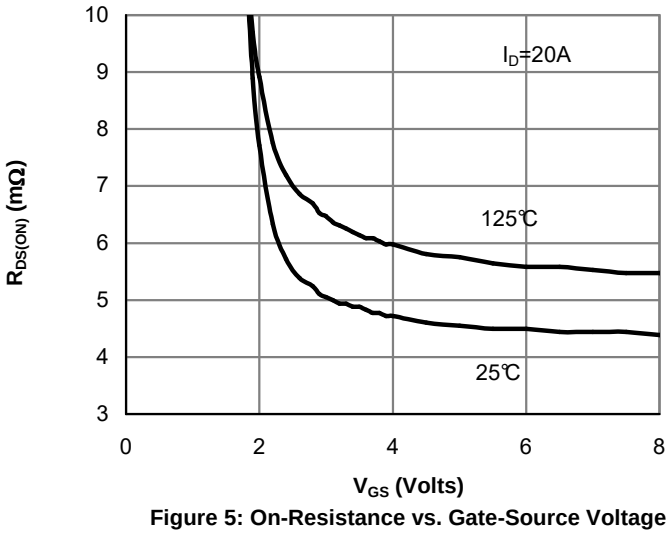


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

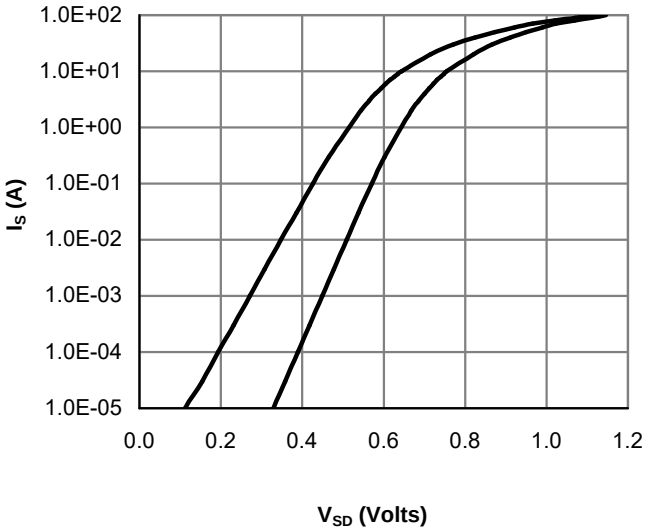


Figure 6: Body-Diode Characteristics (Note E)

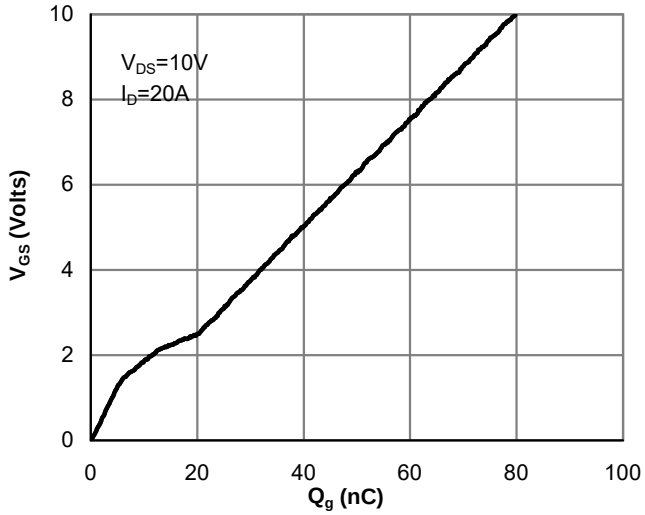


Figure 7: Gate-Charge Characteristics

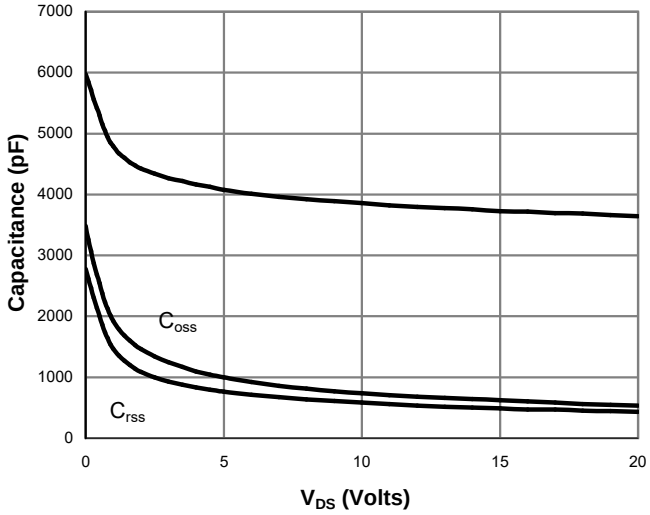


Figure 8: Capacitance Characteristics

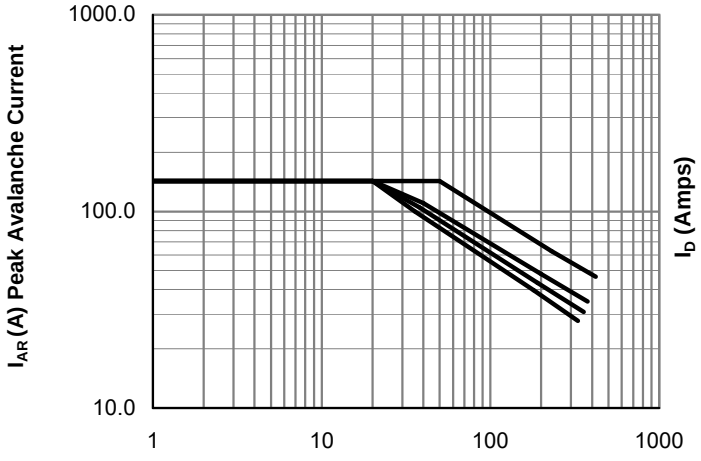
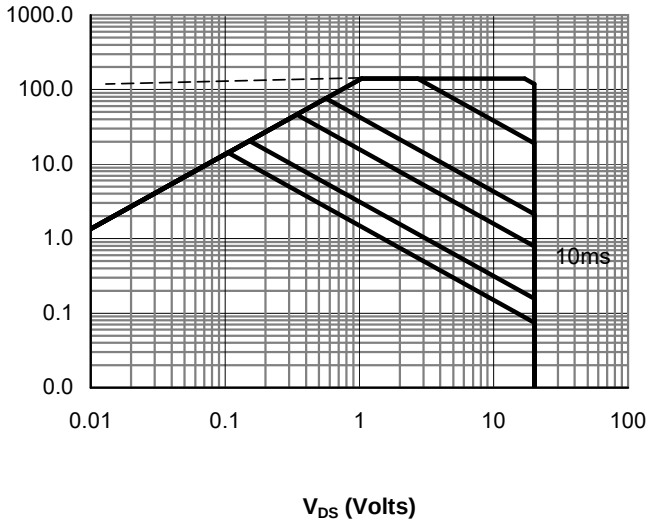


Figure 9: Single Pulse Avalanche capability (Note C)



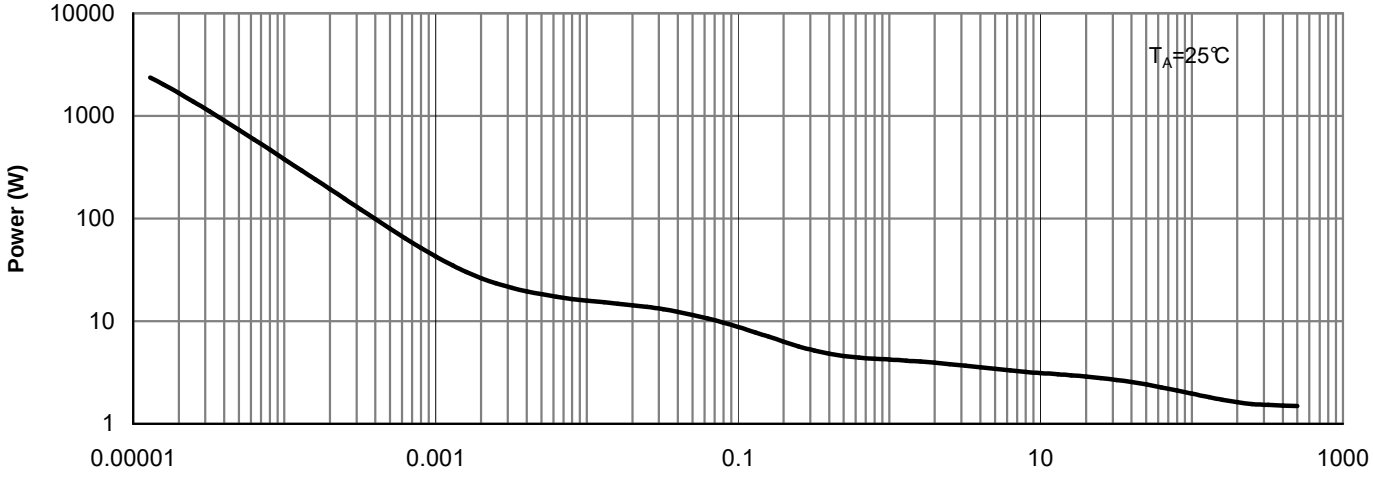


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

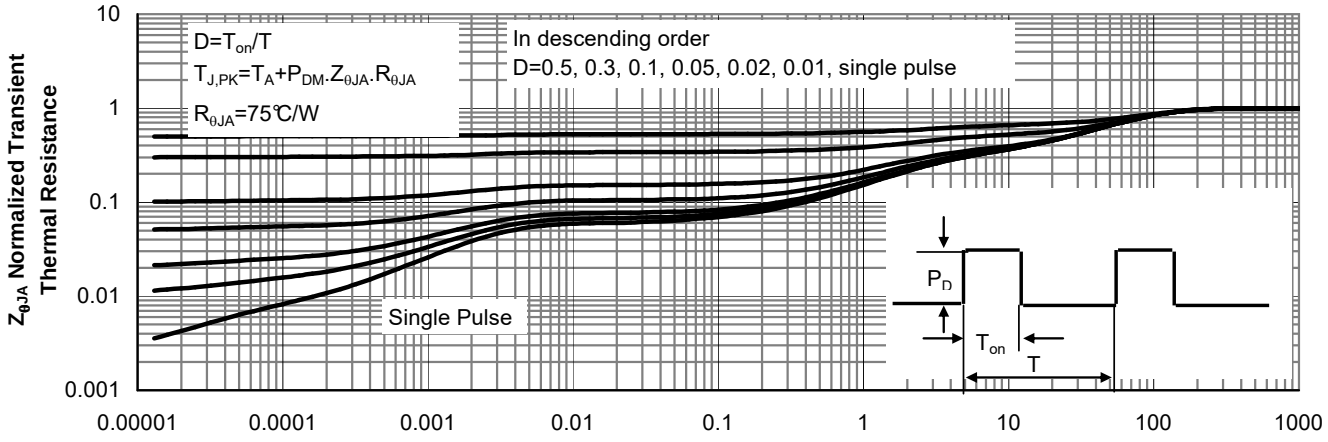
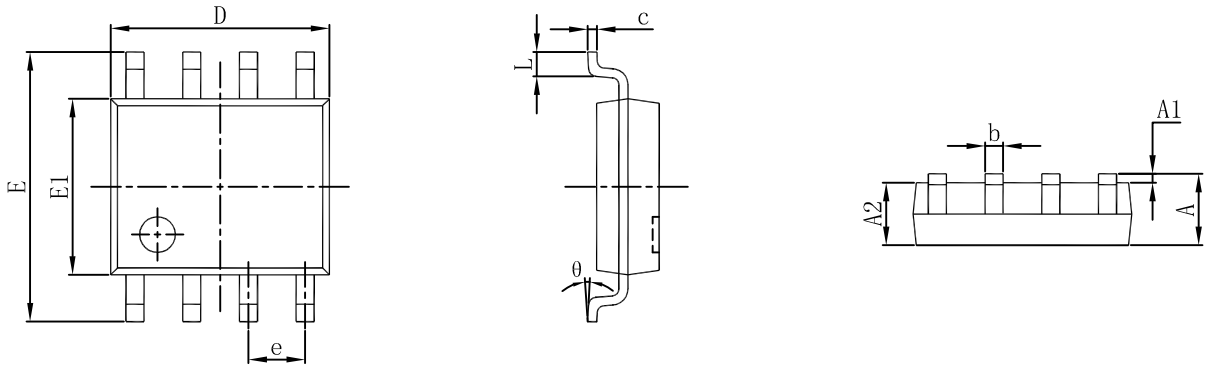
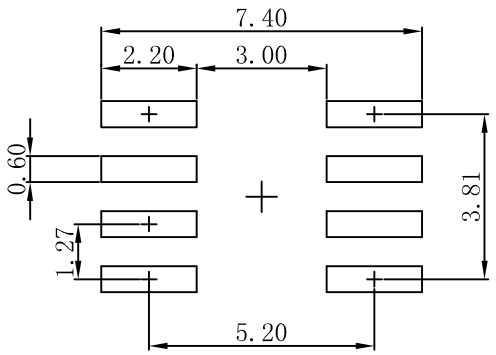


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

SOP-8(SO-8) Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

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