TPCA8021-H(TE12LQM-VB Datasheet

N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a, e]	Q_g (Typ)
30	0.007 at V_{GS} = 10 V	80	31 nC
	0.009 at V_{GS} = 4.5 V	60	

FEATURES

- Trench Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2011/65/EU

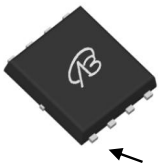
RoHS COMPLIANT

APPLICATIONS

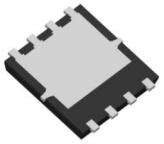
- OR-ing
- Server
- DC/DC

DFN5X6

Top View

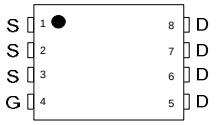


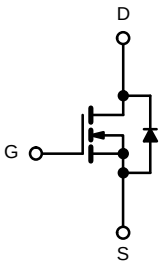
Bottom View



PIN1

Top View





N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)					
Parameter		**Symbol**	**Limit**		**Unit**
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current (T_J = 175 °C)	T_C = 25 °C	I_D	80		A
	T_C = 70 °C		60		
	T_A = 25 °C		50[b, c]		
	T_A = 70 °C		45[b, c]		
Pulsed Drain Current		I_{DM}	210		
Avalanche Current Pulse	L = 0.1 mH	I_{AS}	60		
Single Pulse Avalanche Energy		E_{AS}	95		mJ
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	80		A
	T_A = 25 °C		60		
Maximum Power Dissipation	T_C = 25 °C	P_D	155		W
	T_C = 70 °C		105		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175		°C
THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typ.**	**Max.**	**Unit**
Maximum Junction-to-Ambient[b, d]	t ≤ 10 sec	R_{thJA}	32	40	°C/W
Maximum Junction-to-Case	Steady State	R_{thJC}	0.5	0.6	

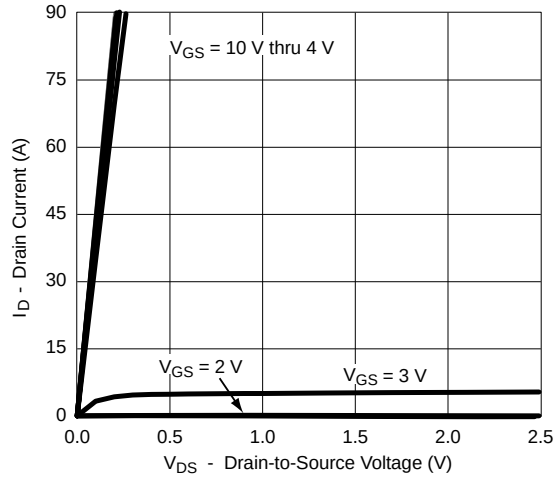
Notes:
a. Based on T_C = 25 °C.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 sec.
d. Maximum under steady state conditions is 90 °C/W.
e. Calculated based on maximum junction temperature. Package limitation current is 90 A.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		35		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 7.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	0.5		2.0	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	60			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 30.8 A		0.007		Ω
		V_{GS} = 4.5 V, I_D = 27 A		0.009		
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 30.8 A		160		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz			1180	pF
Output Capacitance	C_{oss}				425	
Reverse Transfer Capacitance	C_{rss}				170	
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 30.8 A			61	nC
		V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 27.8 A			31.5	
Gate-Source Charge	Q_{gs}				10	
Gate-Drain Charge	Q_{gd}				6	
Gate Resistance	R_g	f = 1 MHz		1.4	2.1	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 0.625 Ω I_D ≅ 24 A, V_{GEN} = 10 V, R_g = 1 Ω		18	27	ns
Rise Time	t_r			11	17	
Turn-Off Delay Time	$t_{d(off)}$			70	105	
Fall Time	t_f			10	15	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 0.67 Ω I_D ≅ 22.5 A, V_{GEN} = 4.5 V, R_g = 1 Ω		55	83	
Rise Time	t_r			180	270	
Turn-Off Delay Time	$t_{d(off)}$			55	83	
Fall Time	t_f			12	18	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C		60		A
Pulse Diode Forward Current[a]	I_{SM}			210		
Body Diode Voltage	V_{SD}	I_S = 22 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 20 A, di/dt = 100 A/µs, T_J = 25 °C		52	78	ns
Body Diode Reverse Recovery Charge	Q_{rr}			70.2	105	nC
Reverse Recovery Fall Time	t_a			27		ns
Reverse Recovery Rise Time	t_b			25		

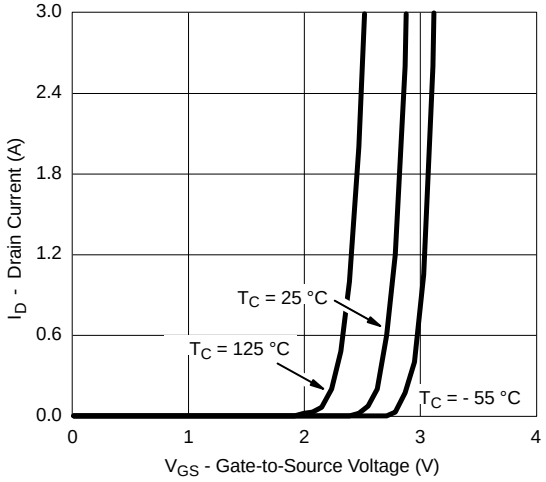
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

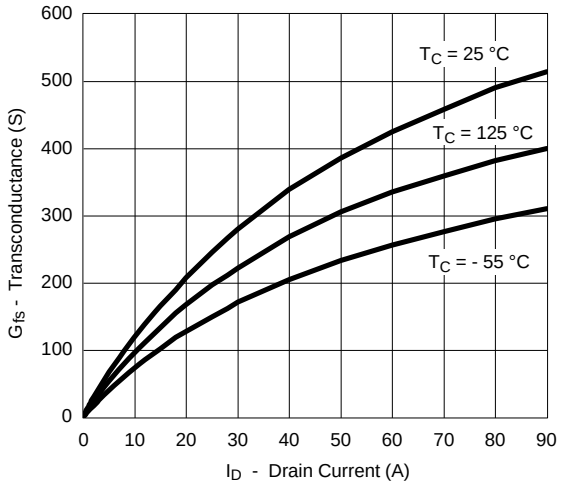
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



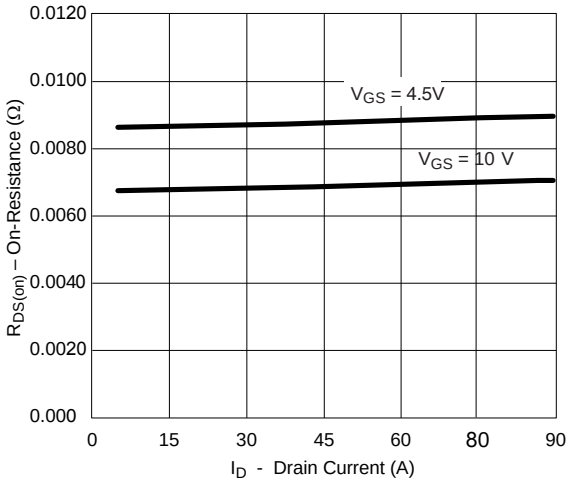
Output Characteristics



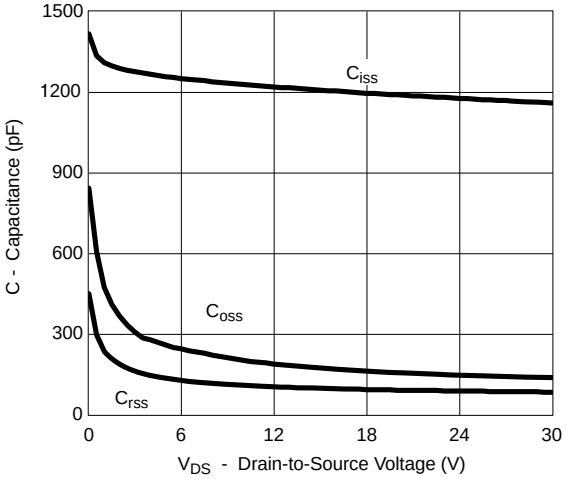
Transfer Characteristics



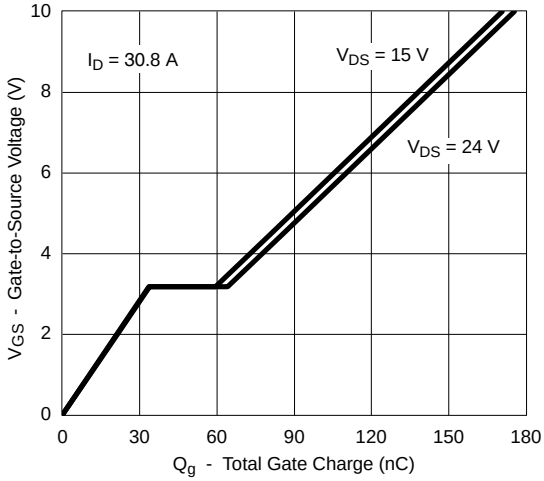
Transconductance



$R_{DS(on)}$ vs. Drain Current

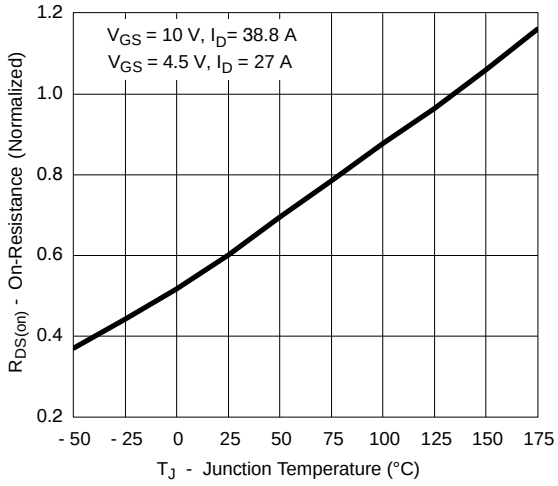


Capacitance

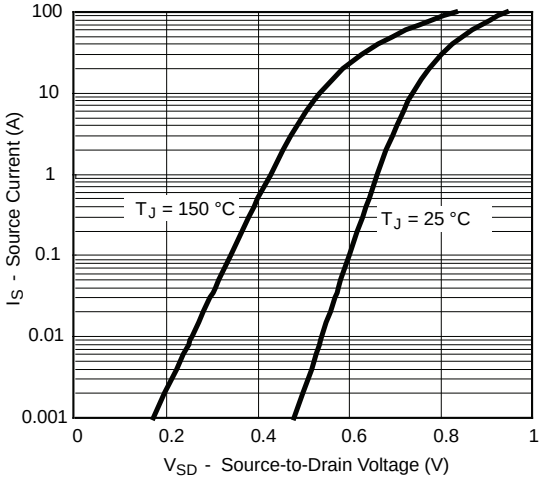


Gate Charge

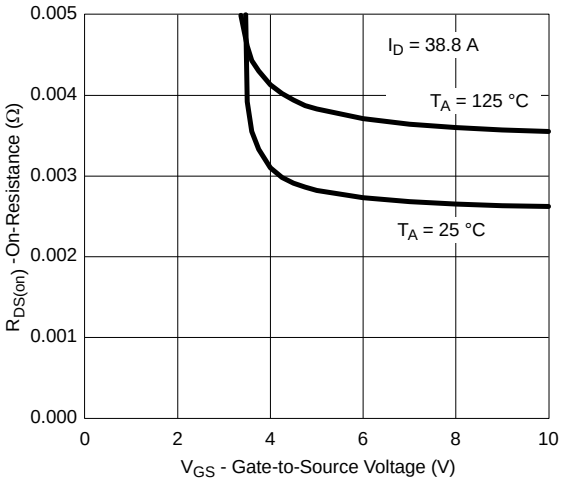
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



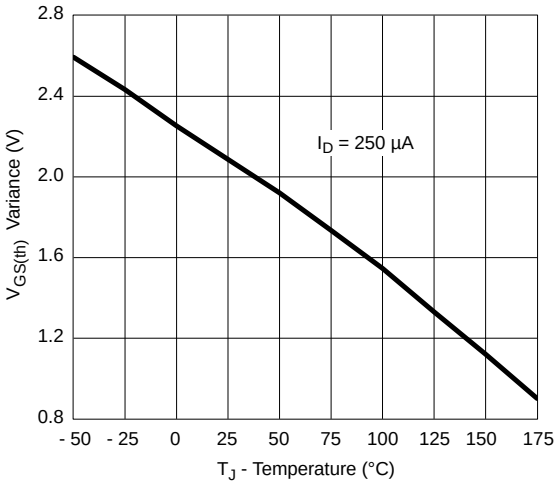
On-Resistance vs. Junction Temperature



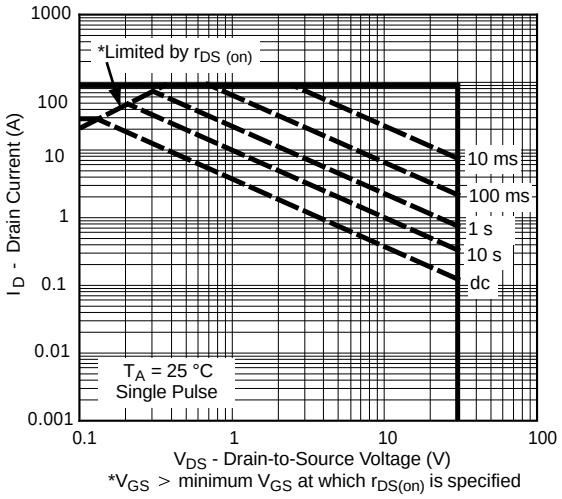
Forward Diode Voltage vs. Temperature



$R_{DS(on)}$ vs. V_{GS} vs. Temperature

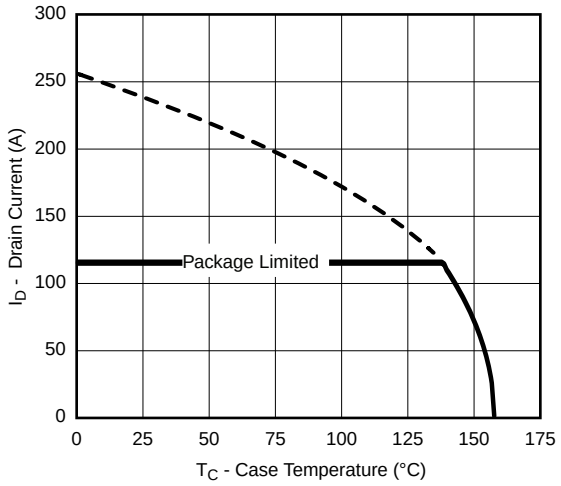


Threshold Voltage

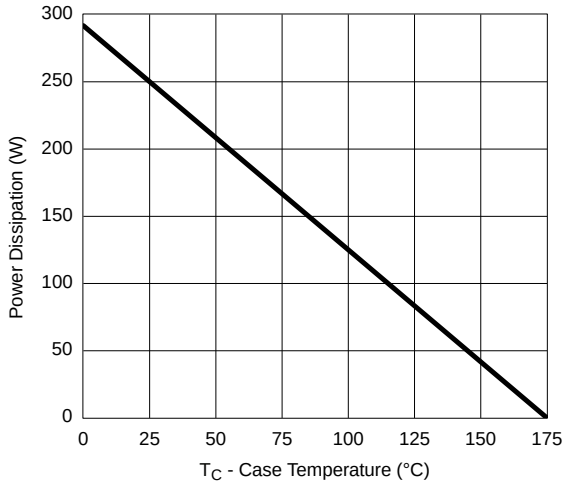


Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

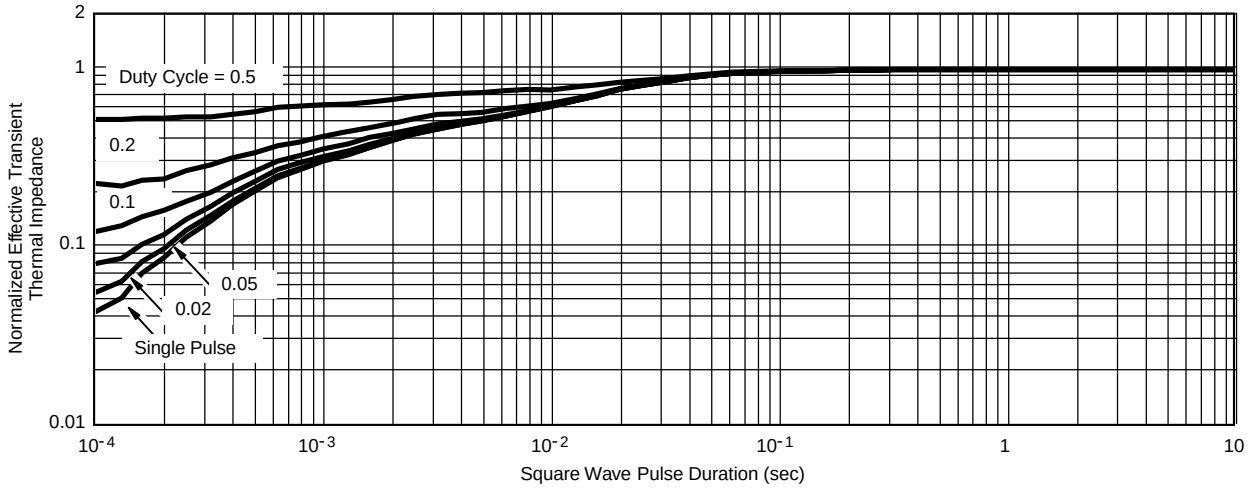


Current Derating*



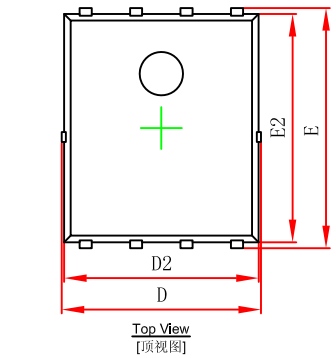
Power Derating

*The power dissipation P_D is based on $T_{J(max)}$ = 175 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

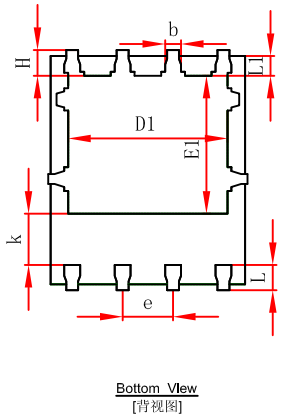


Normalized Thermal Transient Impedance, Junction-to-Case

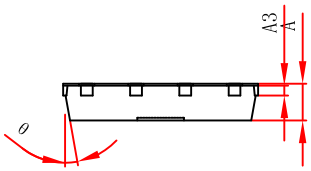
PDFNWB5x6-8L Package Outline Dimensions



Top View
[顶视图]



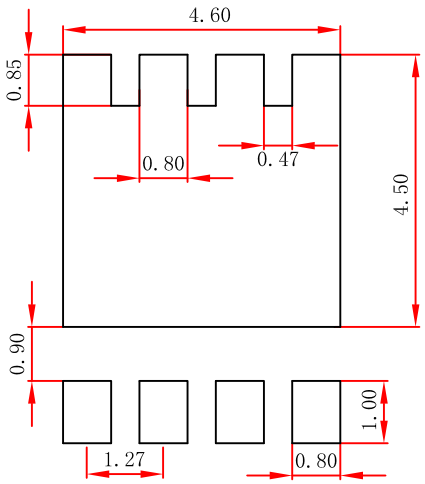
Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

PDFNWB5x6-8L Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

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