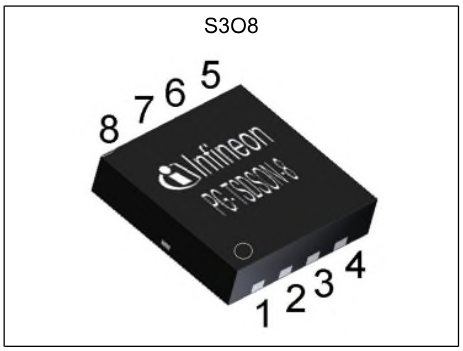
MOSFET

OptiMOS™ 3 Power-Transistor, 60 V



Features

- Ideal for high frequency switching and sync. rec.
- Optimized technology for DC/DC converters
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC[1] for target applications
- Halogen-free according to IEC61249-2-21

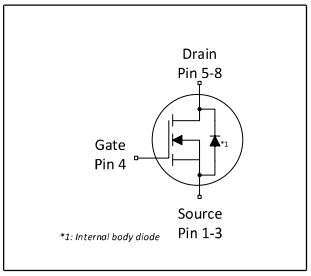


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	11	mΩ
I_D	53	A

Type / Ordering Code	Package	Marking	Related Links
BSZ110N06NS3 G	PG-TSDSON-8	110N06N	-

[1] J-STD20 and JESD22

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1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - -	- - -	53 33 11	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_C=25 °C, R_{thJA} =60 K/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	212	A	T_C=25 °C
Avalanche energy, single pulse[4]	E_{AS}	-	-	55	mJ	I_D=20 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	50 2.1	W	T_C=25 °C T_A=25 °C, R_{thJA}=60 K/W[2]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2.5	K/W	-
Device on PCB, 6 cm² cooling area[2]	R_{thJA}	-	-	60	K/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2	3	4	V	V_{DS}=V_{GS}, I_D=23 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	8.8	11	mΩ	V_{GS}=10 V, I_D=20 A
Gate resistance	R_G	-	1.3	-	Ω	-
Transconductance	g_{fs}	16	32	-	S	|V_{DS}|>2|I_D|$R_{DS(on)max}$, I_D=20 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	2000	2700	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	440	590	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	17	-	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	10	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=20 A, R_G=3 Ω
Rise time	t_r	-	77	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=20 A, R_G=3 Ω
Turn-off delay time	$t_{d(off)}$	-	14	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=20 A, R_G=3 Ω
Fall time	t_f	-	6	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=20 A, R_G=3 Ω

Table 6 Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	10	-	nC	V_{DD}=30 V, I_D=20 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	6	-	nC	V_{DD}=30 V, I_D=20 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	2	-	nC	V_{DD}=30 V, I_D=20 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	7	-	nC	V_{DD}=30 V, I_D=20 A, V_{GS}=0 to 10 V
Gate charge total[1)]	Q_g	-	25	33	nC	V_{DD}=30 V, I_D=20 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	5.2	-	V	V_{DD}=30 V, I_D=20 A, V_{GS}=0 to 10 V
Output charge[1)]	Q_{oss}	-	20	27	-	V_{DD}=30 V, V_{GS}=0 V

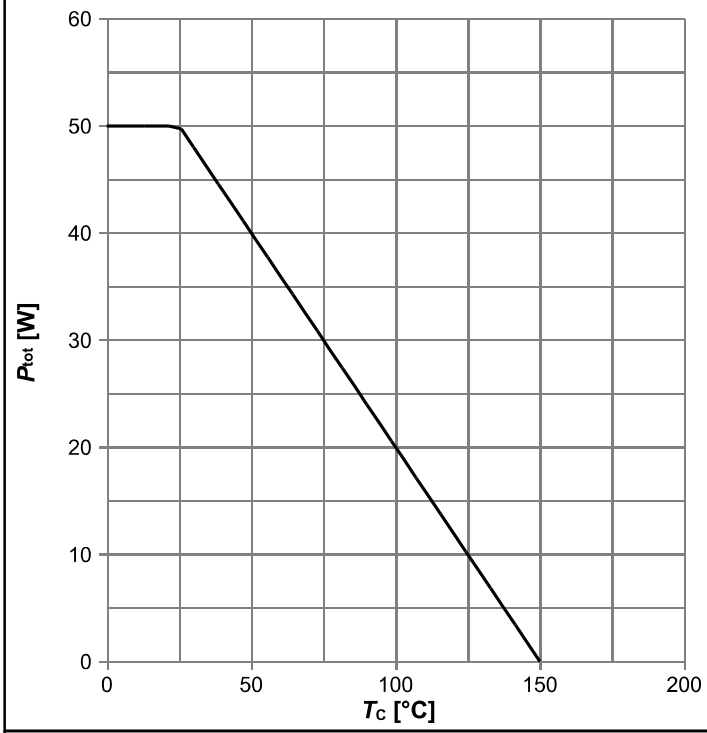
[1)] Defined by design. Not subject to production test
[2)] See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	38	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	212	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.9	1.2	V	V_{GS}=0 V, I_F=20 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	28	-	ns	V_R=30 V, I_F=20A, di_F/dt=100 A/µs
Reverse recovery charge	Q_{rr}	-	22	-	nC	V_R=30 V, I_F=20A, di_F/dt=100 A/µs

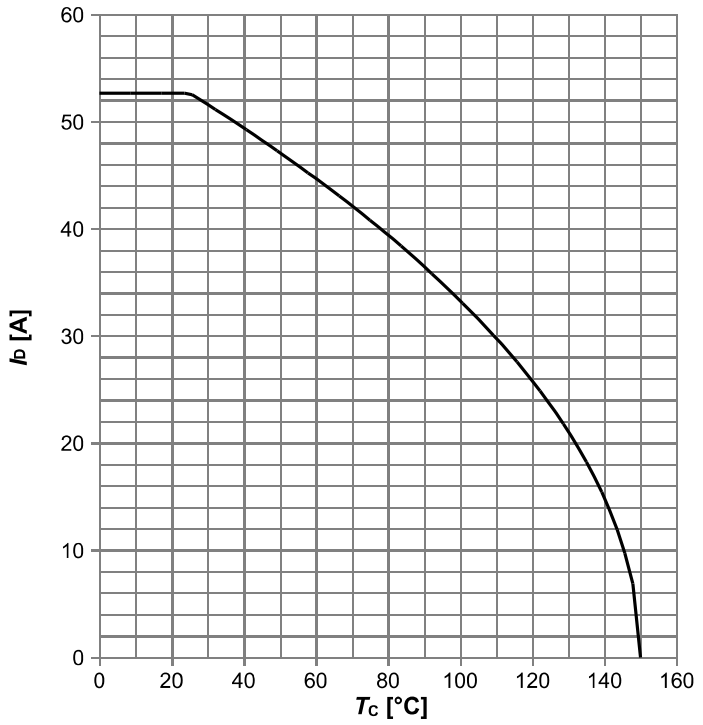
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



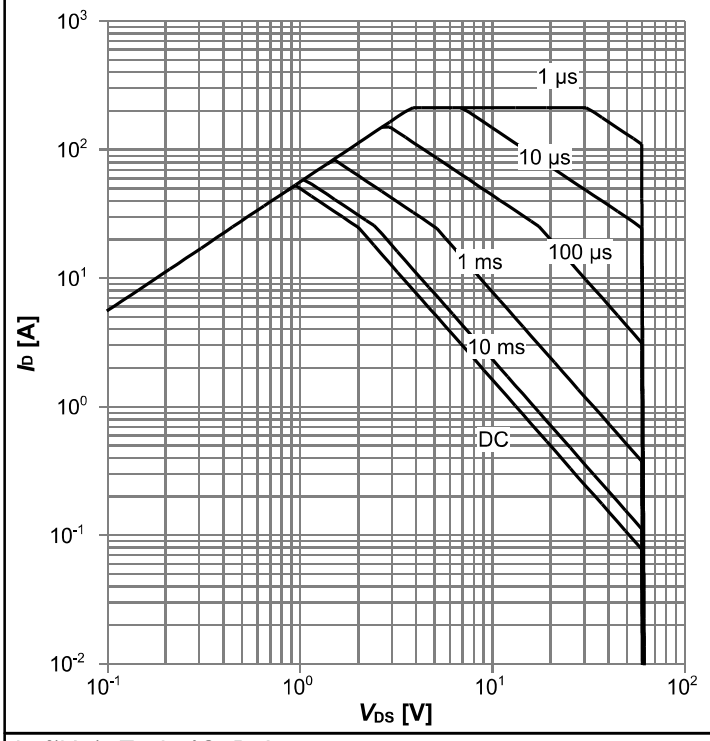
$P_{tot}=f(T_C)$

Diagram 2: Drain current



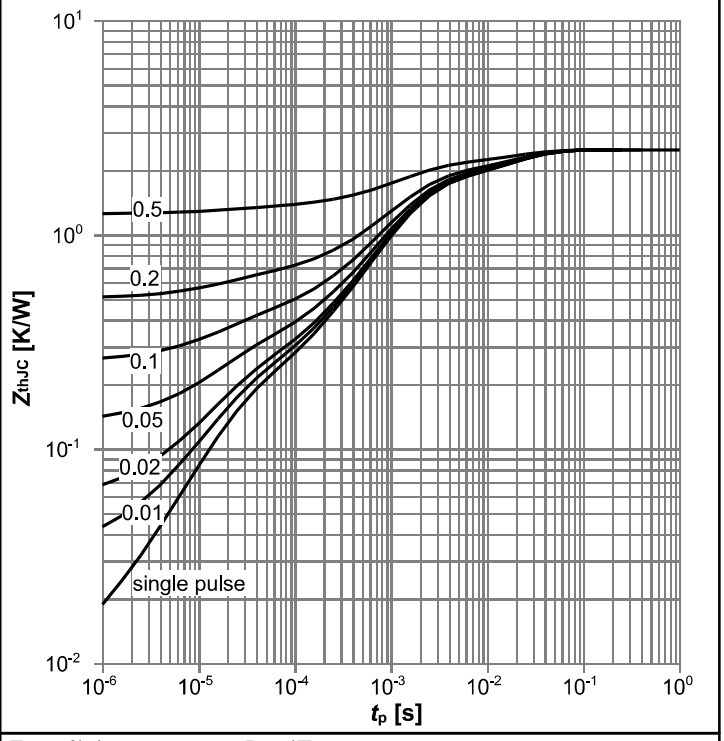
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



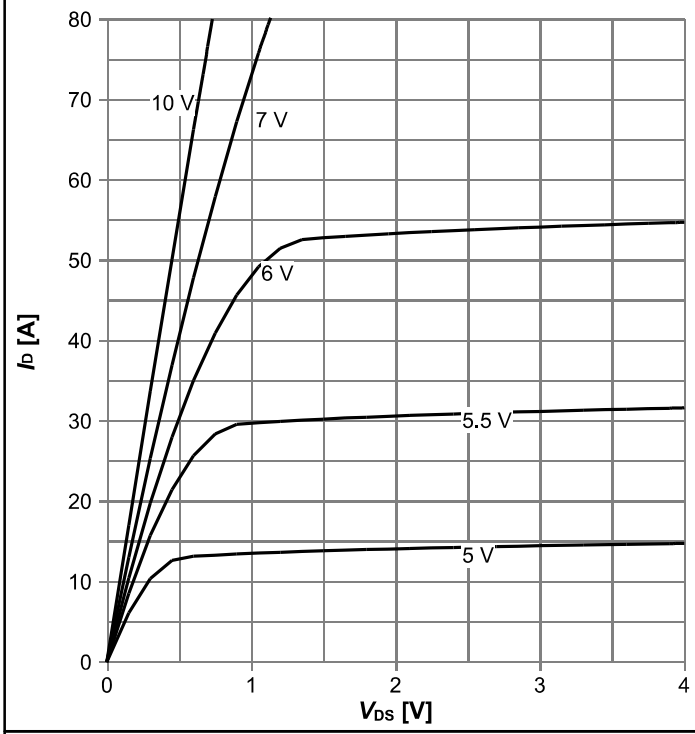
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



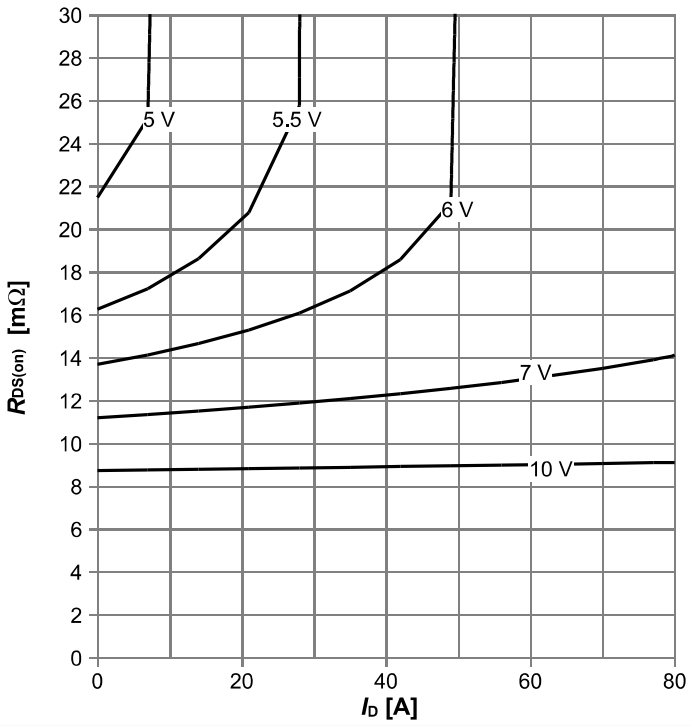
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



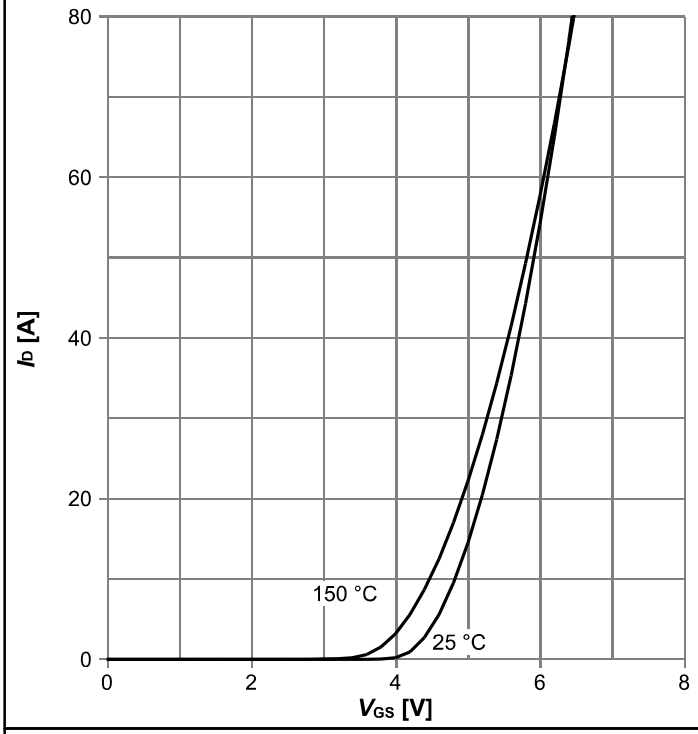
$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



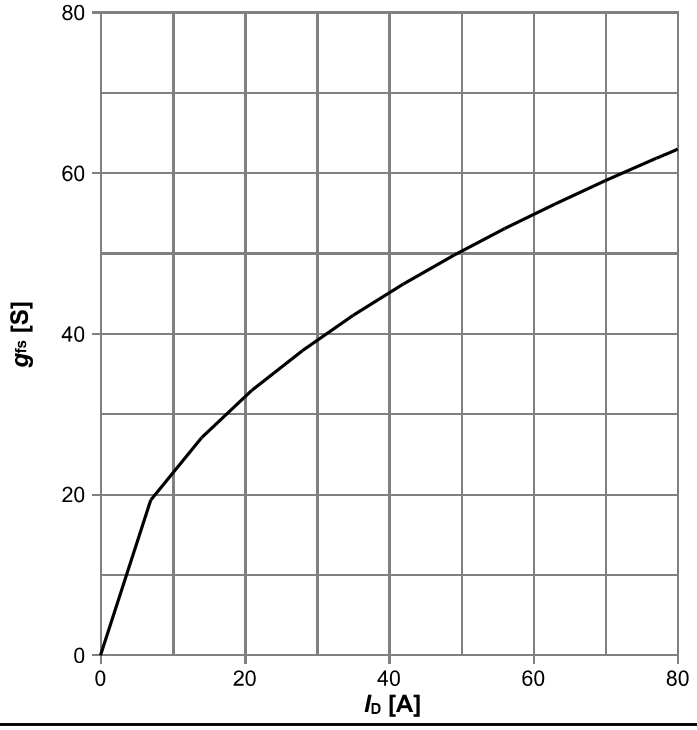
$R_{DS(on)}=f(I_D)$; $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



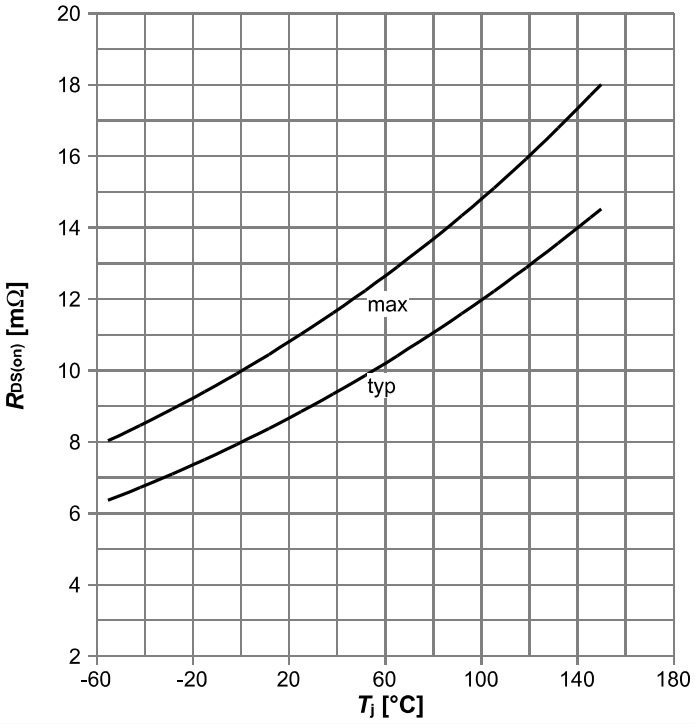
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



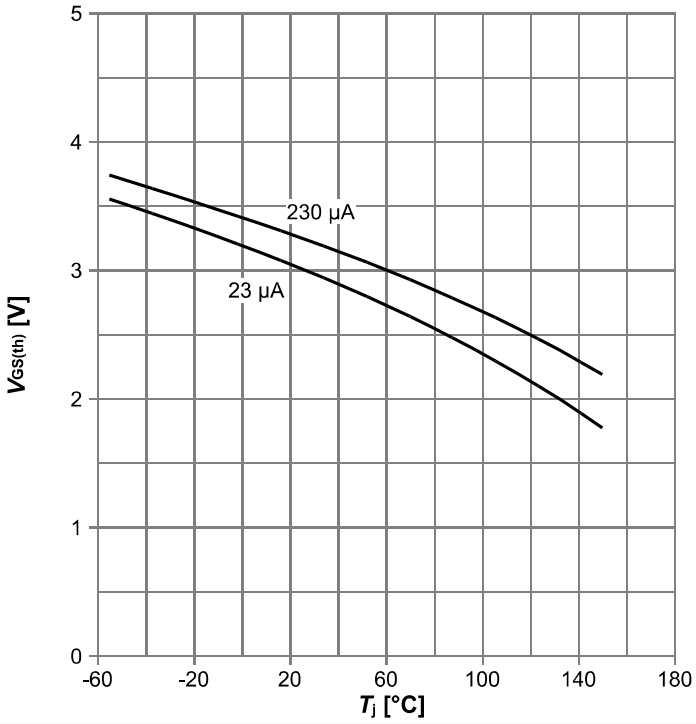
$g_{fs}=f(I_D)$; $T_j=25$ °C

Diagram 9: Drain-source on-state resistance



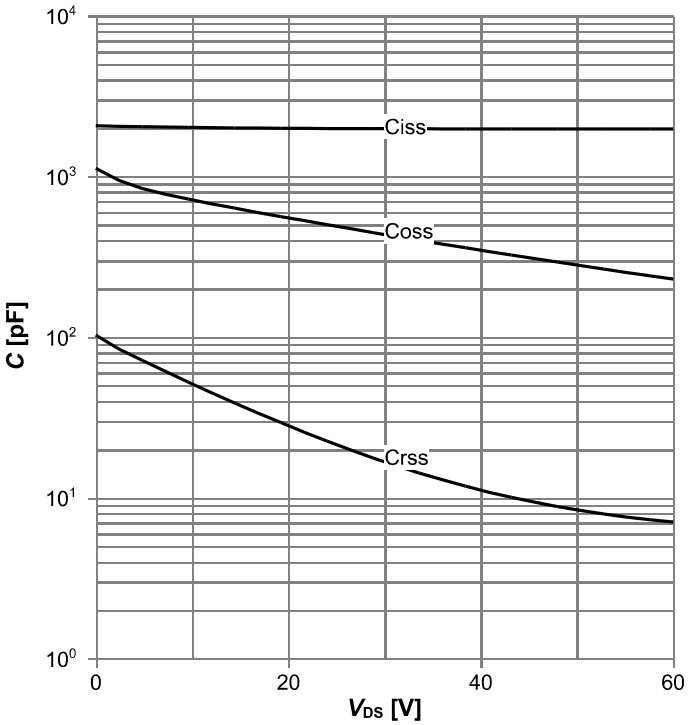
$R_{DS(on)}=f(T_j)$; I_D=20 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



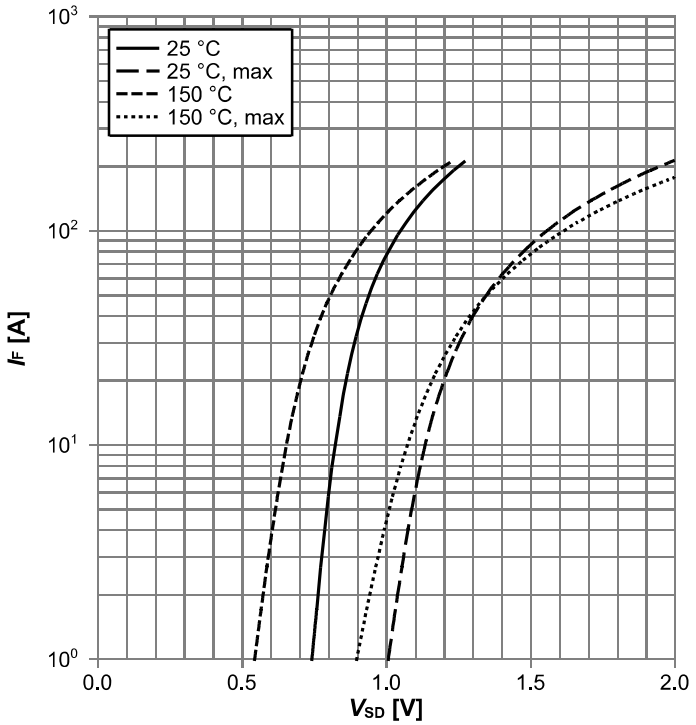
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; parameter I_D

Diagram 11: Typ. capacitances



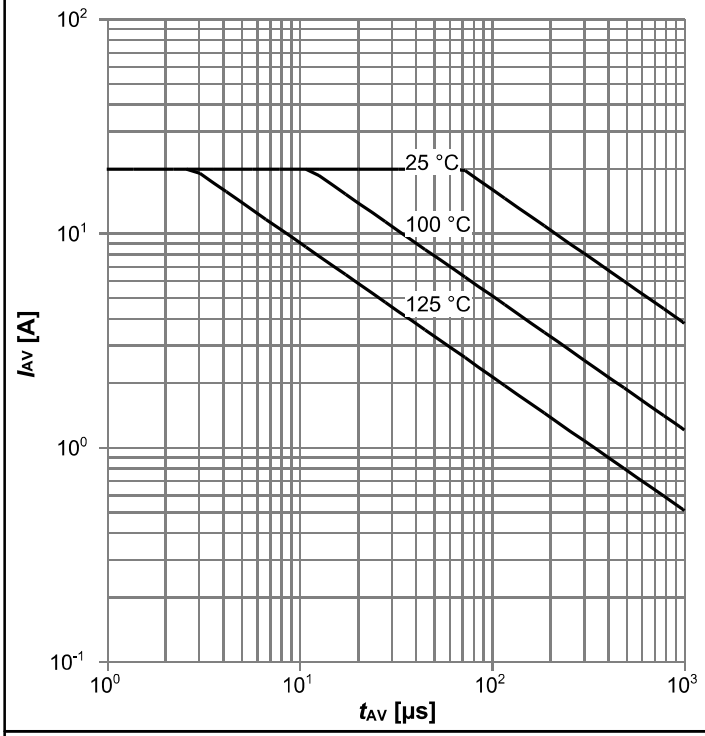
$C=f(V_{DS})$; V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



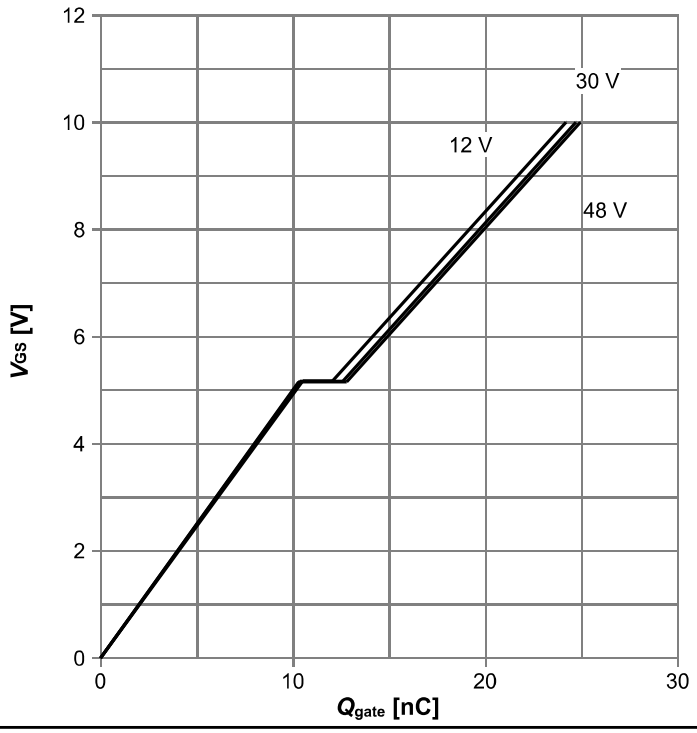
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



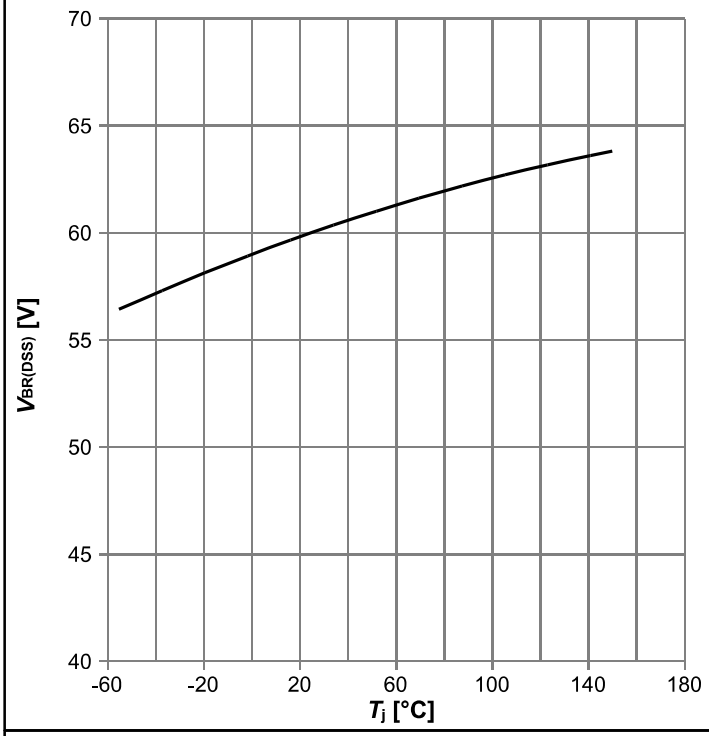
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



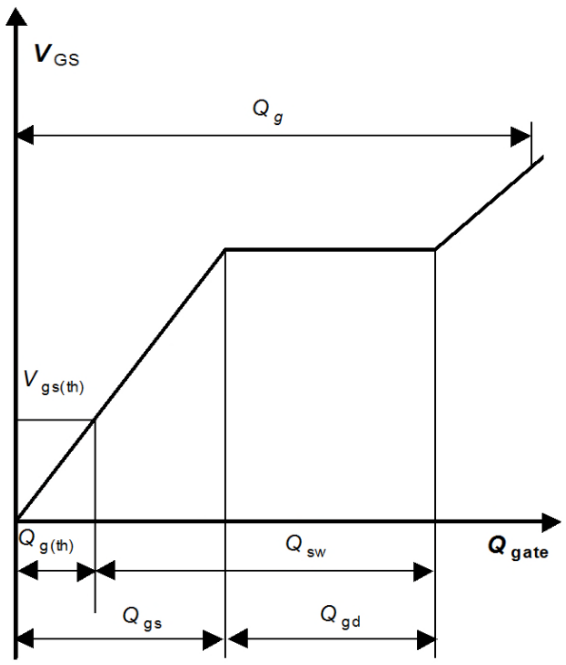
$V_{GS}=f(Q_{gate})$; $I_D=20$ A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

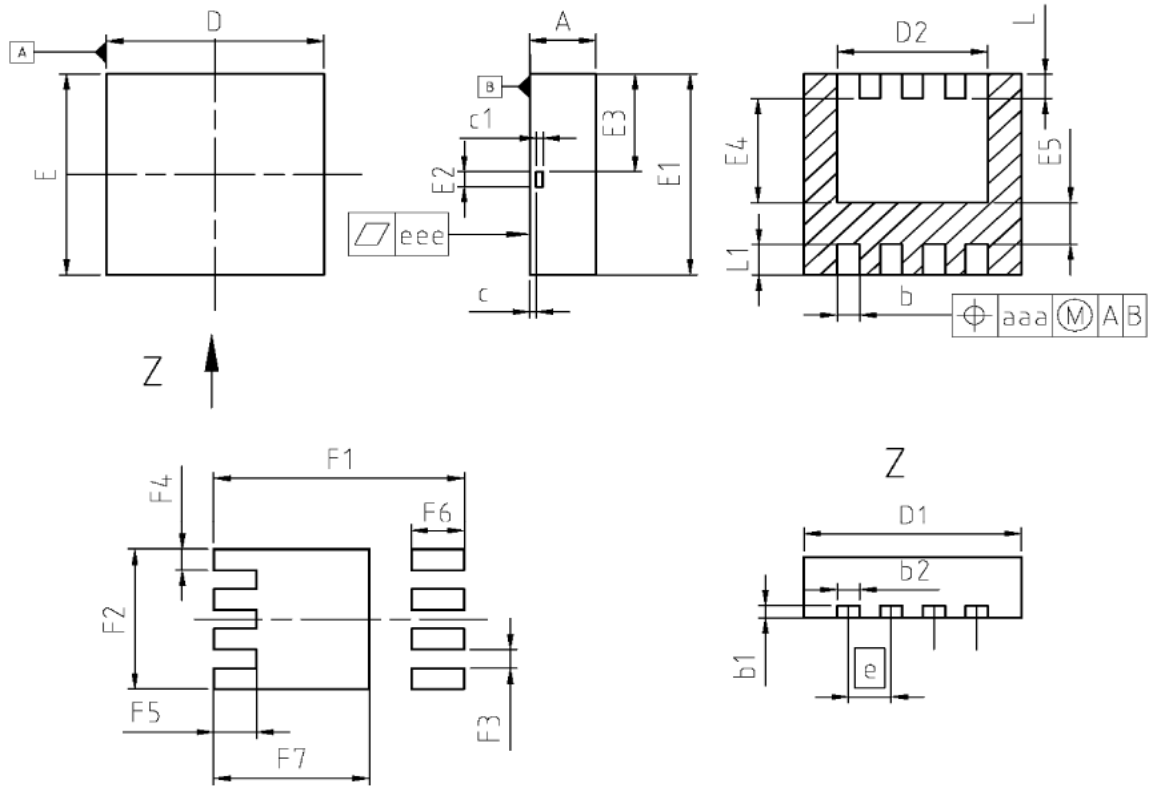


$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

Diagram Gate charge waveforms



5 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.95	1.00	0.037	0.039
b	0.25	0.35	0.010	0.014
b1	0.10	0.30	0.004	0.012
b2	0.20	0.40	0.008	0.016
c	0.00	0.20	0.000	0.008
D=D1	3.20	3.40	0.126	0.134
D2	2.15	2.35	0.085	0.093
E=E1	3.20	3.40	0.126	0.134
E2	0.10	0.30	0.004	0.012
E3	1.35	1.55	0.053	0.061
E4	1.60	1.80	0.063	0.071
E5	0.66	0.86	0.026	0.034
e	0.60	0.70	0.024	0.028
N	8		8	
L	0.31	0.51	0.012	0.020
L1	0.33	0.53	0.013	0.021
aaa	0.25		0.010	
eee	0.05		0.002	
F1	3.70	3.90	0.146	0.154
F2	2.19	2.39	0.086	0.094
F3	0.21	0.41	0.008	0.016
F4	0.24	0.44	0.009	0.017
F5	0.55	0.75	0.022	0.030
F6	0.70	0.90	0.028	0.035
F7	2.26	2.46	0.089	0.097

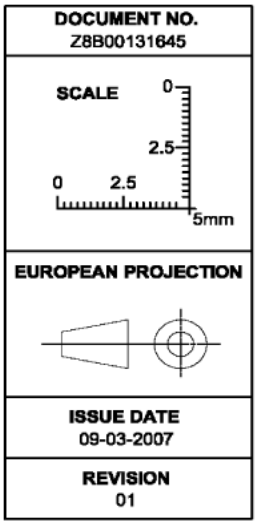


Figure 1 Outline PG-TSDSON-8, dimensions in mm/inches

Revision History

BSZ110N06NS3 G

Revision: 2021-10-25, Rev. 2.5

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.5	2021-10-25	Update current rating and footnotes

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