FDWS9508L_F085-VB Datasheet

P-Channel 40-V (D-S) MOSFET

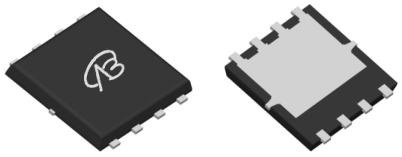
PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 40	0.003 at V_{GS} = - 10 V	- 150	205 nC

FEATURES

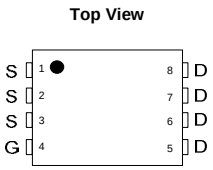
- Trench Power MOSFET

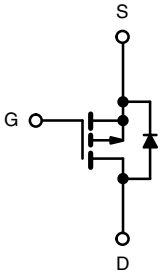
RoHS COMPLIANT

DFN5X6



Top View Bottom View





P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 175 °C)	T_C = 25 °C	I_D	- 150	A
	T_C = 70 °C		- 120[a]	
	T_A = 25 °C		39[b, c]	
	T_A = 70 °C		33[b, c]	
Pulsed Drain Current		I_{DM}	450	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	110	
	T_A = 25 °C		10[b, c]	
Avalanche Current	L = 0.1 mH	I_{AS}	75	
Single-Pulse Avalanche Energy		E_{AS}	281	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	425	W
	T_C = 70 °C		282	
	T_A = 25 °C		15[b, c]	
	T_A = 70 °C		10.5[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C
Soldering Recommendations (Peak Temperature)[d, e]			260	

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b, d]	t ≤ 10 s	R_{thJA}	8	10	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	0.33	0.4	

Notes:
a. Package limited.
b. Surface Mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. Maximum under Steady State conditions is 40 °C/W.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 40			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 40		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 5.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 2	- 3	- 4	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 40 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 40 V, V_{GS} = 0 V, T_J = 55 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = - 10 V	- 120			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = - 10 V, I_D = - 20 A		0.003		Ω
Forward Transconductance[a]	g_{fs}	V_{DS} = - 15 V, I_D = - 20 A		75		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 25 V, V_{GS} = 0 V, f = 1 MHz		8900		pF
Output Capacitance	C_{oss}			1610		
Reverse Transfer Capacitance	C_{rss}			1100		
Total Gate Charge	Q_g	V_{DS} = - 20 V, V_{GS} = - 10 V, I_D = - 110 A		205	315	nC
Gate-Source Charge	Q_{gs}			58		
Gate-Drain Charge	Q_{gd}			52		
Gate Resistance	R_g	f = 1 MHz		4.0		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 20 V, R_L = 0.18 Ω $I_D \cong$ - 110 A, V_{GEN} = - 10 V, R_g = 1 Ω		25	40	ns
Rise Time	t_r			290	440	
Turn-Off Delay Time	$t_{d(off)}$			60	80	
Fall Time	t_f			35	55	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			- 150	A
Pulse Diode Forward Current[a]	I_{SM}				- 450	
Body Diode Voltage	V_{SD}	I_S = - 20 A		- 0.8	- 1.5	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 20 A, di/dt = 100 A/µs, T_J = 25 °C		20	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			130	200	nC
Reverse Recovery Fall Time	t_a			37		ns
Reverse Recovery Rise Time	t_b			33		

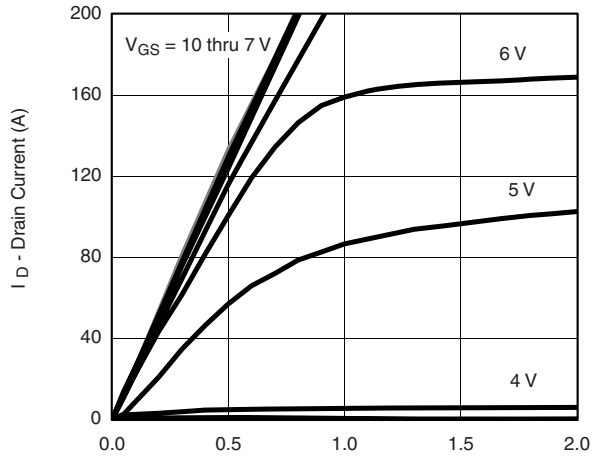
Notes:

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

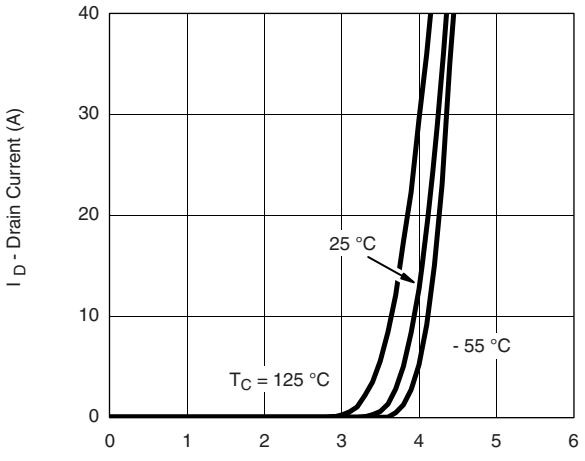
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

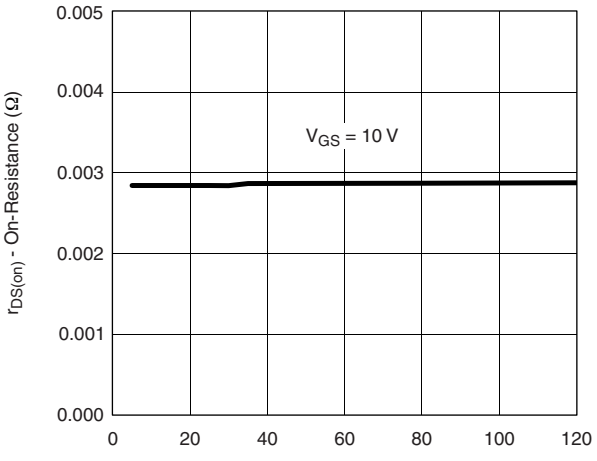
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



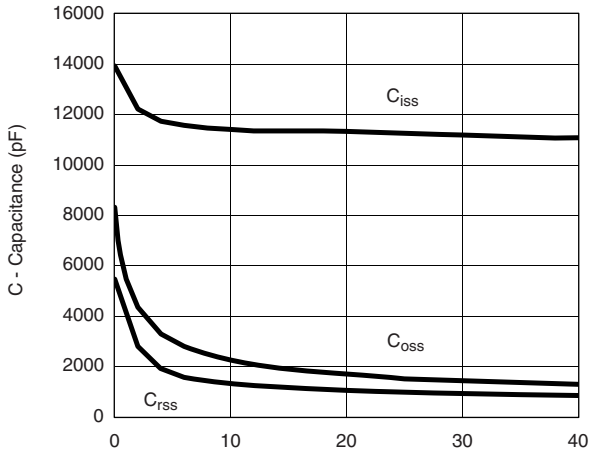
Output Characteristics



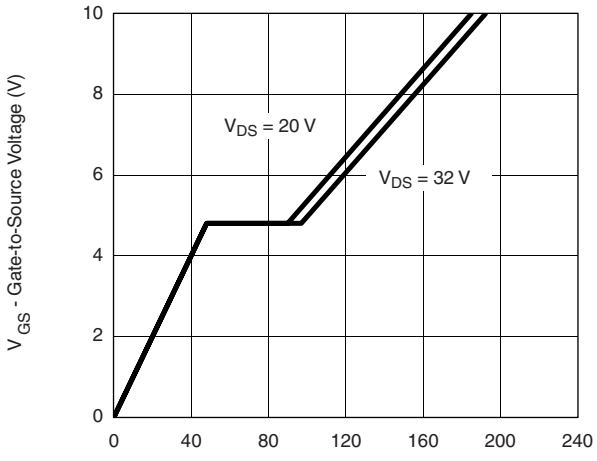
Transfer Characteristics



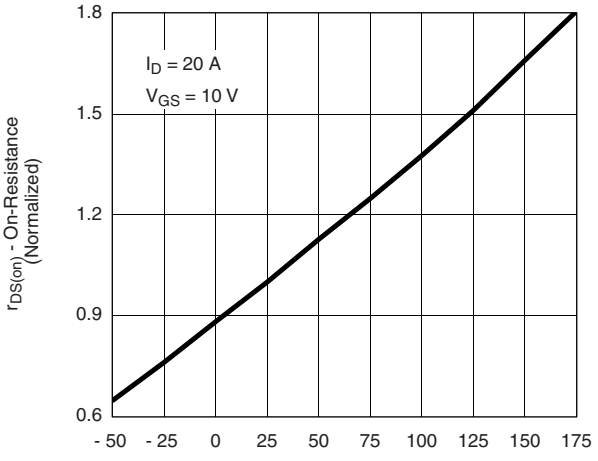
On-Resistance vs. Drain Current



Capacitance

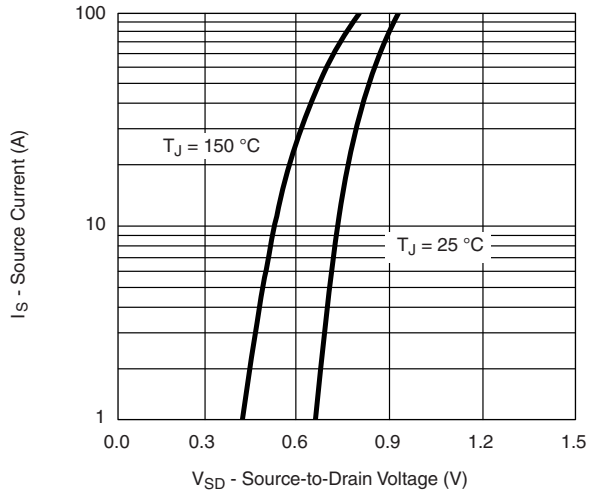


Gate Charge

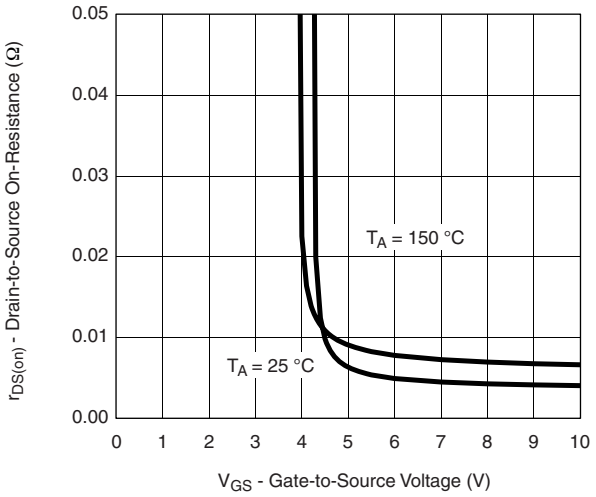


On-Resistance vs. Junction Temperature

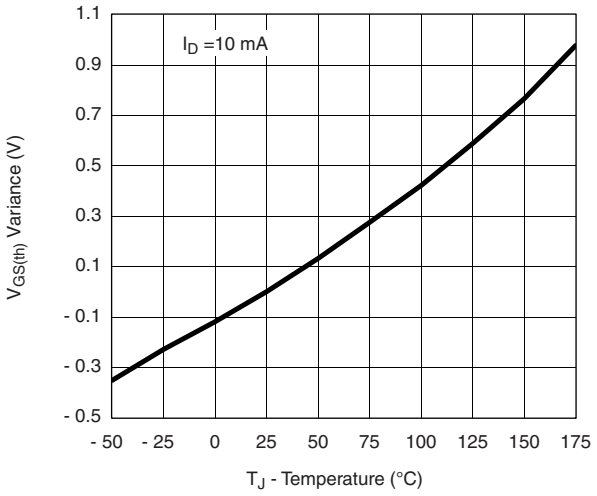
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



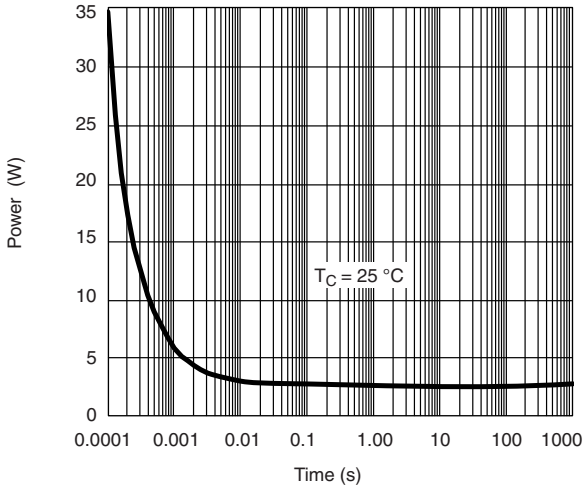
Source-Drain Diode Forward Voltage



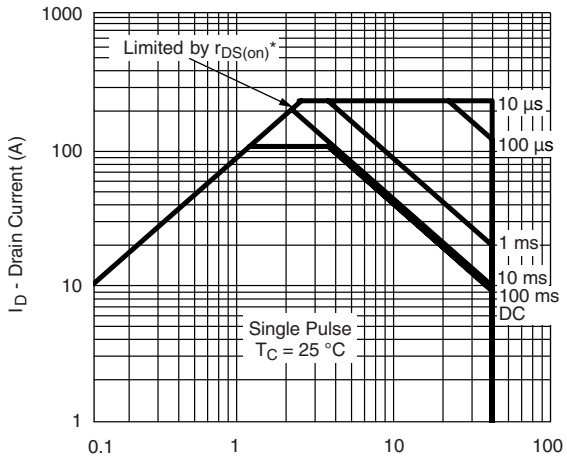
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



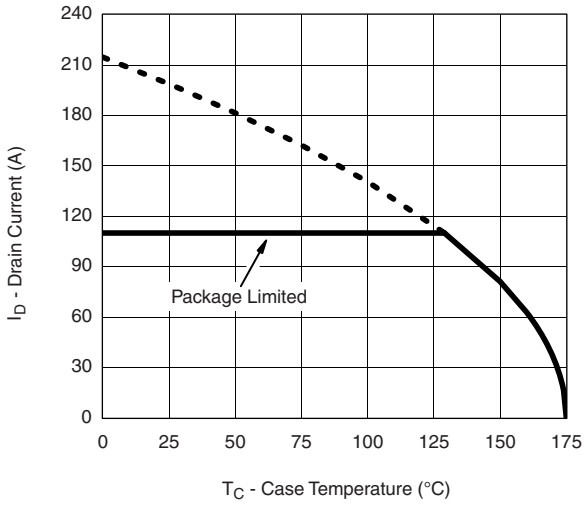
Single Pulse Power, Junction-to-Ambient



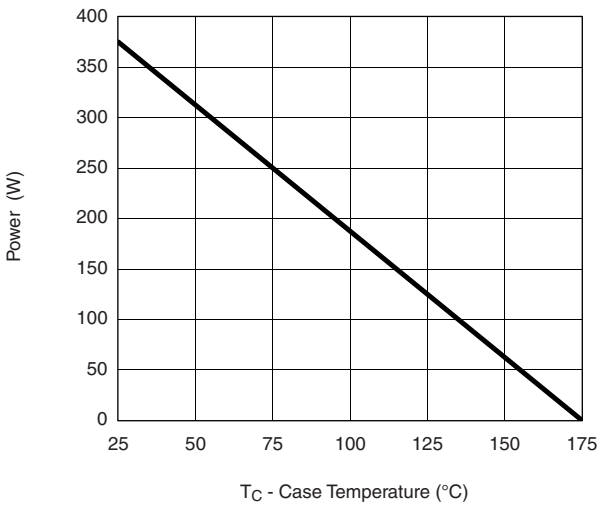
*V_{GS} > minimum V_{GS} at which $r_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case

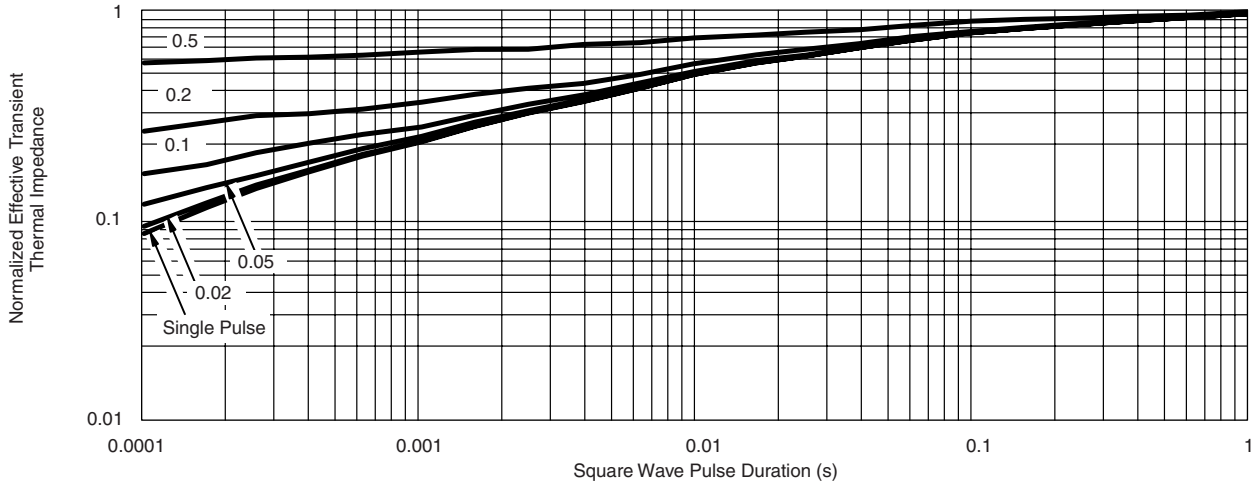
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Max. Avalanche and Drain Current vs. Case Temperature*



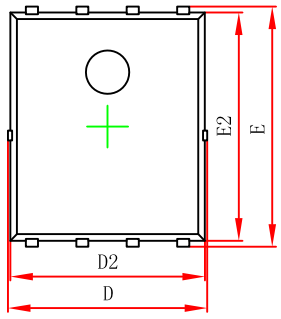
Power Derating, Junction-to-Case



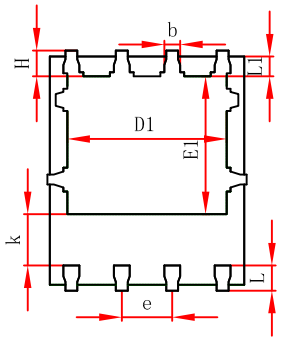
Normalized Thermal Transient Impedance, Junction-to-Case

* The power dissipation P_D is based on $T_{J(max)}$ = 175 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

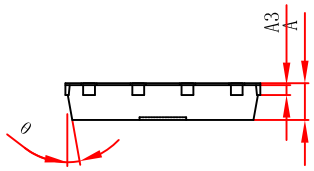
PDFNWB5x6-8L Package Outline Dimensions



Top View
[顶视图]



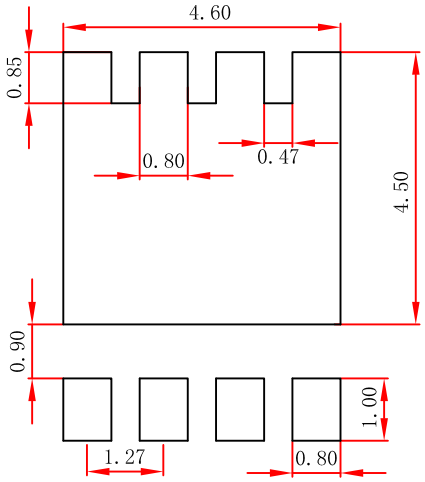
Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

PDFNWB5x6-8L Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

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