74LVC543A

Octal D-type registered transceiver; 3-state

Rev. 8 — 18 December 2012 Product data sheet

1. General description

The 74LVC543A is an octal registered transceiver containing two sets of D-type latches for temporary storage of the data flow in either direction. Separate latch enable inputs (pins $\overline{LEAB}$ and $\overline{LEBA}$) and output enable inputs (pins $\overline{OEAB}$ and $\overline{OEBA}$), are provided for each register. The separate inputs permit independent control of input and output in either direction of the data flow.

The 74LVC543A contains eight D-type latches, with separate inputs and controls for each set. For data flow from pins A to B, the A to B enable input (pin $\overline{EAB}$) must be LOW. The LOW state enables data entry from pins A0 to A7 or from pins B0 to B7, as indicated in Table 3. With pin $\overline{EAB}$ LOW, a LOW signal on the A to B latch enable input (pin $\overline{LEAB}$) makes the A to B latches transparent. A subsequent LOW-to-HIGH transition on pin $\overline{LEAB}$ puts the A data into the latches where it is stored. The B outputs no longer change with the A inputs. With pins $\overline{EAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and display the data present at the outputs of the A latches.

2. Features and benefits

- 5 V tolerant inputs/ouputs for interfacing with 5 V logic
- Supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- 8-bit positive transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 3-state non-inverting outputs for bus-oriented applications
- High-impedance when V_{CC} = 0 V
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Specified from −40 °C to +85 °C and −40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC543AD	–40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74LVC543ADB	–40 °C to +125 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74LVC543APW	–40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74LVC543ABQ	–40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1

4. Functional diagram

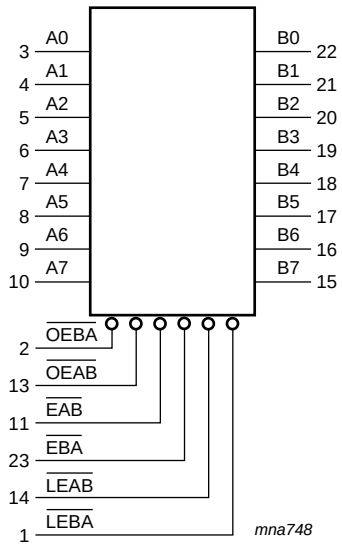


Fig 1. Logic diagram

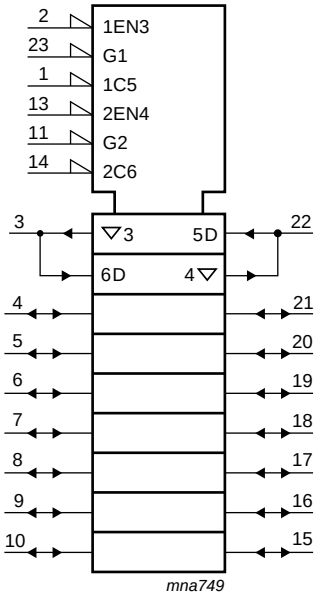


Fig 2. IEC logic symbol

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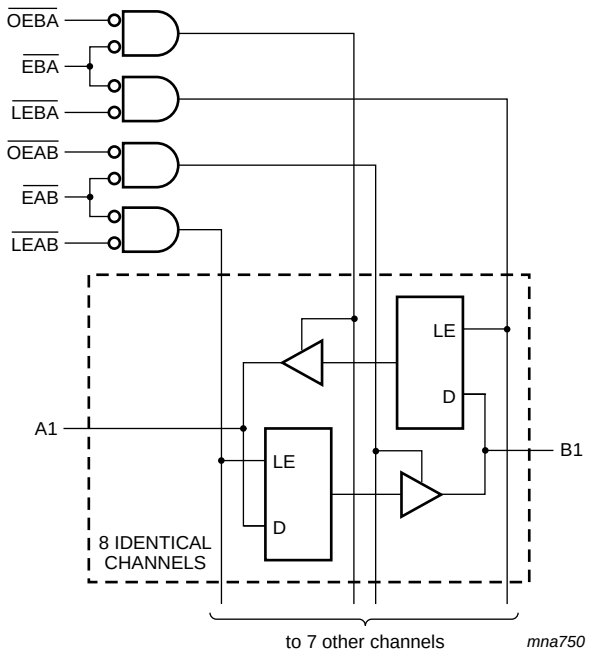


Fig 3. Logic diagram

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5. Pinning information

5.1 Pinning

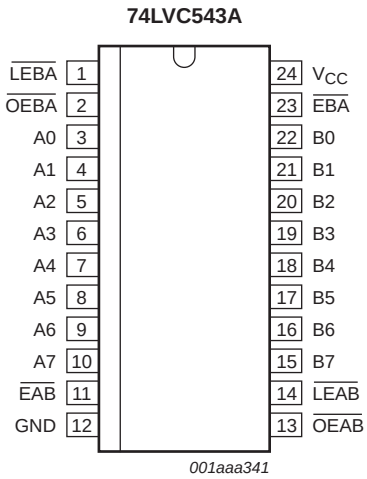
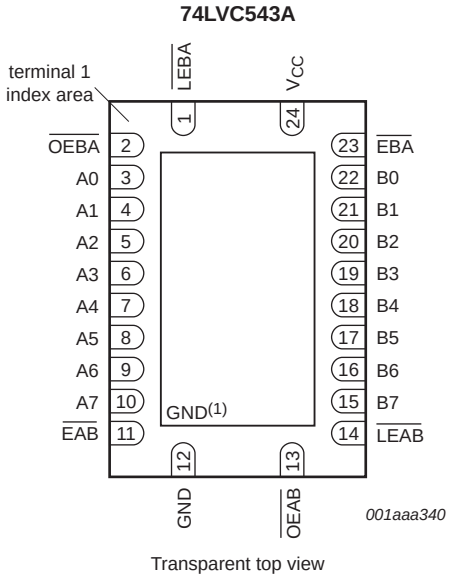


Fig 4. Pin configuration for SO24 and (T)SSOP24



Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 5. Pin configuration for DHVQFN24

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{LEBA}$	1	B to A latch enable input (active LOW)
$\overline{LEAB}$	14	A to B latch enable input (active LOW)
$\overline{OEBA}$	2	B to A output enable input (active LOW)
$\overline{OEAB}$	13	A to B output enable input (active LOW)
$\overline{EBA}$	23	B to A enable input (active LOW)
$\overline{EAB}$	11	A to B enable input (active LOW)
A[0:7]	3, 4, 5, 6, 7, 8, 9, 10	A data input or output
B[0:7]	22, 21, 20, 19, 18, 17, 16, 15	B data output or input
GND	12	ground (0 V)
V_{CC}	24	supply voltage

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6. Functional description

Table 3. Functional table[1]

Operating modes	Input				Output
	$\overline{OEAB}$, $\overline{OEBA}$	$\overline{EAB}$, $\overline{EBA}$	$\overline{LEAB}$, $\overline{LEBA}$	An, Bn	Bn, An
Disabled	H	X	X	X	Z
	X	H	X	X	Z
Disabled plus latch	L	↑	L	h	Z
	L	↑	L	l	Z
Latch plus display	L	L	↑	h	H
	L	L	↑	l	L
Transparent	L	L	L	H	H
	L	L	L	L	L
Hold (do nothing)	L	L	H	X	NC

[1] H = HIGH voltage level
L = LOW voltage level
h = a HIGH must be present one set-up time before the LOW to HIGH transition of $\overline{LEAB}$, $\overline{LEBA}$, $\overline{EAB}$ and $\overline{EBA}$
l = a LOW must be present one set-up time before the LOW to HIGH transition of $\overline{LEAB}$, $\overline{LEBA}$, $\overline{EAB}$ and $\overline{EBA}$
X = don't care
↑ = LOW to HIGH level transition
NC = no change
Z = high-impedance OFF-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		−50	-	mA
V_I	input voltage		[1]	−0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	output HIGH or LOW	[2]	−0.5	V_{CC} + 0.5	V
		output 3-state	[2]	−0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			−100	-	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to +125 °C	[3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO24 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For (T)SSOP24 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN24 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

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8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH or LOW	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	ambient temperature	in free air	−40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	0.65 × V_{CC}	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = −100 μA; V_{CC} = 1.65 V to 3.6 V	V_{CC} − 0.2	-	-	V_{CC} − 0.3	-	V
		I_O = −4 mA; V_{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I_O = −8 mA; V_{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I_O = −12 mA; V_{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I_O = −18 mA; V_{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I_O = −24 mA; V_{CC} = 3.0 V	2.2	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 μA; V_{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.8	V
I_I	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	±0.1	±5	-	±20	μA

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Table 6. Static characteristics *...continued*

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 3.6 V; V_O = 5.5 V or GND;	-	0.1	±10	-	±20	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	0.1	±10	-	±20	µA
I_{CC}	supply current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0 A	-	0.1	10	-	40	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC} - 0.6$ V; I_O = 0 A	-	5	500	-	5000	µA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}	-	4.0	-	-	-	pF
$C_{I/O}$	input/output capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 10.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	An to Bn; Bn to An; see Figure 6 [2]						
		V_{CC} = 1.2 V	-	15	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	1.7	7.1	16.3	1.7	18.9	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	3.8	8.4	1.5	9.7	ns
		V_{CC} = 2.7 V	1.5	3.7	8.0	1.5	10.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.2	7.0	1.0	9.0	ns
		$\overline{LEBA}$ to An; $\overline{LEAB}$ to Bn; see Figure 7 [2]						
		V_{CC} = 1.2 V	-	16	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	1.5	7.3	19.9	1.5	22.9	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	3.9	10.2	1.0	11.8	ns
		V_{CC} = 2.7 V	1.5	4.2	9.5	1.5	12.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	3.2	8.5	1.2	11.0	ns

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Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 10.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{en}	enable time	$\overline{OEBA}$ to An; $\overline{OEAB}$ to Bn; see Figure 8 [2]						
		V_{CC} = 1.2 V	-	17	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	1.7	7.4	17.6	1.7	20.3	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	4.2	9.7	1.5	11.2	ns
		V_{CC} = 2.7 V	1.5	4.3	9.2	1.5	11.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.3	3.4	7.7	1.3	10.0	ns
		$\overline{EBA}$ to An; $\overline{EAB}$ to Bn; see Figure 8 [2]						
		V_{CC} = 1.2 V	-	18	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	1.9	8.0	18.3	1.9	21.1	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	4.5	10.1	1.5	11.6	ns
		V_{CC} = 2.7 V	1.5	4.6	9.3	1.5	12.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.3	3.6	8.0	1.3	10.0	ns
t_{dis}	disable time	$\overline{OEBA}$ to An; $\overline{OEAB}$ to Bn; see Figure 8 [2]						
		V_{CC} = 1.2 V	-	8.0	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.7	4.8	12.0	2.7	13.9	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.7	6.8	1.0	7.9	ns
		V_{CC} = 2.7 V	1.5	3.5	7.5	1.5	9.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	3.3	7.0	1.5	9.0	ns
		$\overline{EBA}$ to An; $\overline{EAB}$ to Bn; see Figure 8 [2]						
		V_{CC} = 1.2 V	-	8.5	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	3.1	5.0	12.1	3.1	14.0	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.8	6.9	1.0	8.0	ns
		V_{CC} = 2.7 V	1.5	3.6	7.5	1.5	11.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	3.4	7.0	1.5	9.0	ns
t_W	pulse width	$\overline{LEAB}$, $\overline{LEBA}$ LOW; see Figure 7						
		V_{CC} = 1.65 V to 1.95 V	5.0	-	-	5.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	4.0	-	-	4.0	-	ns
		V_{CC} = 2.7 V	3.0	-	-	3.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	3.0	0.9	-	3.0	-	ns
t_{su}	set-up time	An, Bn to $\overline{LEAB}$, $\overline{LEBA}$, $\overline{EAB}$, $\overline{EBA}$; see Figure 9						
		V_{CC} = 1.65 V to 1.95 V	3.0	-	-	3.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	2.0	-	-	2.0	-	ns
		V_{CC} = 2.7 V	1.5	-	-	1.5	-	ns
		V_{CC} = 3.0 V to 3.6 V	+1.5	-0.5	-	1.5	-	ns

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Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 10.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_h	hold time	An, Bn to $\overline{LEAB}$, $\overline{LEBA}$, $\overline{EAB}$, $\overline{EBA}$; see Figure 9							
		V_{CC} = 1.65 V to 1.95 V		4.0	-	-	4.0	-	ns
		V_{CC} = 2.3 V to 2.7 V		2.5	-	-	2.5	-	ns
		V_{CC} = 2.7 V		1.5	-	-	1.5	-	ns
		V_{CC} = 3.0 V to 3.6 V		1.5	0.6	-	1.5	-	ns
$t_{sk(o)}$	output skew time	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}	[4]						
		V_{CC} = 1.65 V to 1.95 V		-	8.3	-			pF
		V_{CC} = 2.3 V to 2.7 V		-	11.9	-			pF
		V_{CC} = 3.0 V to 3.6 V		-	15.2	-			pF

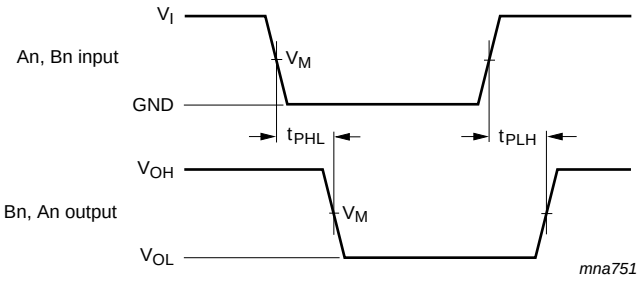
[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

11. AC waveforms



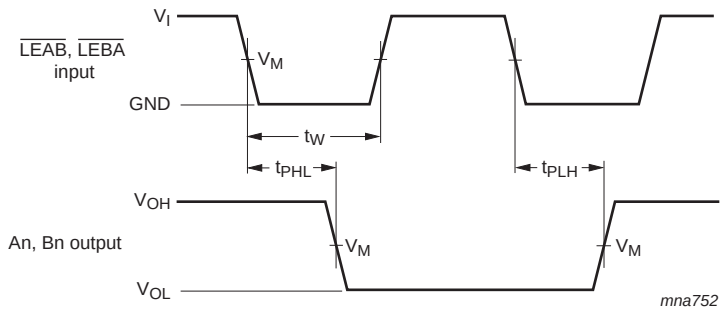
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. Input (An and Bn) to output (Bn and An) propagation delays

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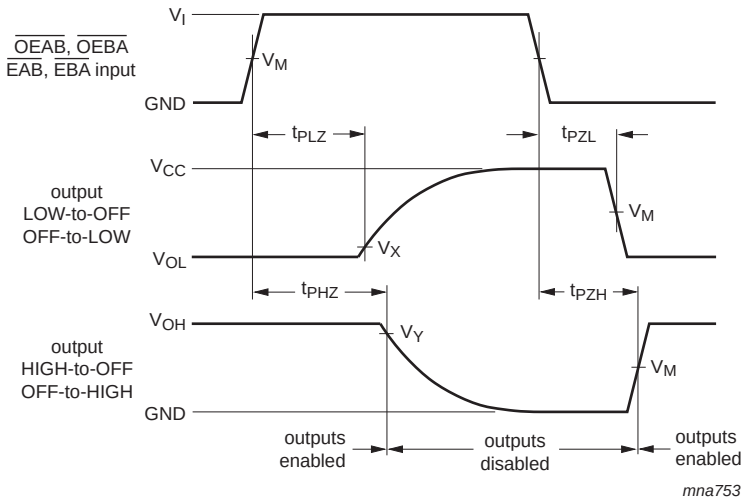
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Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. Latch enable input ($\overline{LEAB}$, $\overline{LEBA}$) pulse width and latch enable input to output An and Bn propagation delays



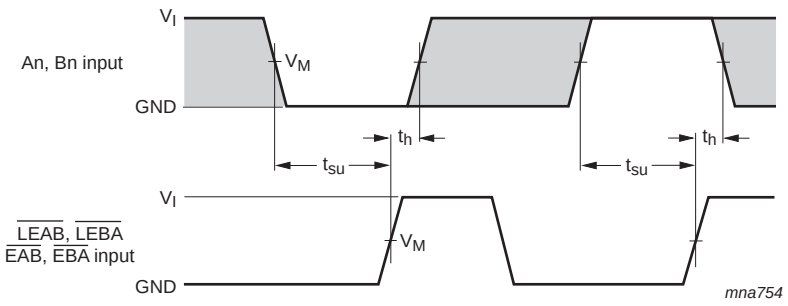
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. 3-state enable and disable times

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Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

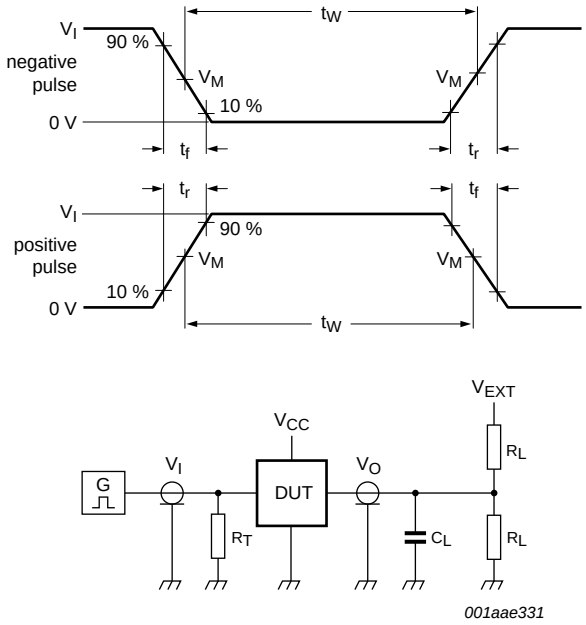
Fig 9. Data set-up and hold times for the inputs An and Bn to $\overline{LEAB}$, $\overline{LEBA}$ and $\overline{EAB}$, $\overline{EBA}$ inputs

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
1.2 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
1.65 V to 1.95 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V

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Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 10. Test circuit for measuring switching times

Table 9. Test data

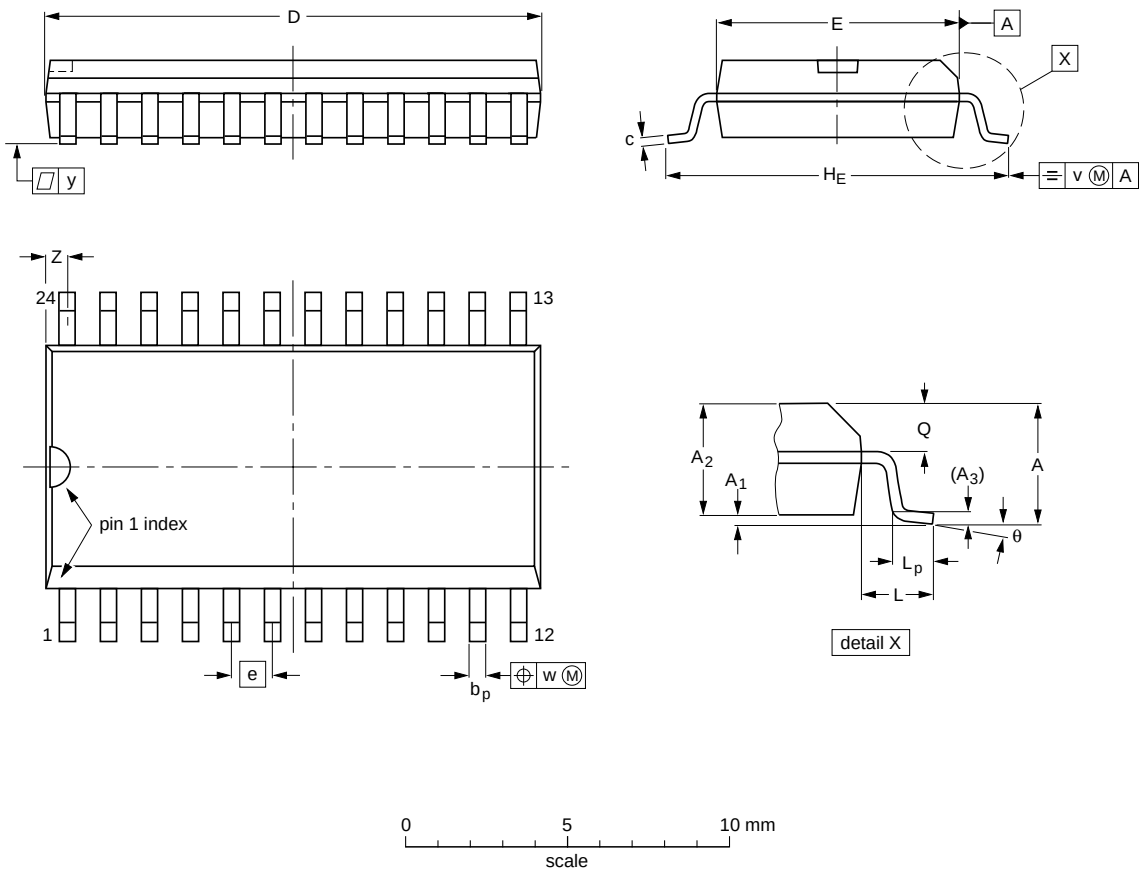
Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

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12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

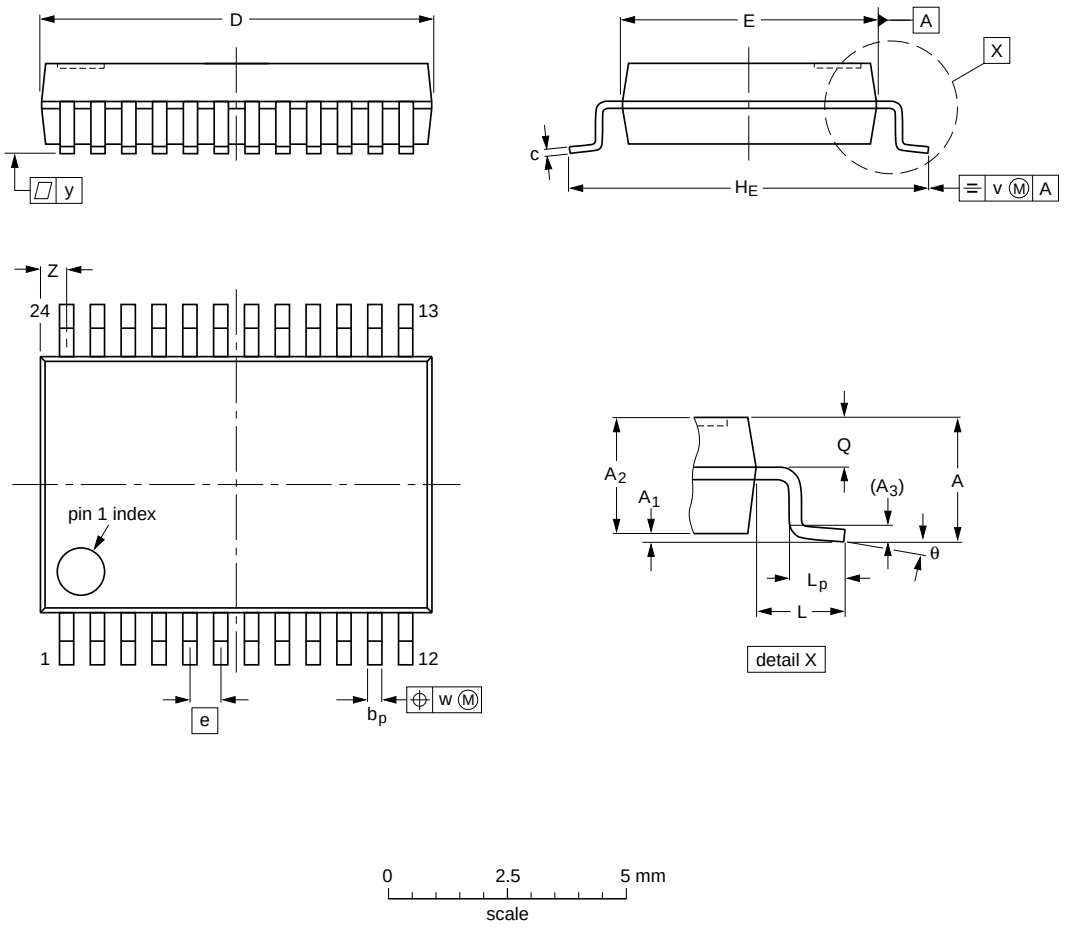
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT137-1 (SO24)

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SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

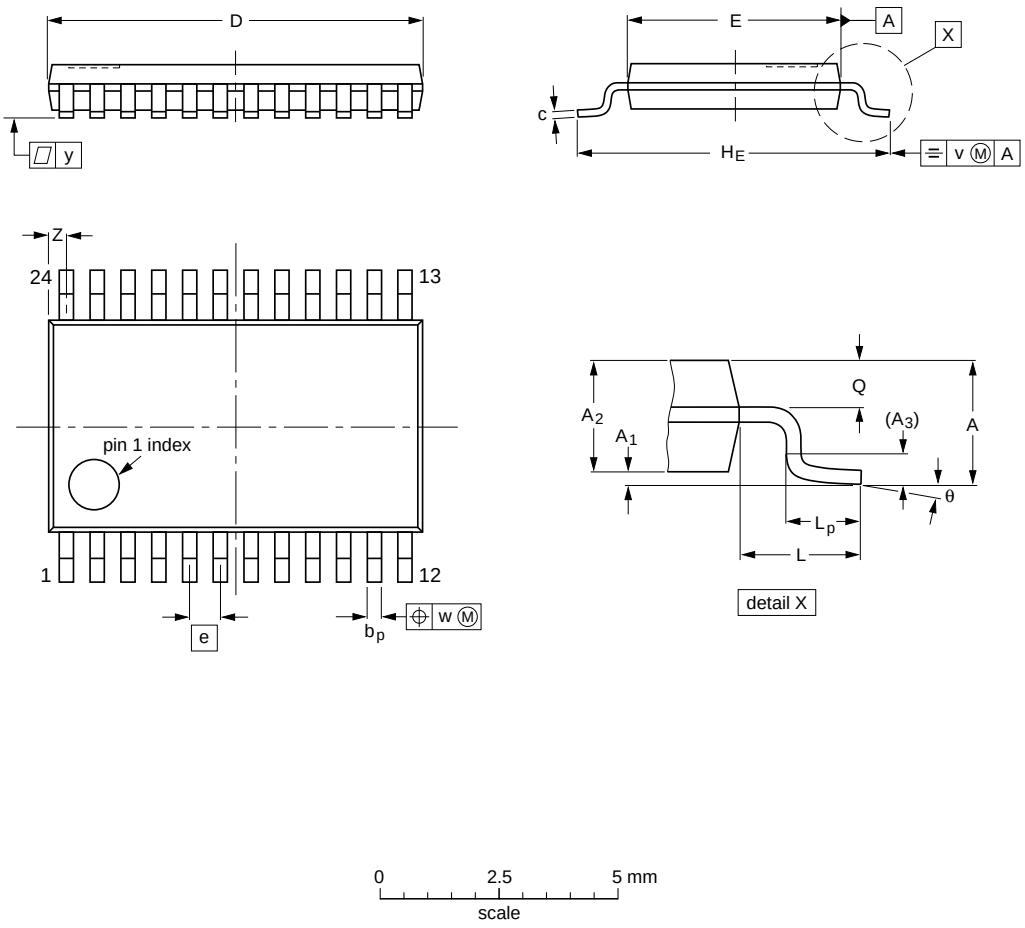
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT340-1 (SSOP24)

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TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

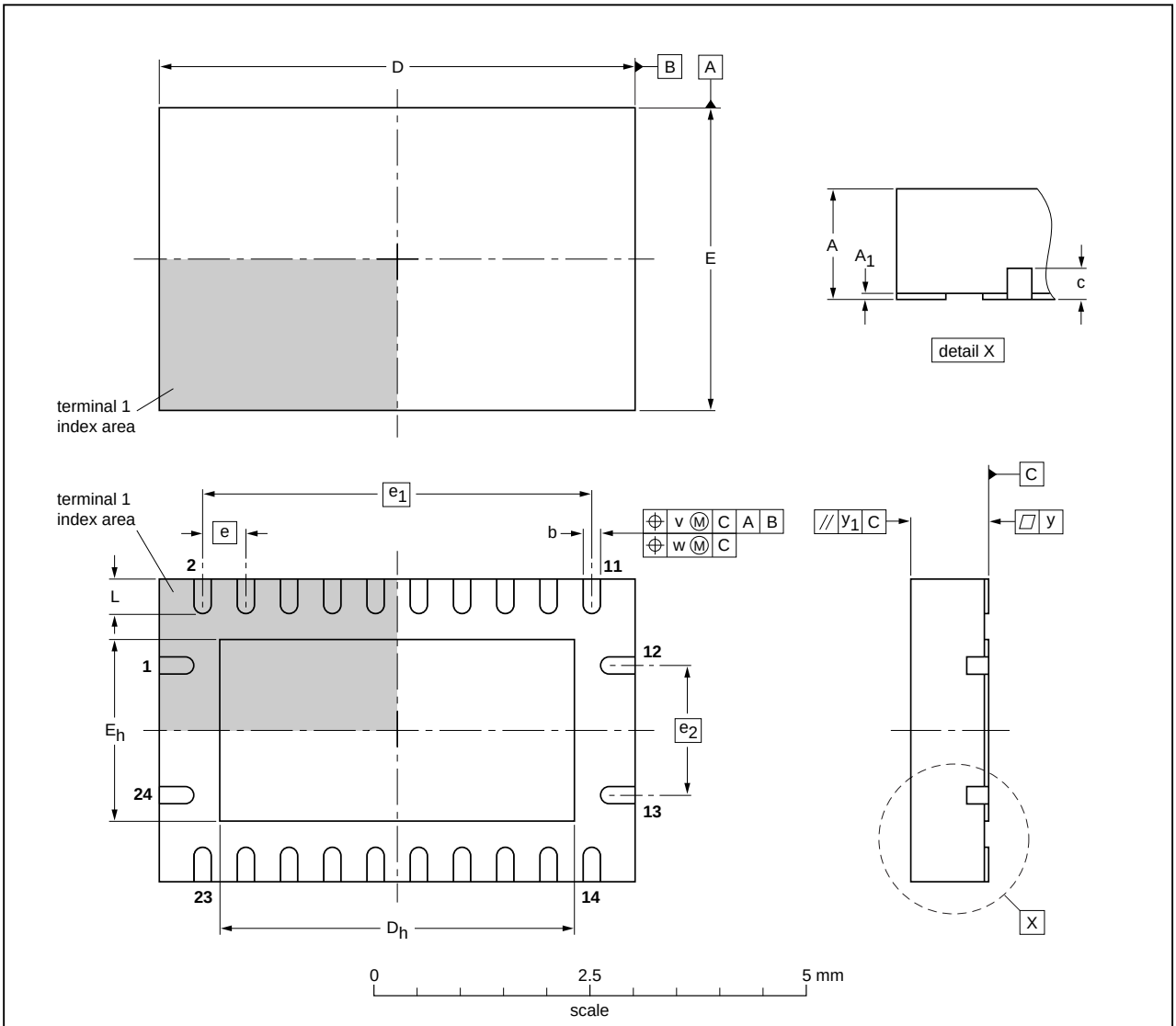
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT355-1 (TSSOP24)

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DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm **SOT815-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.6 5.4	4.25 3.95	3.6 3.4	2.25 1.95	0.5	4.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT815-1	- - -	- - -	- - -			03-04-29

Fig 14. Package outline SOT815-1 (DHVQFN24)

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC543A v.8	20121218	Product data sheet	-	74LVC543A v.7
Modifications:	• Changed interlacing into interfacing (errata) in features list.			
74LVC543A v.7	20121129	Product data sheet	-	74LVC543A v.6
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 4, Table 5, Table 6, Table 7, Table 8 and Table 9: values added for lower voltage ranges.			
74LVC543A v.6	20040407	Product specification	-	74LVC543A v.5
74LVC543A v.5	20040205	Product specification	-	74LVC543A v.4
74LVC543A v.4	20030516	Product specification	-	74LVC543A v.3
74LVC543A v.3	20000621	Product specification	-	74LVC543A v.2
74LVC543A v.2	19980731	Product specification	-	74LVC543A v.1
74LVC543A v.1	19970630	Product specification	-	-

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