Discription

The HPJGBLC05C-AU protects sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD) and other voltage induced transient events. Excellent clamping capability, low leakage, low capacitance, and fast response time provide best in class protection on designs that are exposed to ESD.

It gives designer the flexibility to protect one bi-directional line in applications where arrays are not practical.



SOD-323

Features

- ★ Small Body Outline Dimensions
- ★ Low Body Height
- ★ Peak Power up to 30 Watts @ 8 x 20 _s Pulse
- ★ Low Leakage current
- ★ Response Time is Typically < 1 ns
- ★ IEC61000−4−2 Level 4 ESD Protection
- ★ IEC61000−4−4 Level 4 EFT Protection



Circuit Diagram

Orderingin formation

Product ID	Pack	Qty(PCS)
HPJGBLC05C-AU	SOD-323	3000

Absolute Ratings(Tamb = 25°C)

Symbol	Parameter	Value	Units
P_{PP}	Peak Pulse Power (t_p = 8/20 μ s)	30	W
T_L	Maximum lead temperature for soldering during 10s	260	°C
T_{stg}	Storage Temperature Range	-55 to +155	°C
T_{op}	Operating Temperature Range	-40 to +125	°C
T_j	Maximum junction temperature	150	°C
	IEC61000-4-2 (ESD) air discharge contact discharge	±10 ±15	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Rating are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR-5 = 1.0*0.75*0.62 in.

Electrical Characteristics Ratings at 25°C ambient temperature unless otherwise specified.VF = 0.9V at IF = 10mA

V_{RWM} (V)	I_R(uA) @ V_{RWM}	V_{BR} (V)@ I_T (Note 1)	I_T	V_C (V) @ I_{PP}=1 A*	V_C (V) @ Max I_{PP}*	I_{PP} (A)*	P_{PK} (W)*	C (pF)
Max	Max	Min	mA	Typ	Max	Max	Max	Max
5	1.0	5.4	1	9.5	12.9	2	30	2.5

*Surge current waveform per Figure 1.

1. V_{BR} is measured with a pluse test current I_T at an ambient temperature of 25℃.

Typical Characteristics

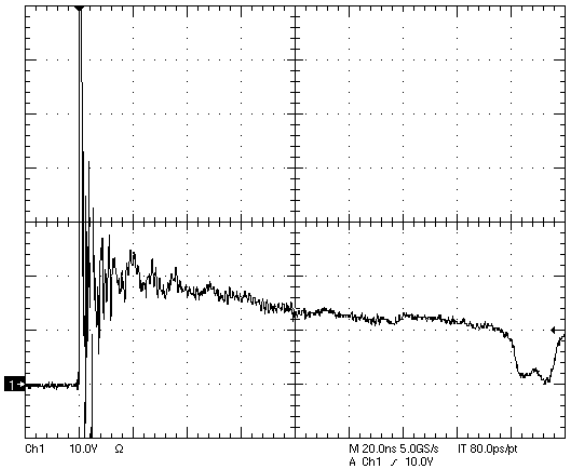


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

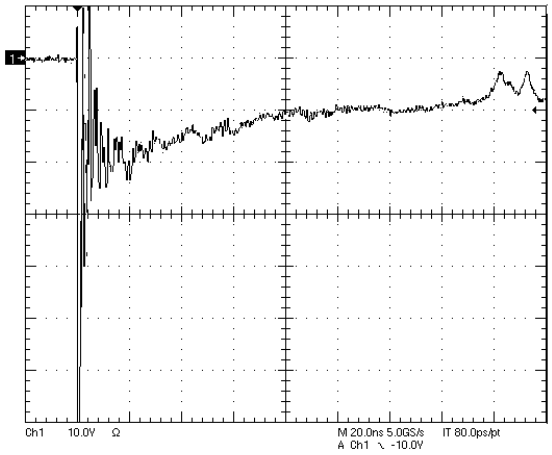


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

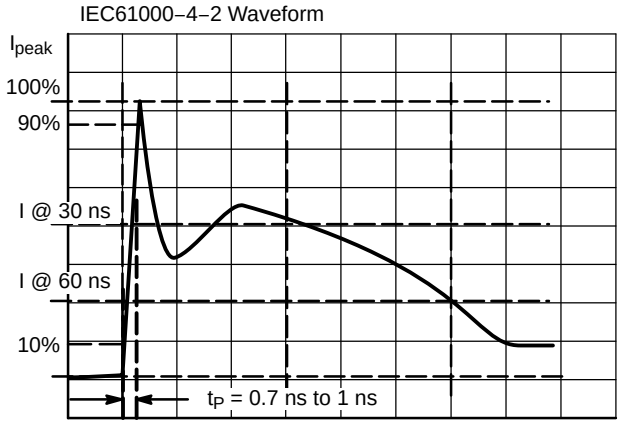
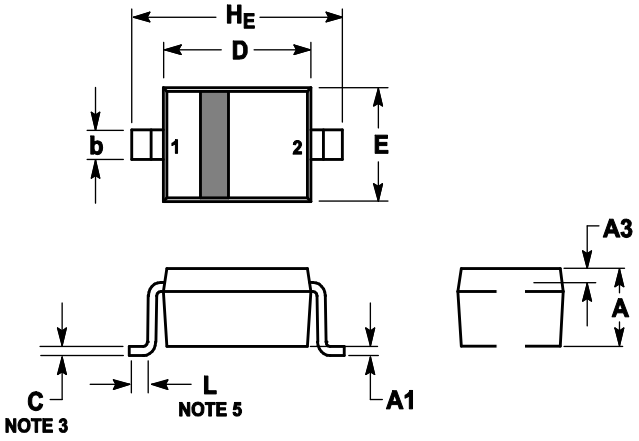


Figure 3. IEC61000−4−2 Spec

OUTLINE AND DIMENSIONS

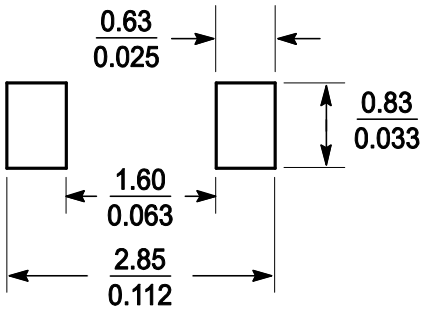


Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.8	0.9	1	0.031	0.035	0.04
A1	0	0.05	0.1	0	0.002	0.004
A3	0.15REF			0.006REF		
b	0.25	0.32	0.4	0.01	0.012	0.016
C	0.089	0.12	0.177	0.003	0.005	0.007
D	1.6	1.7	1.8	0.062	0.066	0.07
E	1.15	1.25	1.35	0.045	0.049	0.053
L	0.08			0.003		
H_E	2.3	2.5	2.7	0.09	0.098	0.105

SOLDERING FOOTPRINT



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