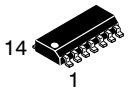
8-Bit Serial-in/Parallel-out Shift Register

MM74HCT164



SOIC−14
CASE 751EF

Description

The MM74HCT164 utilizes advanced silicon−gate CMOS technology. It has the high noise immunity and low consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices. This 8−bit shift register has gated serial inputs and CLEAR. Each register bit is a D−type master/slave flip−flop. Inputs A & B permit complete control over the incoming data. A LOW at either or both inputs inhibits entry of new data and resets the first flip−flop to the low level at the next clock pulse. A high level on one input enables the other input which will then determine the state of the first flip−flop. Data at the serial inputs may be changed while the clock is HIGH or LOW, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8−bit register during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the CLEAR input.

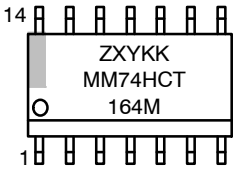
The 74HCT logic family is functionally as well as pin−out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug−in replacements for LS−TTL devices and can be used to reduce power consumption in existing designs.

Features

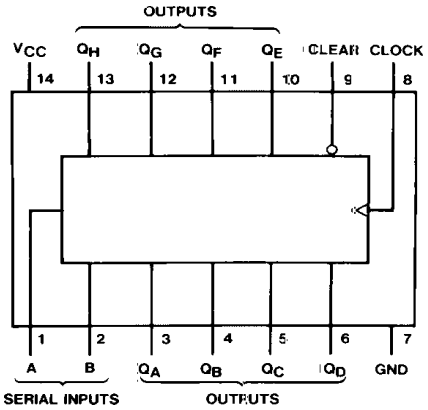
- Typical Propagation Delay: 20 ns
- Low Quiescent Current: 160 μA Maximum (74HCT Series)
- Low Input Current: 1 μA Maximum
- Fanout of 10 LS−TTL Loads
- TTL Input Compatible
- These are Pb−Free Devices

MARKING DIAGRAM



MM74HCT164M = Specific Device Code
Z = Assembly Plant Code
XY = Data Code (Year & Week)
KK = Lot Traceability Code

CONNECTION DIAGRAM



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
MM74HCT164MX	SOIC−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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TRUTH TABLE

Inputs				Outputs			
Clear	**Clock**	**A**	**B**	**Q_A**	**Q_B**	**…**	**Q_H**
L	X	X	X	L	L		L
H	L	X	X	Q_{AO}	Q_{BO}		Q_{HO}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

H = HIGH Level (steady state)
L = LOW Level (steady state)
X = Irrelevant (any input, including transitions)
↑ = Transition from LOW−to−HIGH level
Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicated a one−bit shift.

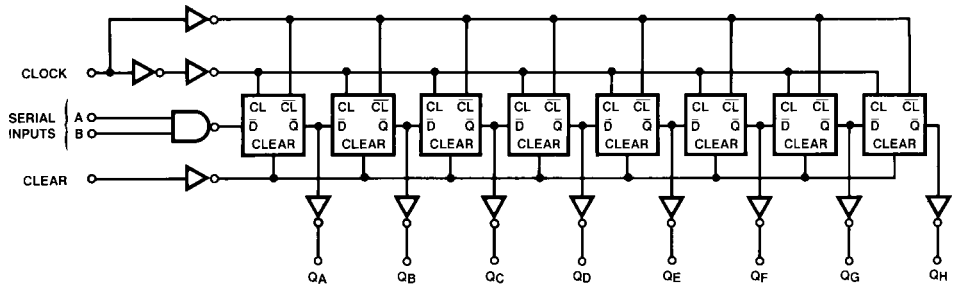


Figure 1. Logic Diagram

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to +6.5	V
V_{IN}	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_{OUT}	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}, I_{OK}	Clamp Diode Current	±20	mA
I_{OUT}	DC Output Current, per Pin	±25	mA
I_{CC}	DC V_{CC} or GND Current, per Pin	±50	mA
T_{STG}	Storage Temperature Range	−65 to +150	°C
P_D	Power Dissipation SOIC−14 TSSOP−14	1077 833	mW
T_L	Lead Temperature (Soldering 10 seconds)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Unless otherwise specified all voltages are referenced to ground.

RECOMMENDED OPERATIONG CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	−55	+125	°C
t_r, t_f	Input Rise or Fall Times	–	500	ns

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ±10% unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	T_A = −40°C to 85°C	T_A = −55°C to 125°C	Unit
			Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage		–	2.0	2.0	2.0	V
V_{IL}	Maximum LOW Level Input Voltage		–	0.8	0.8	0.8	V
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}					V
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} −0.1	V_{CC} −0.1	V_{CC} −0.1	
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5 V	4.2	3.98	3.84	3.7	
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5 V	5.2	4.98	4.84	4.7	
V_{OL}	Maximum LOW Level Voltage	$V_{IN} = V_{IH}$ or V_{IL}					V
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5 V	0.2	0.26	0.33	0.4	
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5 V	0.2	0.26	0.33	0.4	
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	–	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, I_{OUT} = 0 μA	–	8.0	80	160	μA
		V_{IN} = 2.4 V or 0.4 V (Note 2)	–	1.0	1.3	1.5	mA

2. This is measured per input pin. All other inputs are held at V_{CC} or ground.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
f_{MAX}	Maximum Operating Frequency from Clock to Q	50% Duty Cycle Clock	55	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		17	27	ns
t_{PHL}	Maximum Propagation Delay, from Clear to Q		23	38	ns
t_{REM}	Minimum Removal Time, Clear to Clock		3	6	ns
t_S	Minimum Setup Time, Data to Clock	$t_H \geq$ 20 ns	6	13	ns
t_H	Minimum Hold Time, Clock to Data	$t_S \geq$ 20 ns	1.5	5	ns
t_W	Minimum Pulse Width, Preset or Clear		9	16	ns

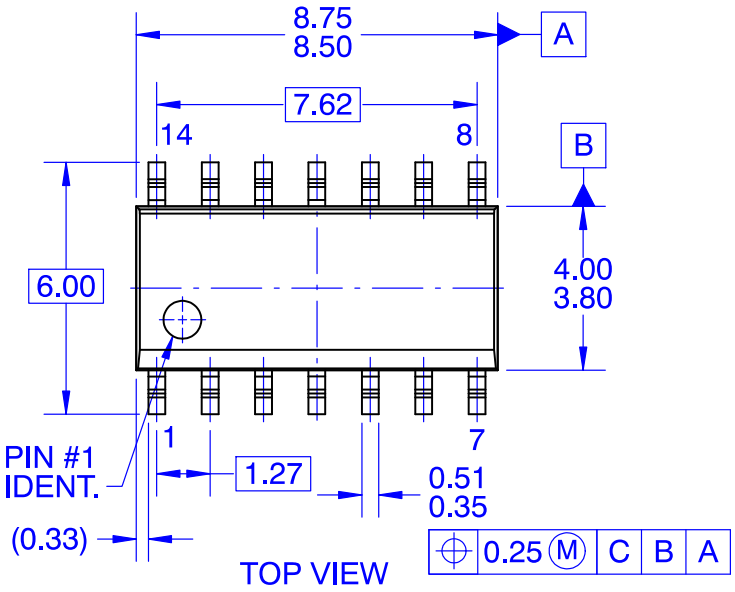
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, ±10%, C_L = 50 pF, $t_r = t_f$ = 6 ns unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C		T_A −40°C to 85°C		T_A = −55°C to 125°C		Unit
			Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Operating Frequency	50% Duty Cycle Clock	45	30	–	25	–	22	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, from Clock to Q		20	30	–	38	–	45	ns
t_{PHL}	Maximum Propagation Delay, from Clear to Q		26	41	–	51	–	61	ns
t_{REM}	Minimum Removal Time, Clear to Clock		4	8	–	10	–	14	ns
t_S	Minimum Setup Time, Data to Clock	$t_H \geq 20$ ns	7	15	–	19	–	23	ns
t_H	Minimum Hold Time, Clock to Data	$t_S \geq 20$ ns	1.5	5	–	5	–	5	ns
t_W	Minimum Pulse Width, Clock or Clear		10	18	–	22	–	27	ns
t_r, t_f	Maximum Input Rise and Fall Time		–	500	–	500	–	500	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		–	15	–	19	–	22	ns
C_{PD}	Power Dissipation Capacitance (Note 3)		160	–	–	–	–	–	pF
C_{IN}	Maximum Input Capacitance		5	10	–	10	–	10	pF

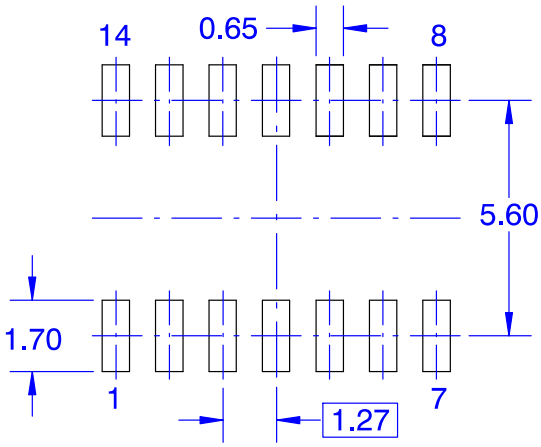
3. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

SOIC14
CASE 751EF
ISSUE O

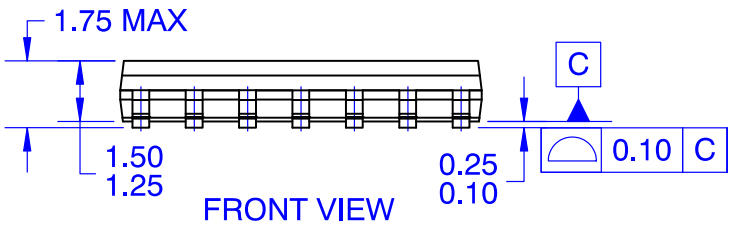
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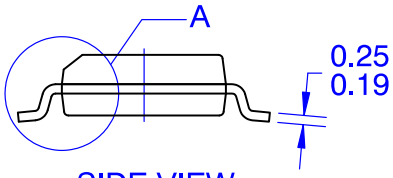
TOP VIEW



LAND PATTERN RECOMMENDATION

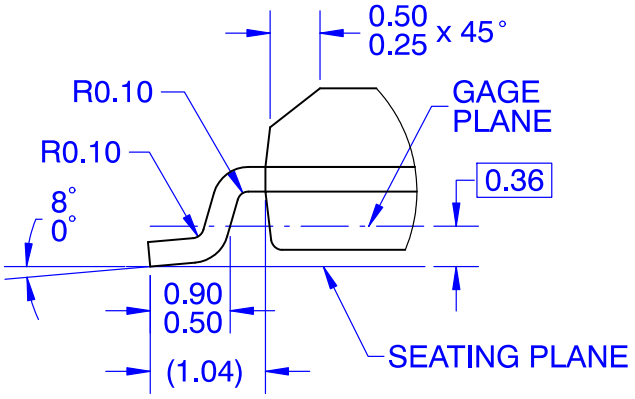


FRONT VIEW



SIDE VIEW

NOTES:
A. CONFORMS TO JEDEC MS−012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145−14M
E. CONFORMS TO ASME Y14.5M, 2009



DETAIL A
SCALE 16 : 1

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