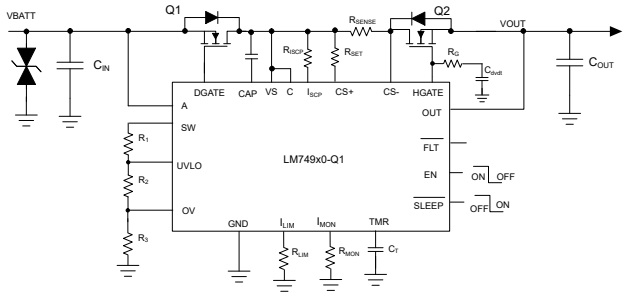
LM749x0-Q1 Automotive Ideal Diode With Circuit Breaker, Undervoltage, and Overvoltage Protection With Fault Output

1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- 3-V to 65-V input range
- Reverse input protection down to –65 V
- Drives external back-to-back N-Channel MOSFETs in common drain configuration
- Ideal diode operation with 10.5-mV A to C forward voltage drop regulation
- Low reverse detection threshold (–10.5 mV) with fast turn off response (0.5 µs)
- 20-mA peak gate (DGATE) turn on current
- 2.6-A peak DGATE turnoff current
- Adjustable overcurrent and short circuit protection
- Analog current monitor output with 10% accuracy (IMON)
- Adjustable overvoltage and undervoltage protection
- Low 2.5-µA shutdown current (EN=Low)
- SLEEP mode with 6-µA current (EN=High, $\overline{\text{SLEEP}}$=Low)
- Meets automotive ISO7637 transient requirements with a suitable TVS diode
- Available in space saving 24-Pin VQFN package

2 Applications

- Automotive battery protection
  - ADAS domain controller
  - Infotainment and cluster
  - Automotive audio: external amplifier
- Active ORing for redundant power



Typical Application Diagram

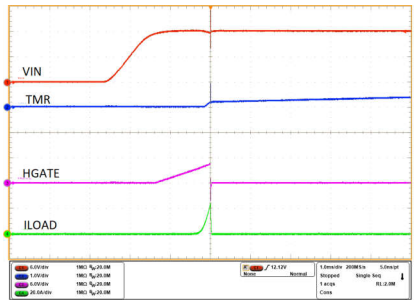
3 Description

The LM749x0-Q1 ideal diode controller drives and controls external back to back N-Channel MOSFETs to emulate an ideal diode rectifier with power path ON/OFF control with overcurrent and overvoltage protection. The wide input supply of 3 V to 65 V allows protection and control of 12-V and 24-V automotive battery powered ECUs. The device can withstand and protect the loads from negative supply voltages down to –65 V. An integrated ideal diode controller (DGATE) drives the first MOSFET to replace a Schottky diode for reverse input protection and output voltage holdup. With a second MOSFET in the power path the device allows load disconnect (ON/OFF control) in case of overcurrent and overvoltage events using HGATE control. The device has integrated current sense amplifier which provides accurate current monitoring with adjustable overcurrent and short circuit thresholds. The device features an adjustable overvoltage cut-off protection feature. The device features a SLEEP mode which enables ultra-low quiescent current consumption (6 µA) and at the same time providing refresh current to the always ON loads when vehicle is in the parking state. The LM749x0-Q1 has a maximum voltage rating of 65 V.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
LM74900-Q1	VQFN (24)	4.00 mm × 4.00 mm
LM74910-Q1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Device Start-Up With Overcurrent Protection

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2023) to Revision B (July 2023)	Page
• Removed preview notes for LM74900-Q1 in the Package Information table	1
• Added minor editorial changes throughout the document	1

Changes from Revision * (December 2022) to Revision A (June 2023)	Page
• Changed status from *Advance Information* to *Production Data*	1

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5 Device Comparison Table

Parameter	LM74900-Q1	LM74910-Q1
Charge pump strength	2.7 mA	4.2 mA

6 Pin Configuration and Functions

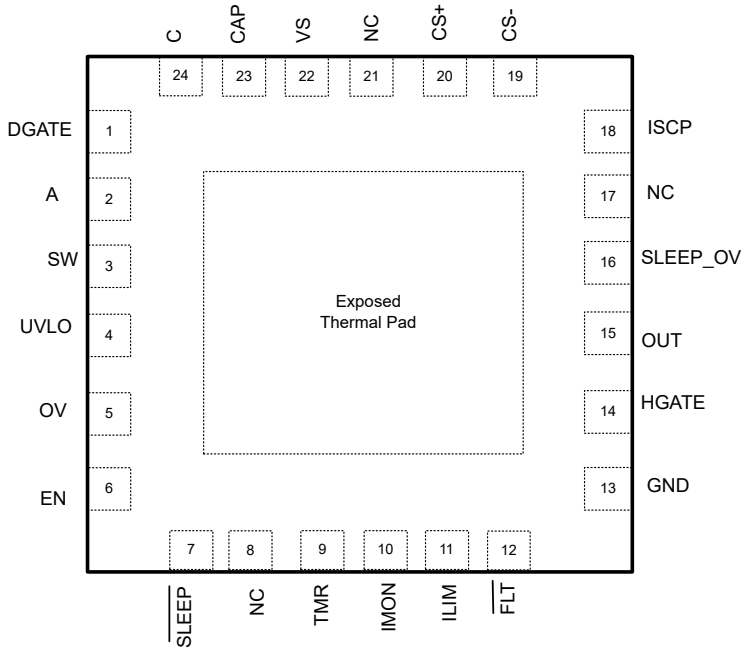


Figure 6-1. RGE Package, 24-Pin VQFN (Transparent Top View)

Table 6-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
DGATE	1	O	Diode controller gate drive output. Connect to the GATE of the external MOSFET.
A	2	I	Anode of the ideal diode. Connect to the source of the external MOSFET.
SW	3	I	Voltage sensing disconnect switch terminal. VSNS and SW are internally connected through a switch. Use SW as the top connection of the battery sensing or OV resistor ladder network. When EN is pulled low, the switch is OFF disconnecting the resistor ladder from the battery line thereby cutting off the leakage current. If the internal disconnect switch between VSNS and SW is not used then short them together and connect to VS pin.
UVLO	4	I	Adjustable undervoltage threshold input. Connect a resistor ladder across SW to UVLO terminal to GND. When the voltage at UVLO goes below the undervoltage cut-off threshold then the HGATE is pulled low turning OFF the HSFET. HGATE turns ON when the sense voltage goes above the UVLO falling threshold.
OV	5	I	Adjustable overvoltage threshold input. Connect a resistor ladder across SW to OV terminal. When the voltage at OVP exceeds the overvoltage cut-off threshold then the HGATE is pulled low turning OFF the HSFET. HGATE turns ON when the sense voltage goes below the OVP falling threshold.
EN	6	I	EN input. Connect to VS pin for always ON operation. Can be driven externally from a microcontroller I/O. Pulling it low below $V_{(ENF)}$ makes the device enter into low Iq shutdown mode.
$\overline{\text{SLEEP}}$	7	I	Active low SLEEP mode input. Can be driven from the microcontroller. When pulled low device enters into low power state with charge pump and gate drive turned off. Internal bypass switch provides output voltage with limited current capacity.
NC	8	—	No connect.

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Table 6-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
TMR	9	I	Fault timer input. A capacitor across TMR pin to GND sets the times for fault warning, fault turn off ($\overline{FLT}$), and retry periods. Leave it open for fastest setting. Connect TMR to GND to disable overcurrent protection.
IMON	10	O	Analog current monitor output. This pin sources a scaled down ratio of current through the external current sense resistor R_{SNS}. A resistor from this pin to GND converts current to proportional voltage. If unused, leave it floating.
ILIM	11	I	Overcurrent detection setting. A resistor across ILIM to GND sets the overcurrent comparator threshold. Connect ILIM to GND if overcurrent protection feature is not desired.
$\overline{FLT}$	12	O	Open drain fault output. FLT pin is pulled low in case of UVLO, OV, OCP, or SCP event.
GND	13	G	Connect to the system ground plane.
HGATE	14	O	GATE driver output for the HSFET. Connect to the GATE of the external FET.
OUT	15	I	Connect to the output rail (external MOSFET source).
SLEEP_OV	16	I	SLEEP mode overvoltage protection pin. Connect this pin to VS for overvoltage cut-off functionality. Connect to OUT for overvoltage clamp functionality.
NC	17	—	No connect.
ISCP	18	I	Short circuit detection threshold setting. Leave ISCP floating if short circuit protection is not desired. When ISCP is connected to CS+, device sets an internal fix threshold of 20 mV.
CS–	19	I	Current sense negative input.
CS+	20	I	Current sense positive input. Connect a TBD resistor across CS+ to the external current sense resistor.
NC	21	—	No connect.
VS	22	P	Input power supply to the IC. Connect VS to middle point of the common drain back to back MOSFET configuration. Connect a 100-nF capacitor across VS and GND pins.
CAP	23	O	Charge pump output. Connect a 100-nF capacitor across CAP and VS pins.
C	24	I	Cathode of the ideal diode. Connect to the drain of the external MOSFET.
RTN	Thermal Pad	—	Leave exposed pad floating. Do not connect to GND plane.

(1) I = input, O = output, I/O = input and output, P = power, G = ground

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Pins	A to GND	–65	70	V
	VS, CS+, CS-, ISCP, OUT, SLEEP_OV to GND	–1	70	
	SW, C, EN, $\overline{SLEEP}$, FLT, UVLO, OV to GND, $V_{(A)}$ > 0 V	–0.3	70	
	SW, C, EN, $\overline{SLEEP}$, FLT, UVLO, OV to GND, $V_{(A)}$ ≤ 0 V	$V_{(A)}$	(70 + $V_{(A)}$)	
	RTN to GND	–65	0.3	
	I_{SW} ,I_{FLT}	–1	10	mA
	TMR, ILIM	–0.3	5.5	V
	I_{EN}, I_{UVLO},I_{OV} $V_{(A)}$ > 0 V	–1		mA
	I_{EN}, I_{UVLO},I_{OV} $V_{(A)}$ ≤ 0 V	Internally limited		
Input Pins	ISCP, CS+ to CS-	–0.3	0.3	V
Output Pins	OUT to VS	–65	5	V
	CAP to VS	–0.3	15	V
	CAP to A	–0.3	85	
	DGATE to A	–0.3	15	
	FLT to GND	-0.3	70	
	IMON	-1	5.5	
	HGATE to OUT	–0.3	15	
Output to Input Pins	C to A	–5	85	
Operating junction temperature, T_j (2)		–40	150	°C
Storage temperature, T_{stg}		–40	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input Pins	A to GND	–60		65	V
	VS, SW, CS+, CS–, ISCP to GND	0		65	V
	EN,UVLO, OV, $\overline{SLEEP}$ to GND	0		65	V
Output pins	FLT to GND	0		65	V
Output pins	IMON to GND	0		5	V

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7.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
External Capacitance	CAP to A, VS to GND, A to GND	0.1			µF
External MOSFET max VGS rating	DGATE to A and HGATE to OUT	15			V
Tj	Operating Junction temperature(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.4 Thermal Information

THERMAL METRIC(1)		LM749x0-Q1 RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	21.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(OUT)}$ = $V_{(VS)}$ = 12 V, $C_{(CAP)}$ = 0.1 µF, $V_{(EN)}$, $V_{(SLEEP)}$= 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{(VS)}$	Operating input voltage		3		65	V
$V_{(VS_PORR)}$	VS POR threshold, rising		2.4	2.6	2.9	V
$V_{(VS_PORF)}$	VS POR threshold, falling		2.2	2.4	2.7	V
$I_{(SHDN)}$	SHDN current, $I_{(GND)}$	$V_{(EN)}$ = 0 V		2.5	5	µA
$I_{(SLEEP)}$	SLEEP mode current, $I_{(GND)}$	$V_{(EN)}$ = 2 V, $V_{(SLEEP)}$ = 0 V		5.5	10	µA
$I_{(Q)}$	Total System Quiescent current, $I_{(GND)}$	$V_{(EN)}$ = 2 V		630	750	µA
		$V_{(A)}$ = $V_{(VS)}$ = 24 V, $V_{(EN)}$ = 2 V		635	750	µA
$I_{(REV)}$	$I_{(A)}$ leakage current during Reverse Polarity,	0 V ≤ $V_{(A)}$ ≤ – 65 V	–100	–35		µA
	$I_{(OUT)}$ leakage current during Reverse Polarity		–1	–0.3		µA
ENABLE						
$V_{(ENF)}$	Enable rising threshold voltage		0.6	0.8	1.05	V
$V_{(ENF)}$	Enable threshold voltage for low Iq shutdown, falling		0.41	0.7	0.98	V
$I_{(EN)}$		0 V ≤ $V_{(EN)}$ ≤ 65 V		55	200	nA
UNDER VOLTAGE LOCKOUT COMPARATOR (SW, UVLO)						

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7.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(OUT)}$ = $V_{(VS)}$ = 12 V, $C_{(CAP)}$ = 0.1 µF, $V_{(EN)}$, $V_{(SLEEP)}$= 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(UVLOR)}$	UVLO threshold voltage, rising		0.585	0.6	0.63	V
$V_{(UVLOF)}$	UVLO threshold voltage, falling		0.533	0.55	0.573	V
$I_{(UVLO)}$		0 V ≤ $V_{(UVLO)}$ ≤ 5 V		50	200	nA
OVER VOLTAGE PROTECTION AND BATTERY SENSING (SW, OV) INPUT						
$R_{(SW)}$	Battery sensing disconnect switch resistance	3 V ≤ $V_{(A)}$ ≤ 65 V	10	22.5	46	Ω
$V_{(OVR)}$	Overvoltage threshold input, rising		0.585	0.6	0.63	V
$V_{(OVF)}$	Overvoltage threshold input, falling		0.533	0.55	0.573	V
$I_{(OV)}$	OV Input leakage current	0 V ≤ $V_{(OV)}$ ≤ 5 V		50	200	nA
CURRENT SENSE AMPLIFIER						
$V_{(OFFSET)}$	Input referred offset (V_{SNS} to V_{IMON} scaling)	R_{SET} = 50Ω, R_{IMON} = 5kΩ, 10kΩ (corresponds to V_{SNS} = 6mV to 30mV) Gain of 45 and 90 respectively.	-2.1		2.1	mV
$V_{(GE_SET)}$	V_{SNS} to V_{IMON} scaling	R_{SET} = 50Ω, R_{IMON} = 5kΩ, (corresponds to V_{SNS} = 6mV to 30mV)	82	90	97	
$V_{(SNS_TH)}$	OCP comparator threshold, rising (ILIM)		1.08	1.22	1.32	
$V_{(SNS_TH)}$	OCP comparator threshold, falling (ILIM)		1.02	1.15	1.25	V
I_{SCP}	SCP Input Bias current	V_{ISCP} = 12V	9.5	10.5	12	µA
$V_{(SNS_SCP)}$	SCP threshold	$R_{(ISCP)}$ = 0Ω (I_{SCP} connected to VS)	17.86	20	22.77	mV
$V_{(SNS_SCP)}$	SCP threshold	$R_{(ISCP)}$ = 1kΩ (external)		31		mV
I_{MON_ACC}	Current monitor output accuracy	V_{SENSE} = 20mV	-12.5		12.5	%
FAULT						
R($\overline{FLT}$)	$\overline{FLT}$_I Pull-down resistance		11	25	60	Ω
I_$\overline{FLT}$	$\overline{FLT}$ Input leakage current	0 V ≤ $V_{(\overline{FLT})}$ ≤ 20 V	–100		400	nA
DELAY TIMER (TMR)						
$I_{(TMR_SRC_CB)}$	TMR source current		65	85	97	µA
$I_{(TMR_SRC_FLT)}$	TMR source current		1.94	2.7	3.4	µA
$I_{(TMR_SNK)}$	TMR sink current		2	2.7	3.15	µA
$V_{(TMR_OC)}$	Voltage at TMR pin for IWRN shut off		1.1	1.2	1.4	V
$V_{(TMR_FLT)}$	Voltage at TMR pin for IFLT triggerring		1.04	1.1	1.2	V
$V_{(TMR_LOW)}$	Voltage at TMR pin for AR counter falling threshold		0.1	0.2	0.3	V
$N_{(A_R_Count)}$	Number of autoretry cycles			32		
CHARGE PUMP (CAP)						
$I_{(CAP)}$	Charge Pump source current (Charge pump on)	$V_{(CAP)}$ – $V_{(A)}$ = 7 V, 6 V ≤ $V_{(S)}$ ≤ 65 V	1.3	2.7		mA
		V(CAP) – V(A) = 7 V, VS= 65 V, LM74910-Q1 Only	2.5	4.2		mA
VCAP – VS	Charge Pump Turn ON voltage		11	12.2	13.2	V
	Charge Pump Turnoff voltage		11.9	13.2	14.1	V
$V_{(CAP\ UVLO)}$	Charge Pump UVLO voltage threshold, rising		5.4	6.6	7.9	V
	Charge Pump UVLO voltage threshold, falling		4.4	5.5	6.6	V
IDEAL DIODE (A, C, DGATE)						

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7.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(OUT)}$ = $V_{(VS)}$ = 12 V, $C_{(CAP)}$ = 0.1 µF, $V_{(EN)}$, $V_{(SLEEP)}$= 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(A_PORR)}$	$V_{(A)}$ POR threshold, rising		2.2	2.45	2.7	V
$V_{(A_PORF)}$	$V_{(A)}$ POR threshold, falling		2	2.25	2.45	V
$V_{(AC_REG)}$	Regulated Forward $V_{(A)}$–$V_{(C)}$ Threshold		3.6	10.5	13.4	mV
$V_{(AC_REV)}$	$V_{(A)}$–$V_{(C)}$ Threshold for Fast Reverse Current Blocking		–16	–10.5	–5	mV
$V_{(AC_FWD)}$	$V_{(A)}$–$V_{(C)}$ Threshold for Reverse to Forward transition		150	177	200	mV
$V_{(DGATE)}$ – $V_{(A)}$	Gate Drive Voltage	3 V < $V_{(S)}$ < 5 V	7			V
		5 V < $V_{(S)}$ < 65 V	9.2	11.5	14	V
$I_{(DGATE)}$	Peak Gate Source current	$V_{(A)}$ – $V_{(C)}$ = 100 mV, $V_{(DGATE)}$ – $V_{(A)}$ = 1 V		18.5		mA
	Peak Gate Sink current	$V_{(A)}$ – $V_{(C)}$ = –12 mV, $V_{(DGATE)}$ – $V_{(A)}$ = 11 V		2670		mA
	Regulation sink current	$V_{(A)}$ – $V_{(C)}$ = 0 V, $V_{(DGATE)}$ – $V_{(A)}$ = 11 V	5	13.5		µA
$I_{(C)}$	Cathode leakage Current	$V_{(A)}$ = –14 V, $V_{(C)}$ = 12 V	4	9	32	µA
HIGH SIDE CONTROLLER (HGATE, OUT)						
$V_{(HGATE)}$ – $V_{(OUT)}$	Gate Drive Voltage	3 V < $V_{(S)}$ < 5 V	7			V
		5 V < $V_{(S)}$ < 65 V	10	11.1	14.5	V
$I_{(HGATE)}$	Source Current		39	55	75	µA
	Sink Current	$V_{(OV)}$ > $V_{(OVR)}$	128	180		mA
SLEEP MODE						
$V_{(\overline{SLEEP}R)}$	$\overline{SLEEP}$ high threshold voltage			0.85	1.05	V
$V_{(\overline{SLEEP}F)}$	$\overline{SLEEP}$ threshold voltage for low Iq shutdown, falling		0.41	0.7		V
$I_{(\overline{SLEEP})}$	$\overline{SLEEP}$ input leakage current			100	160	nA
Overvoltage threshold	SLEEP mode overvoltage rising threshold	$\overline{SLEEP}$=Low, EN=High	19.3	21.3	23	V
Overvoltage threshold	SLEEP mode overvoltage threshold	$\overline{SLEEP}$=Low, EN=High	18.4	21	22.2	V
Overcurrent threshold	SLEEP mode overcurrent threshold (device Latch-off)		150	250	310	mA
$T_{(TSD)}$	SLEEP mode TSD Threshold, rising	$\overline{SLEEP}$=Low, EN=High		155		℃
$T_{(TSDhyst)}$	TSD Hysteresis	$\overline{SLEEP}$=Low, EN=High		10		℃

7.6 Switching Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(OUT)}$ = $V_{(VS)}$ = 12 V, $C_{(CAP)}$ = 0.1 µF, $V_{(EN)}$, $V_{(SLEEP)}$= 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DGATE_OFF(dly)}$	DGATE Turnoff Delay during reverse voltage detection	$V_{(A)}$ – $V_{(C)}$ = +30 mV to –100 mV to $V_{(DGATE–A)}$ < 1 V, $C_{(DGATE–A)}$ = 10 nF		0.5	0.95	µs
$t_{DGATE_ON(dly)}$	DGATE Turnon Delay during forward voltage detection	$V_{(A)}$ – $V_{(C)}$ = –20 mV to +700 mV to $V_{(DGATE-A)}$ > 5 V, $C_{(DGATE-A)}$ = 10 nF,LM74900-Q1 only		2	3.8	µs
$t_{DGATE_ON(dly)}$	DGATE Turnon Delay during forward voltage detection	$V_{(A)}$ – $V_{(C)}$ = –20 mV to +700 mV to $V_{(DGATE-A)}$ > 5 V, $C_{(DGATE-A)}$ = 10 nF, LM74910-Q1 only		0.75	1.6	µs

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7.6 Switching Characteristics (continued)

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(OUT)}$ = $V_{(VS)}$ = 12 V, $C_{(CAP)}$ = 0.1 µF, $V_{(EN)}$, $V_{(SLEEP)}$= 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{EN(dly)_DGATE}$	DGATE Turnon Delay during EN	EN ↑ to $V_{(DGATE-A)}$ > 5 V, $C_{(DGATE-A)}$ = 10 nF		180	270	µs
$t_{UVLO_OFF(deg)_HGATE}$	HGATE Turnoff Deglitch during UVLO	UVLO ↓ to HGATE ↓		5	7	µs
$t_{UVLO_ON(deg)_HGATE}$	HGATE Turnon Deglitch during UVLO	UVLO ↑ to HGATE ↑		8.5		µs
$t_{OVP_OFF(deg)_HGATE}$	HGATE Turnoff Deglitch during OV	OV ↑ to HGATE ↓		4	7	µs
$t_{OVP_ON(deg)_HGATE}$	HGATE Turnon Deglitch during OV	OV ↓ to HGATE ↑		9		µs
t_{SCP_DLY}	Short circuit protection turn off delay	(V_{ISCP} - V_{CS}-) = 0 mv to 100 mV HGATE↓, C_{GS} = 4.7 nF		3	5.5	µs
$t_{OCP_TMR_DLY}$	Over current protection turn off delay	(V_{CS+} - V_{CS-})↑ HGATE↓, C_{TMR} = 50 pF		35		µs
	Over current protection turn off delay	(V_{CS+} - V_{CS-})↑ HGATE↓, C_{TMR} = 10 nF		190		µs
$t_{AUTO_RETRY_DLY}$	Over current / Short circuit protection auto retry delay	(V_{CS+} - V_{CS-}) ↓ HGATE ↑, C_{TMR} = 50 pF		1.5		ms
	Over current / Short circuit protection auto retry delay	(V_{CS+} - V_{CS-}) ↓ HGATE ↑, C_{TMR} = 10 nF		230		ms
t_{FLT_ASSERT}	Fault assert delay	(V_{CS+} - V_{CS-})↑ $\overline{FLT}$↓, C_{TMR} = 50 pF		35		µs
	Fault assert delay	OV ↑ to $\overline{FLT}$ ↓		3		µs
$t_{FLT_DE-ASSERT}$	Fault de-assert delay			4		µs
$t_{SLEEP_OCP_LATCH}$	SLEEP OCP Latch delay			3.5	7.5	µs
t_{SLEEP_MODE}	Sleep Mode Entry Delay	$\overline{SLEEP}$=Low, EN=High		95		µs
$t_{OVCLAMP}$	OV clamp response delay			3.5		µs

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7.7 Typical Characteristics

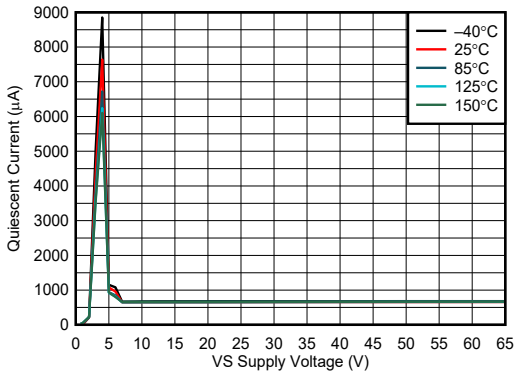


Figure 7-1. Operating Quiescent Current vs Supply Voltage

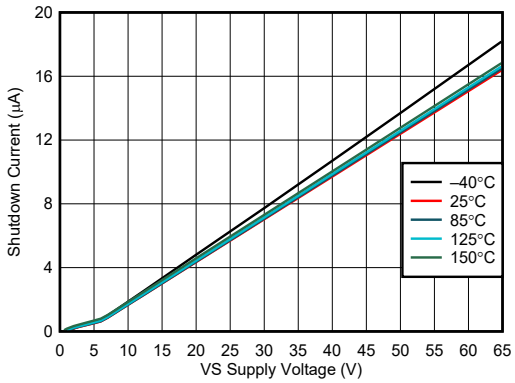


Figure 7-2. Shutdown Current vs Supply Voltage

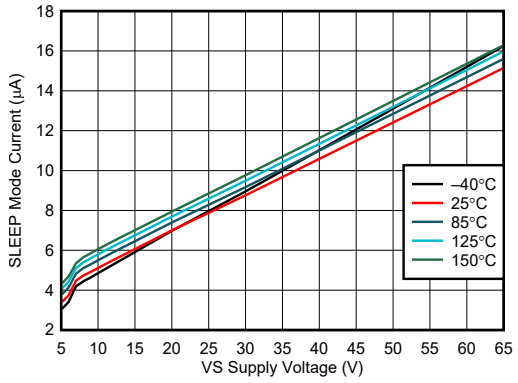


Figure 7-3. SLEEP Mode Current vs Supply Voltage

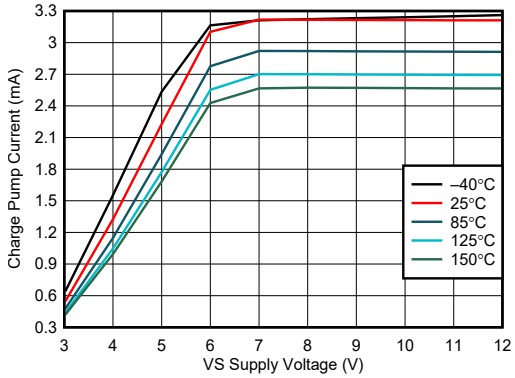


Figure 7-4. Charge Pump Current vs Supply Voltage at CAP – VS ≥ 6 V (LM74900-Q1)

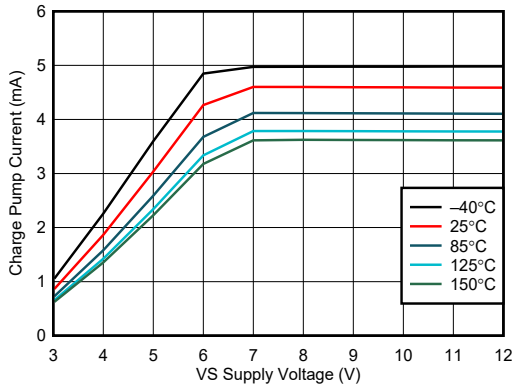


Figure 7-5. Charge Pump Current vs Supply Voltage at CAP – VS ≥ 6 V (LM74910-Q1)

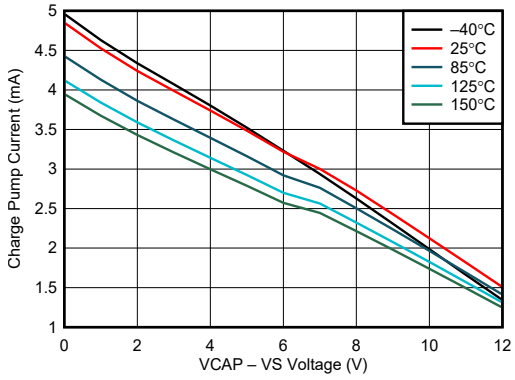


Figure 7-6. Charge Pump V-I Characteristics at VS ≥ 12 V (LM74900-Q1)

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7.7 Typical Characteristics (continued)

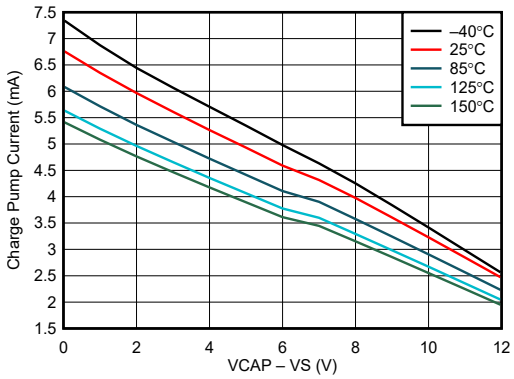


Figure 7-7. Charge Pump V-I Characteristics at VS ≥ 12 V (LM74910-Q1)

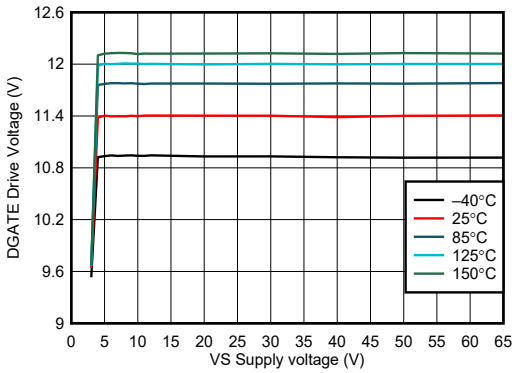


Figure 7-8. DGATE Drive Voltage vs Supply Voltage

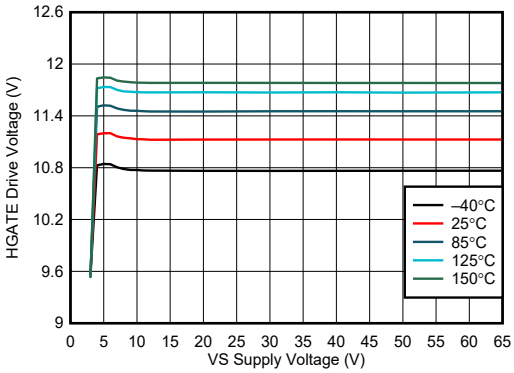


Figure 7-9. HGATE Drive Voltage vs Supply Voltage

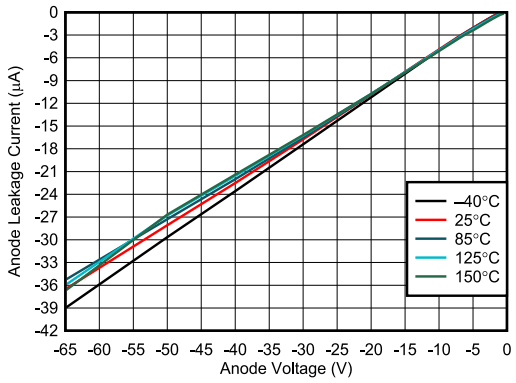


Figure 7-10. ANODE Leakage Current vs Reverse ANODE Voltage

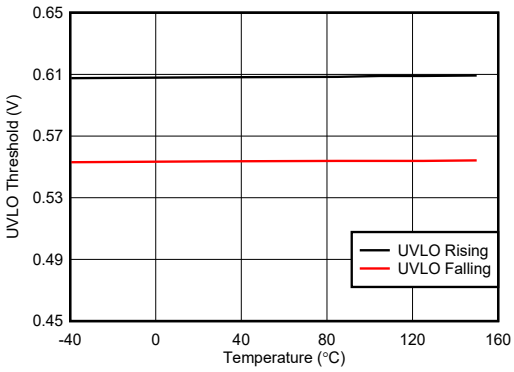


Figure 7-11. UVLO Thresholds vs Temperature

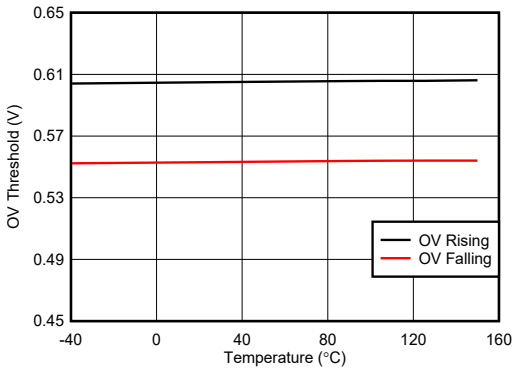


Figure 7-12. OVP Thresholds vs Temperature

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7.7 Typical Characteristics (continued)

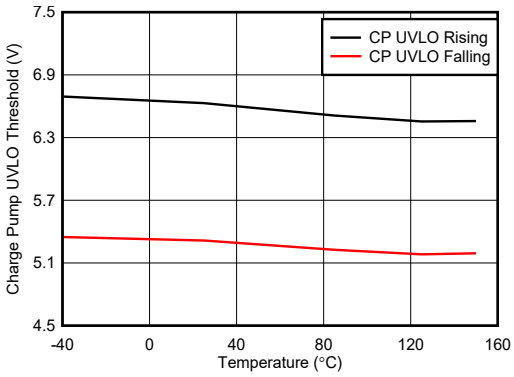


Figure 7-13. Charge Pump UVLO Threshold vs Temperature

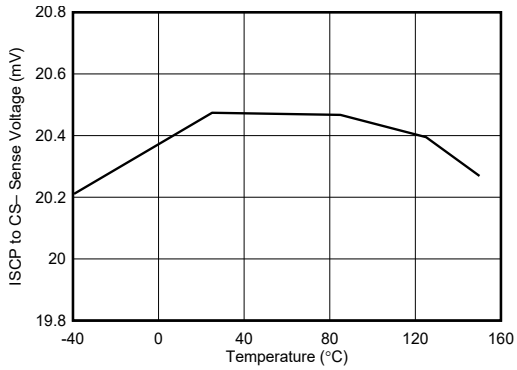


Figure 7-14. ISCP to CS– Threshold vs Temperature

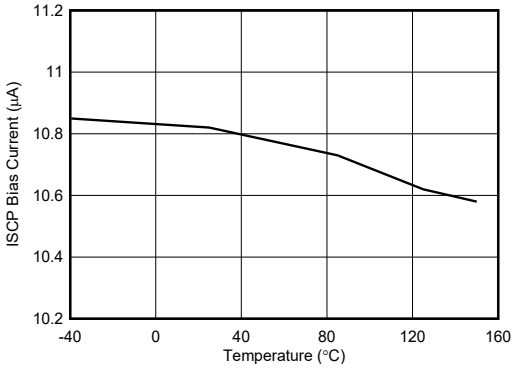


Figure 7-15. ISCP Bias Current vs Temperature

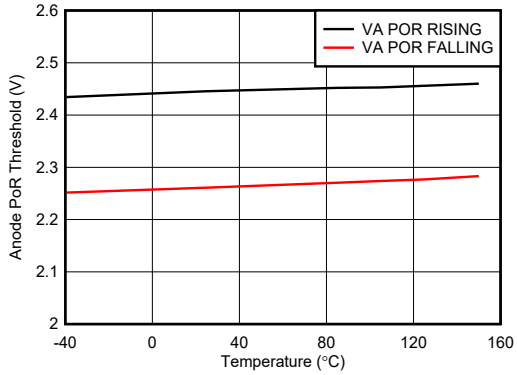


Figure 7-16. VA POR Threshold vs Temperature

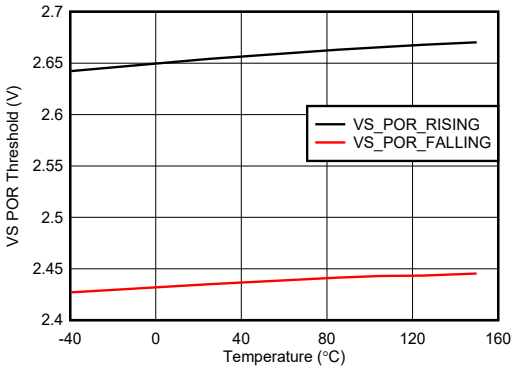


Figure 7-17. VS POR Threshold vs Temperature

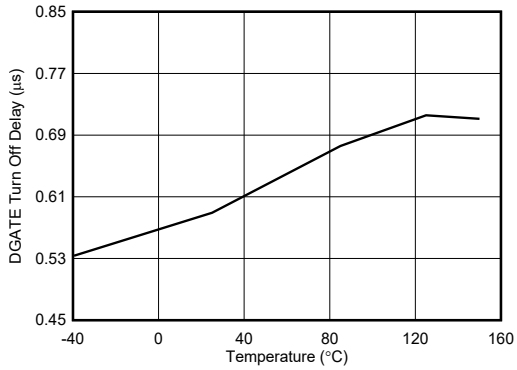


Figure 7-18. DGATE Turn OFF Delay

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7.7 Typical Characteristics (continued)

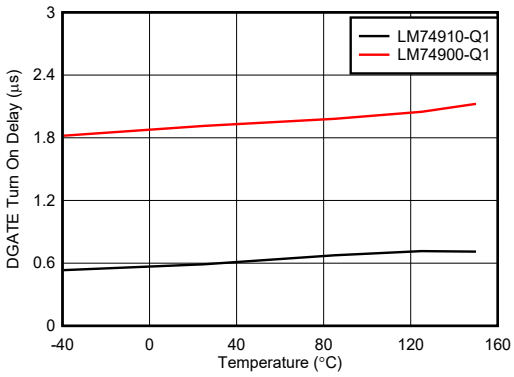


Figure 7-19. DGATE Turn On Delay During Forward Conduction

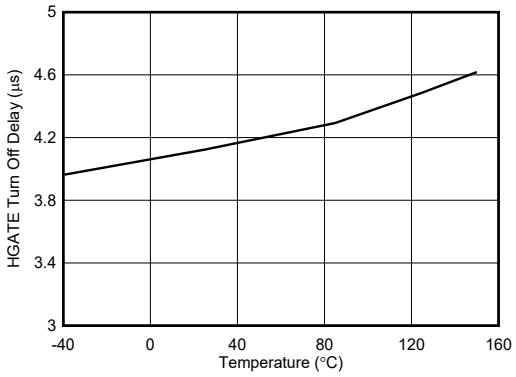


Figure 7-20. HGATE Turn OFF Delay During OV

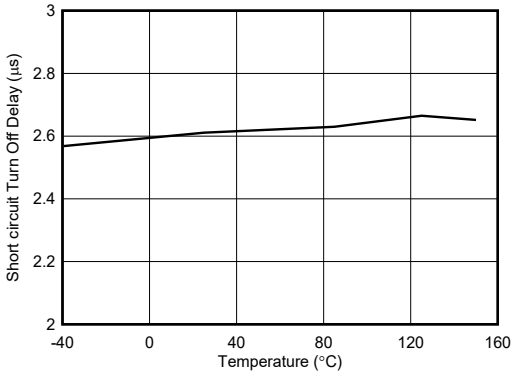


Figure 7-21. HGATE Turn OFF Delay During SCP

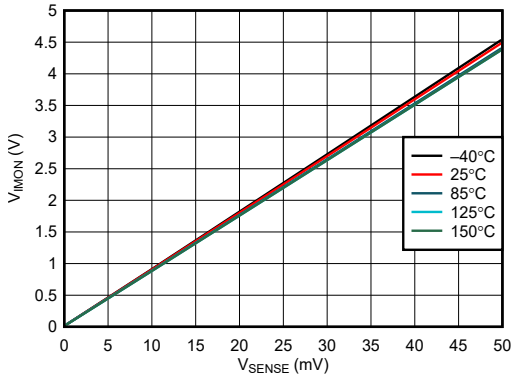


Figure 7-22. Current Monitor Output vs Sense Voltage (R_{IMON} = 5kΩ, R_{SET} = 50Ω)

8 Parameter Measurement Information

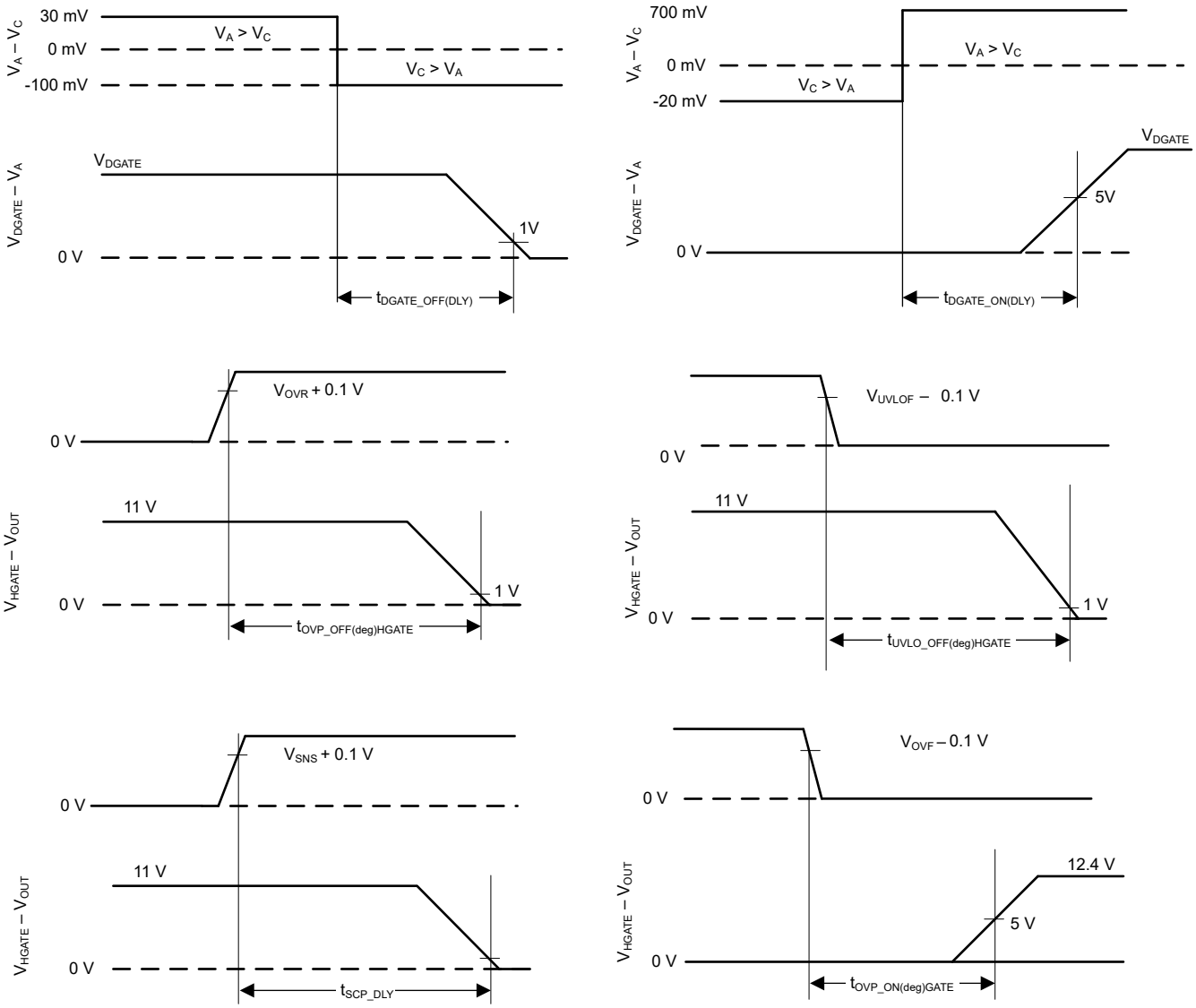


Figure 8-1. Timing Waveforms

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9 Detailed Description

9.1 Overview

The LM749x0-Q1 family of ideal diode controllers drive back-to-back external N-Channel MOSFETs to realize low-loss power path protection with circuit breaker, undervoltage, and overvoltage protection functionality.

The wide input supply of 3 V to 65 V allows protection and control of 12-V and 24-V automotive battery powered ECUs. The device can withstand and protect the loads from negative supply voltages down to –65 V. An integrated ideal diode controller (DGATE) drives the first MOSFET to replace a Schottky diode for reverse input protection and output voltage holdup. With a second MOSFET in the power path the device allows load disconnect (ON/OFF control) and overvoltage protection using HGATE control. The device features an adjustable overvoltage cut-off protection feature. With common drain configuration of the power MOSFETs, the mid-point can be utilized for OR-ing designs using another ideal diode. The LM749x0-Q1 has a maximum voltage rating of 65 V.

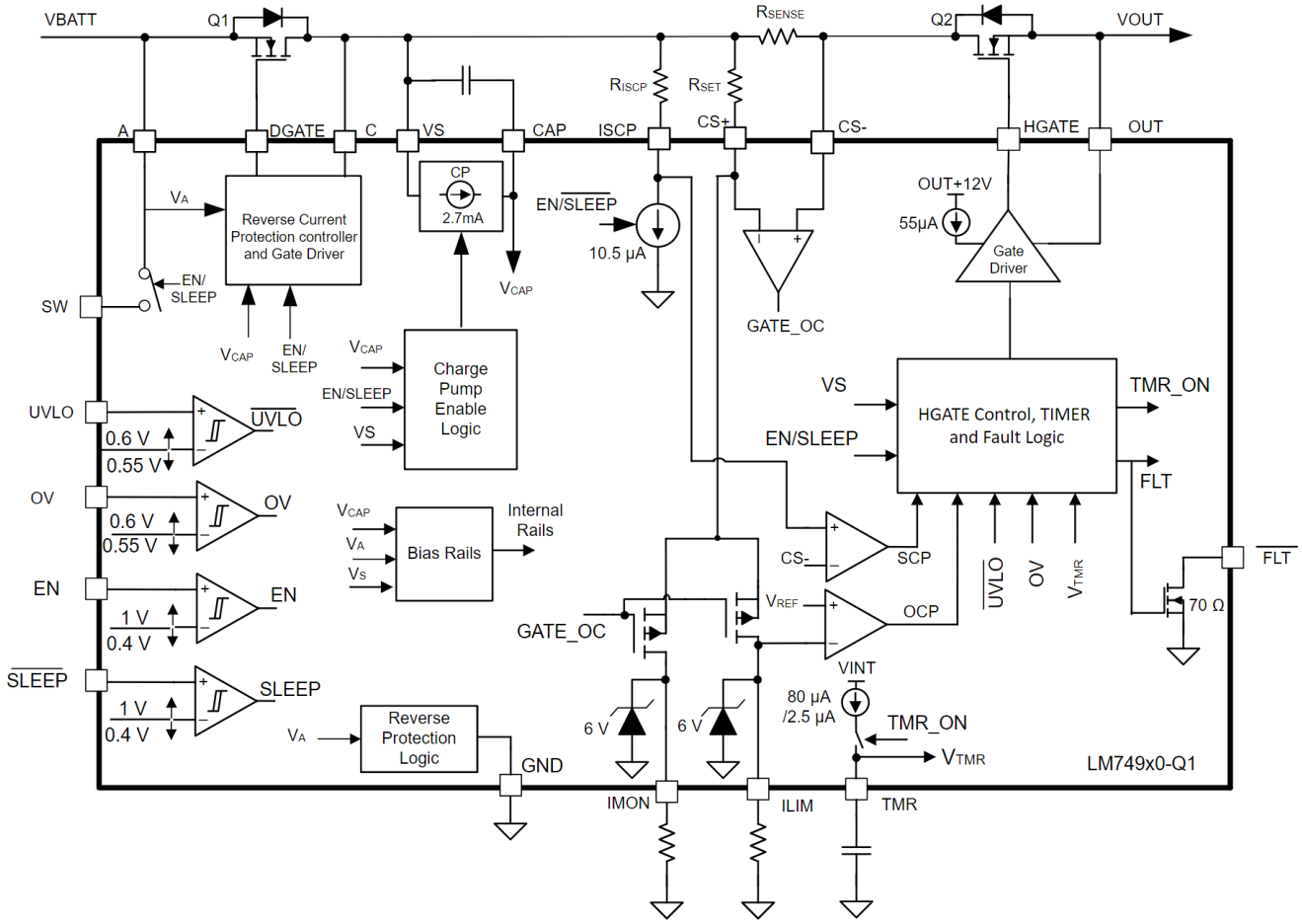
The device has accurate current sensing output (IMON) with typical accuracy of (±10%) enabling systems for energy management. It has integrated two level overcurrent protection with circuit breaker functionality (TMR) and fault ($\overline{FLT}$) output with complete adjustability of thresholds and response time. Auto-retry and latch-off fault behavior can be configured.

The device offers adjustable overvoltage and undervoltage protection, providing robust load disconnect in case of voltage transient events.

LM749x0-Q1 features two different low power modes based on status of EN and $\overline{SLEEP}$ pin. In SLEEP mode ($\overline{SLEEP}$ = Low, EN = High) the device consumes only 6-µA current by turning off both the external MOSFET gate drives and internal charge pump but at the same time providing internal bypass path to power up always ON loads with limited current capacity. With the enable pin low, device enters into ultra-low-power mode by completely cutting off loads with typical current consumption of 2.87 µA. The high voltage rating of LM749x0-Q1 helps to simplify the system designs for automotive ISO7637 protection. The LM749x0-Q1 is also suitable for ORing and priority power MUX applications.

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9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Charge Pump

The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external charge pump capacitor is placed between CAP and VS pins to provide energy to turn on the external MOSFET. In order for the charge pump to supply current to the external capacitor, the EN and $\overline{\text{SLEEP}}$ pin voltage must be above the specified input high threshold. When enabled the charge pump sources a charging current of 2.7-mA typical. If EN and $\overline{\text{SLEEP}}$ pin is pulled low, then the charge pump remains disabled. To ensure that the external MOSFET can be driven above its specified threshold voltage, the CAP to VS voltage must be above the undervoltage lockout threshold, typically 6.6 V, before the internal gate driver is enabled. Use Equation 1 to calculate the initial gate driver enable delay.

$$T_{(DRV_EN)} = 175\ \mu s + \frac{C_{(CAP)} \times V_{(CAP_UVLOR)}}{2.7\ mA} \quad (1)$$

where

- $C_{(CAP)}$ is the charge pump capacitance connected across VS and CAP pins
- $V_{(CAP_UVLOR)}$ = 6.6 V (typical)

To remove any chatter on the gate drive approximately 1 V of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the CAP to VS voltage reaches 13.2 V, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the CAP to VS voltage is below to 12.2 V typically at which point the charge pump is enabled. The voltage

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between CAP and VS continue to charge and discharge between 12.2 V and 13.2 V as shown in Figure 9-1. By enabling and disabling the charge pump, the operating quiescent current of the LM749x0-Q1 is reduced. When the charge pump is disabled it sinks 15 µA.

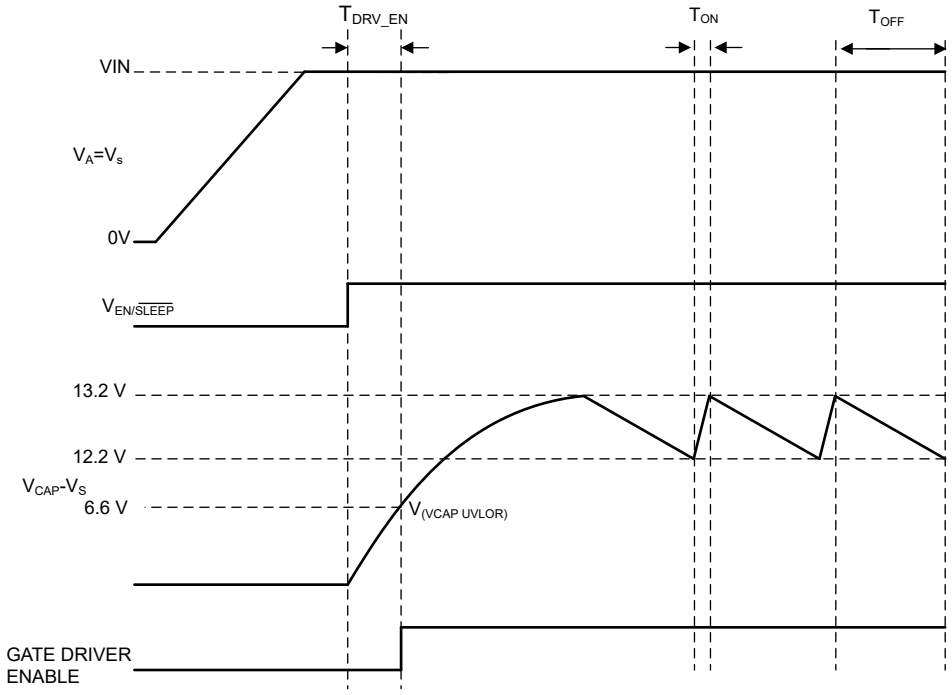


Figure 9-1. Charge Pump Operation

9.3.2 Dual Gate Control (DGATE, HGATE)

The LM749x0-Q1 features two separate gate control and driver outputs i.e DGATE and HGATE to drive back to back N-channel MOSFETs.

9.3.2.1 Reverse Battery Protection (A, C, DGATE)

A, C, DGATE comprises of Ideal Diode stage. Connect the Source of the external MOSFET to A, Drain to C and Gate to DGATE. The LM749x0-Q1 has integrated reverse input protection down to –65 V.

Before the DGATE driver is enabled, following conditions must be achieved:

- The EN and $\overline{\text{SLEEP}}$ pin voltage must be greater than the specified input high voltage.
- The CAP to VS voltage must be greater than the undervoltage lockout voltage.
- Voltage at A pin must be greater than VA POR Rising threshold.
- Voltage at VS pin must be greater than Vs POR Rising threshold.

If the above conditions are not achieved, then the DGATE pin is internally connected to the A pin, assuring that the external MOSFET is disabled.

In LM749x0-Q1 the voltage drop across the MOSFET is continuously monitored between the A and C pins, and the DGATE to A voltage is adjusted as needed to regulate the forward voltage drop at 10.5 mV (typ). This closed loop regulation scheme enables graceful turn off of the MOSFET during a reverse current event and ensures zero DC reverse current flow. This scheme ensures robust performance during slow input voltage ramp down tests. Along with the linear regulation amplifier scheme, the LM749x0-Q1 also integrates a fast reverse voltage comparator. When the voltage drop across A and C reaches $V_{(AC_REV)}$ threshold then the DGATE goes low within 0.5-µs (typ). This fast reverse voltage comparator scheme ensures robust performance during fast input voltage ramp down tests such as input micro-shorts. The external MOSFET is turned ON back when the voltage across A and C hits $V_{(AC_FWD)}$ threshold within 2.8 µs (typ).

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9.3.2.2 Load Disconnect Switch Control (HGATE, OUT)

HGATE and OUT comprises of Load disconnect switch control stage. Connect the Source of the external MOSFET to OUT and Gate to HGATE.

Before the HGATE driver is enabled, following conditions must be achieved:

- The EN and $\overline{\text{SLEEP}}$ pin voltage must be greater than the specified input high voltage.
- The CAP to VS voltage must be greater than the undervoltage lockout voltage.
- Voltage at VS pin must be greater than Vs POR Rising thershold.

If the above conditions are not achieved, then the HGATE pin is internally connected to the OUT pin, assuring that the external MOSFET is disabled.

For Inrush Current limiting, connect C_{dVdT} capacitor and R_1 as shown in Figure 9-2.

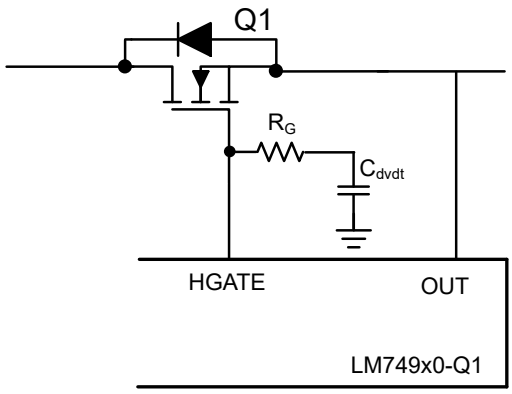


Figure 9-2. Inrush Current Limiting

The C_{dVdT} capacitor is required for slowing down the HGATE voltage ramp during power up for inrush current limiting. Use Equation 2 to calculate C_{dVdT} capacitance value .

$$C_{(dVdT)} = C_{OUT} \times \frac{I_{(HGATE_DRV)}}{I_{INRUSH}} \tag{2}$$

where I_{HATE_DRV} is 55 µA (typ), I_{INRUSH} is the inrush current and C_{OUT} is the output load capacitance. An extra resistor, R_1, in series with the C_{dVdT} capacitor improves the turn off time.

9.3.3 Overcurrent Protection (CS+, CS-, ILIM, IMON, TMR)

LM749x0 has two level overcurrent protection. The device senses the voltage across the external current sense resistor through CS+ and CS–.

9.3.3.1 Pulse Overload Protection, Circuit Breaker

LM749x0-Q1 provides programmable overcurrent threshold setting by means of resistor (R_{LIM}) connected from I_{LIM} pin to GND.

$$R_{(ILIM)} = \frac{12 \times R_{SET}}{R_{SENSE} \times I_{LIM}} \tag{3}$$

where

- R_{SET} is the resistor connected across CS+ and VS
- R_{SNS} is the current sense resistor
- I_{LIM} is the overcurrent level

The C_{TMR} programs the circuit breaker and auto-retry time. Once the voltage across CS+ and CS– exceeds the set point, the C_{TMR} starts charging with 85-µA pull up current. Once the C_{TMR} charges to V_{TMR_FLT}, $\overline{\text{FLT}}$ asserts

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low providing warning on impending FET turn OFF. Once C_{TMR} charges to V_{TMR_OC}, HGATE is pulled to OUT turning OFF the HFET. After this event, the auto-retry behavior starts. The C_{TMR} capacitor starts discharging with 2.7-µA pull down current. Once the voltage reaches VTMR_Low level, the capacitor starts charging with 2.7-µA pull up. After 32 charging/discharging cycles of C_{TMR}, the FET turns ON and $\overline{FLT}$ de-asserts after de-assertion delay.

$$T_{(OC)} = 1.2 \times \frac{C_{TMR}}{82.3\ \mu A} \quad (4)$$

where

- T_{OC} is the delay to turn OFF the FET
- C_{TMR} is the capacitance across TMR to GND

The auto-retry time can be computed as

$$T_{RETRY} = 22.7 \times 10^{6} \times C_{TMR} \quad (5)$$

If the overcurrent pulse duration is below T_{OC} then the FET remains ON and C_{TMR} gets discharged using internal pull down switch.

When not used, ILIM is connected to ground while TMR can be left floating.

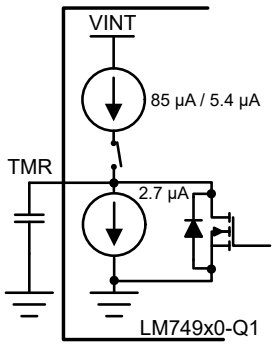


Figure 9-3. LM749x0 Auto Retry TIMER Functionality

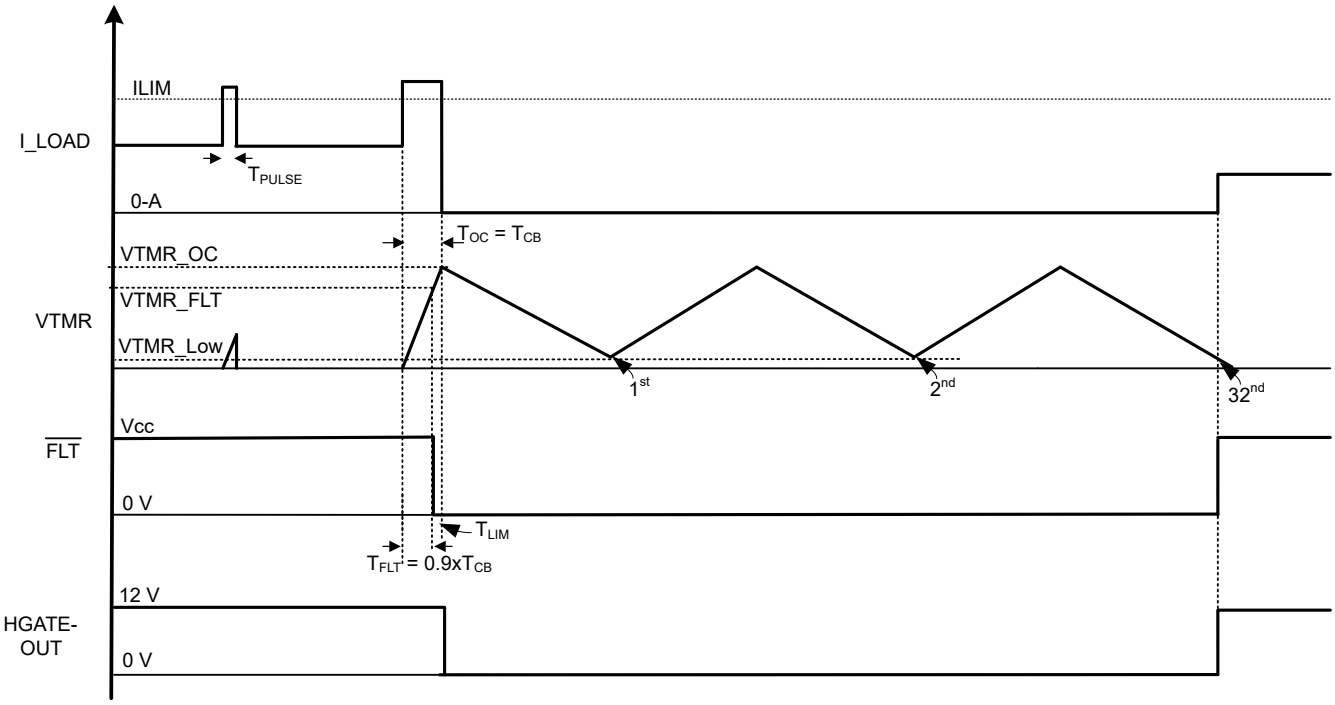


Figure 9-4. Overcurrent Protection With Auto Retry Timing Diagram

If the overcurrent pulse duration is below T_{OC} then the HFET remains ON and C_{TMR} gets discharged using internal pull down switch.

9.3.3.2 Overcurrent Protection With Latch-Off

With about a 100-kΩ resistor across C_{TMR} as shown in figure, overcurrent latch-off functionality can be achieved. With this resistor, during the charging cycle the voltage across C_{TMR} gets clamped to a level below V_{TMR_OC} resulting in a latch-off behavior.

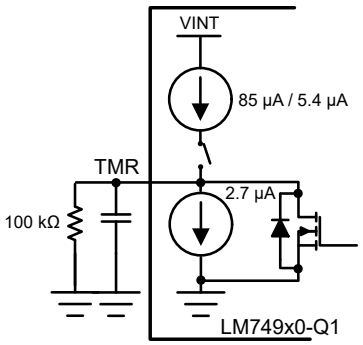


Figure 9-5. LM749x0 Overcurrent Protection With Latch

Toggle EN (below ENF) or power cycle Vs below V_{SPORF} to reset the latch. At low edge, the timer counter is reset and C_{TMR} is discharged.

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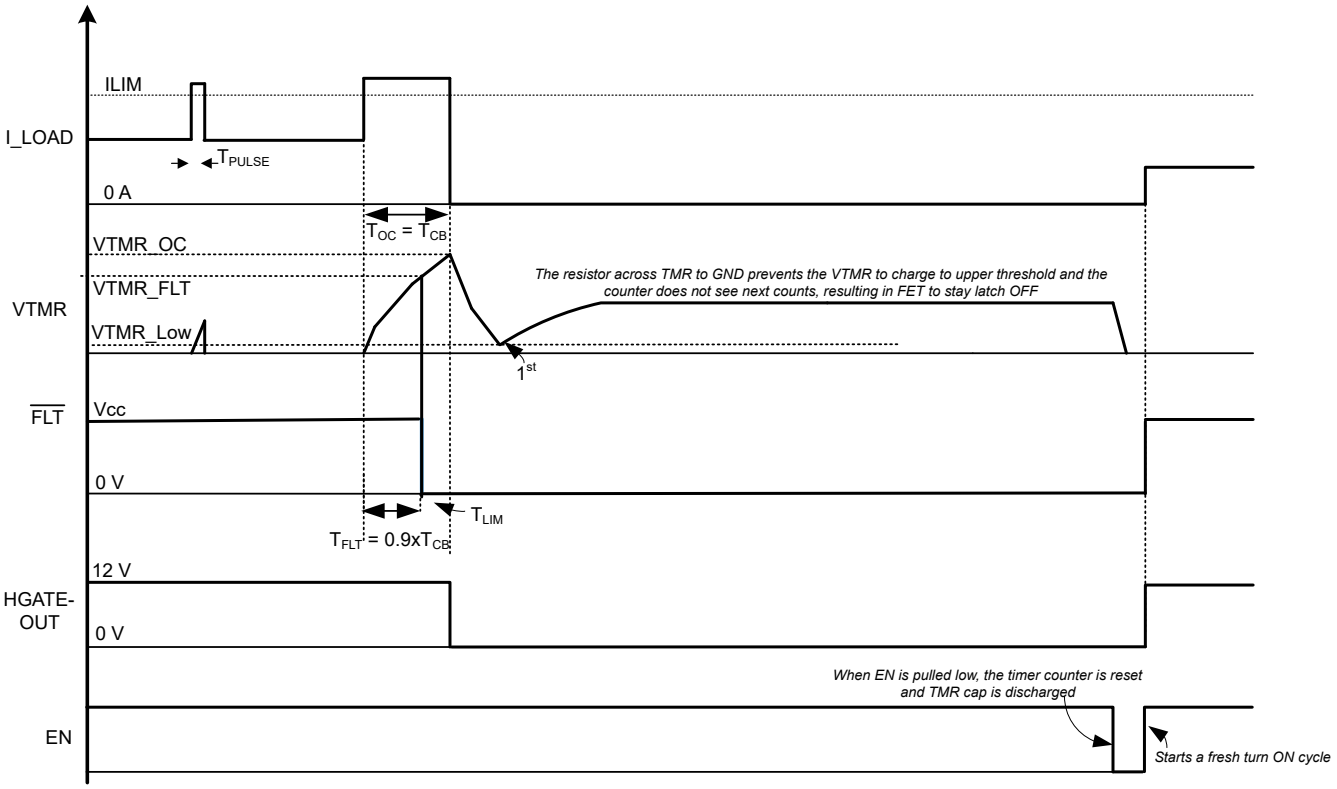


Figure 9-6. Overcurrent Protection With Latch Timing Diagram

9.3.3.3 Short Circuit Protection (ISCP)

LM749x0-Q1 offers fast response to any short circuit events with the short circuit protection feature. Once the voltage across CS+ and CS– exceeds the ISCP set point of 20-mV typical (default threshold), HGATE is pulled to OUT within 5 µs protecting the HFET. $\overline{FLT}$ asserts low at the same time. Subsequent to this event, the charge/discharge cycles of C_{TMR} starts similar to the behavior post FET OFF event in circuit breaker operation.

Short circuit protection threshold can be increased using an external series resistor (R_{ISCP}) from ISCP pin to common drain point. The shift in the short circuit protection threshold can be calculated using Equation 6.

$$V_{SNS_SCP} = (10.5\ \mu A \times R_{ISCP}) + 20\ mV \quad (6)$$

An additional deglitch filter consisting of R_{SCP} and C_{SCP} can be added from ISCP pin to CS– pin as shown in Figure 9-7 to avoid any false short circuit trigger in case of fast automotive transients such as Input Micro cuts (LV124, E-10), AC superimpose (LV124, E-06), ISO7637-2 Pulse 2A.

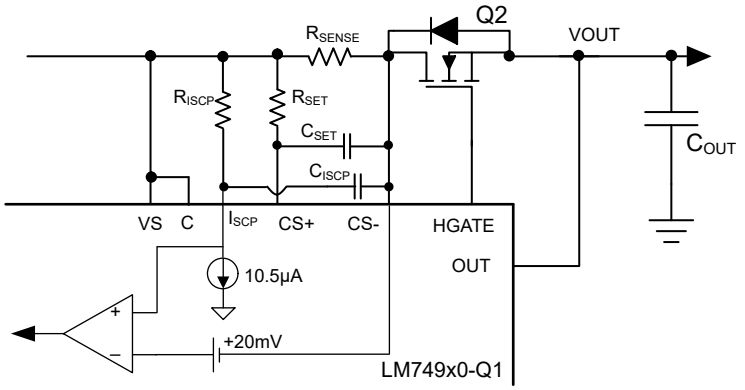


Figure 9-7. Short Circuit Protection With Deglitch Filter

Latch off can also achieved in the similar way as explained in the circuit breaker section.

9.3.3.4 Analog Current Monitor Output (IMON)

LM749x0 features analog load current monitor output (IMON) with adjustable gain. The resistor connected from IMON pin to ground sets the current monitor output voltage given by Equation 7.

$$V_{IMON} = \frac{0.9 \times V_{SENSE} \times R_{IMON}}{R_{SET}} \quad (7)$$

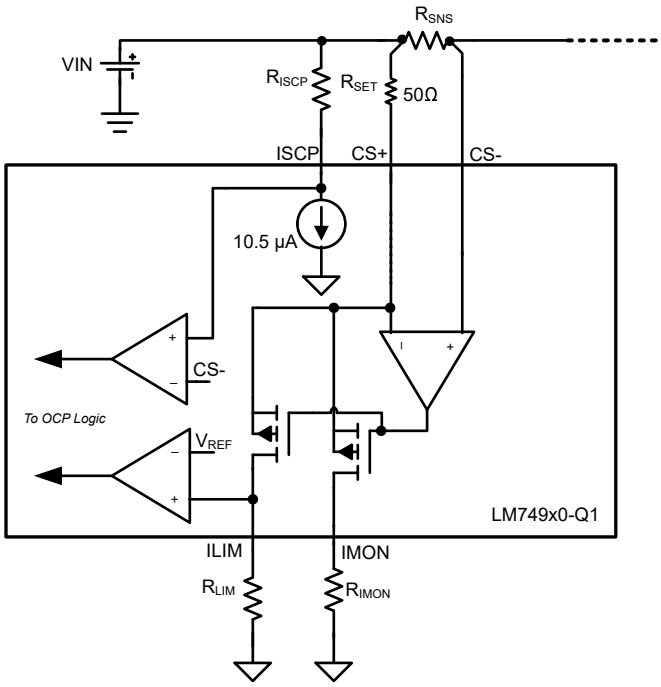


Figure 9-8. Analog Current Monitoring

9.3.4 Undervoltage Protection, Overvoltage Protection, and Battery Voltage Sensing (UVLO, OV, SW)

Connect a resistor ladder as shown in Figure 9-9 for overvoltage threshold programming.

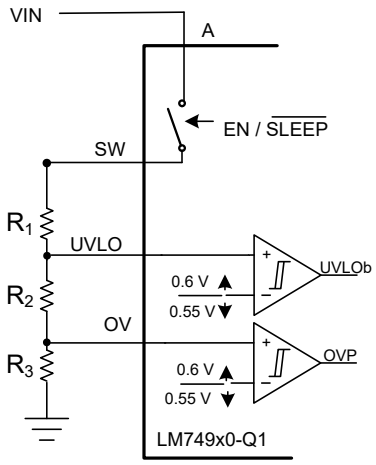


Figure 9-9. Programming Overvoltage Threshold and Battery Sensing

A disconnect switch is integrated between A and SW pins. This switch is turned OFF when EN or $\overline{\text{SLEEP}}$ pin is pulled low. This helps to reduce the leakage current through the resistor divider network during system shutdown state (IGN_OFF state).

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When undervoltage functionality is not required then it is recommended to connect UVLO pin to EN or VS. It is recommended to connect OV pin to ground when overvoltage protection feature is not used.

9.3.5 Low IQ SLEEP Mode ($\overline{\text{SLEEP}}$)

LM749x0-Q1 supports low IQ SLEEP mode operation. This mode can be enabled by pulling $\overline{\text{SLEEP}}$ pin low (EN = High). In SLEEP mode, device turns off internal charge pump, SW switch and disables DGATE and HGATE drive thus achieving low current consumption of 6-µA typical. However at the same time device power up always on loads connected on OUT pin through an internal low power MOSFET with typical on resistance of 7 Ω. In this mode device can support peak load current of 100 mA. As load is increased, voltage drop across internal MOSFET increases. Device offers overcurrent protection during sleep mode with typical overcurrent threshold of 250 mA. In case of overcurrent event during sleep mode, device protects internal FET by disconnecting the internal MOSFET switch and latching off the device. As an additional layer of protection, device also features thermal shutdown with latch off feature in SLEEP mode in case of any overheating of the device in SLEEP mode. To put the device out of the latch mode user has to toggle the $\overline{\text{SLEEP}}$ or EN pin.

In SLEEP mode LM749x0-Q1 offers protection against input overvoltage events. Device can be configured in either overvoltage cut-off (SLEEP_OV connected to C) or overvoltage clamp mode (SLEEP_OV connected to VOUT) with default overvoltage threshold of 21-V typical.

If SLEEP mode feature is not required then $\overline{\text{SLEEP}}$ pin should be tied to EN. When not used SLEEP_OV pin can be left floating.

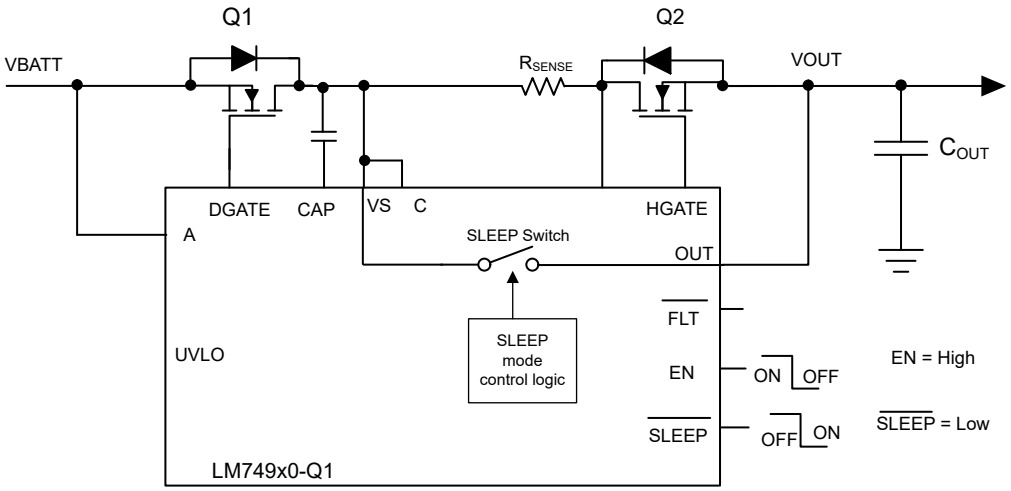


Figure 9-10. LM749x0-Q1 SLEEP Mode Operation

A higher overvoltage threshold for SLEEP mode can be achieved by adding an external Zener diode between SLEEP_OV pin to OUT/C as shown in Figure 9-11. This feature is useful while configuring overvoltage threshold for 24-V or 48-V powered systems.

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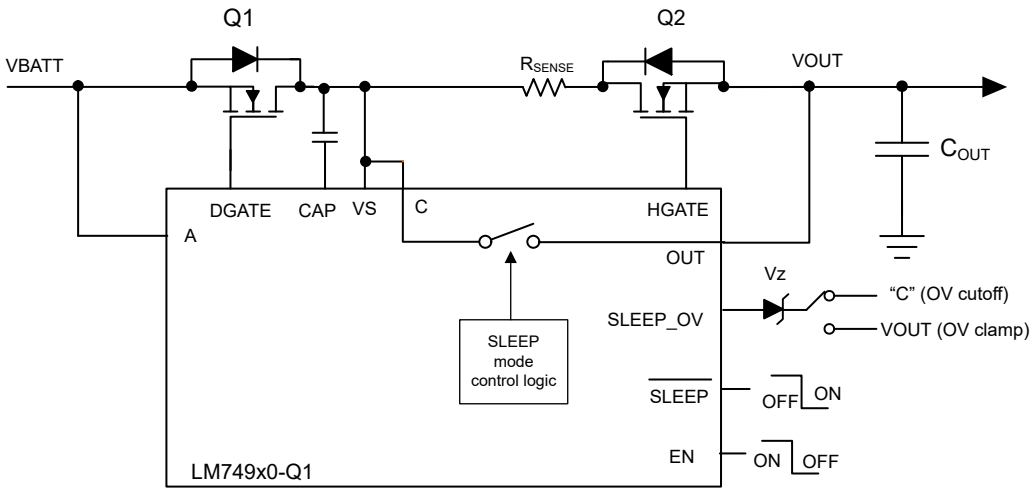


Figure 9-11. Increasing SLEEP_OV Threshold Using an External Zener Diode

9.3.6 Ultra Low IQ Shutdown (EN)

The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in *Charge Pump*. If EN pin voltage is less than the input low threshold, $V_{(ENF)}$, the charge pump and both the gate drivers (DGATE and HGATE) are disabled placing the LM749x0-Q1 in shutdown mode with ultra-low-current consumption of 3 µA. The EN pin can withstand a maximum voltage of 65 V. For always ON operation, connect EN pin to VS.

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10 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

LM749x0-Q1 controls two N-channel power MOSFETs with DGATE used to control diode MOSFET to emulate an ideal diode and HGATE controlling second MOSFET for power path cut-off when disabled or during an overcurrent, overvoltage, undervoltage events. HGATE controlled MOSFET can be used to clamp the output during overvoltage or load dump conditions. LM749x0-Q1 can be placed into low quiescent current mode using EN or $\overline{\text{SLEEP}}$, where both DGATE and HGATE are turned OFF.

The device has a separate supply input pin (VS). The charge pump is derived from this supply input. With the separate supply input provision and separate GATE control architecture, the LM749x0-Q1 device drives back to back connected MOSFET in common drain topology thus enabling various system architectures such as power supply ORing and Power supply priority MUX applications. With these various topologies, the system designers can design the front-end power system to meet various system design requirements.

10.2 Typical 12-V Reverse Battery Protection Application

A typical application circuit of LM749x0-Q1 configured in **common-drain topology** to provide reverse battery protection with overvoltage protection is shown in Figure 10-1.

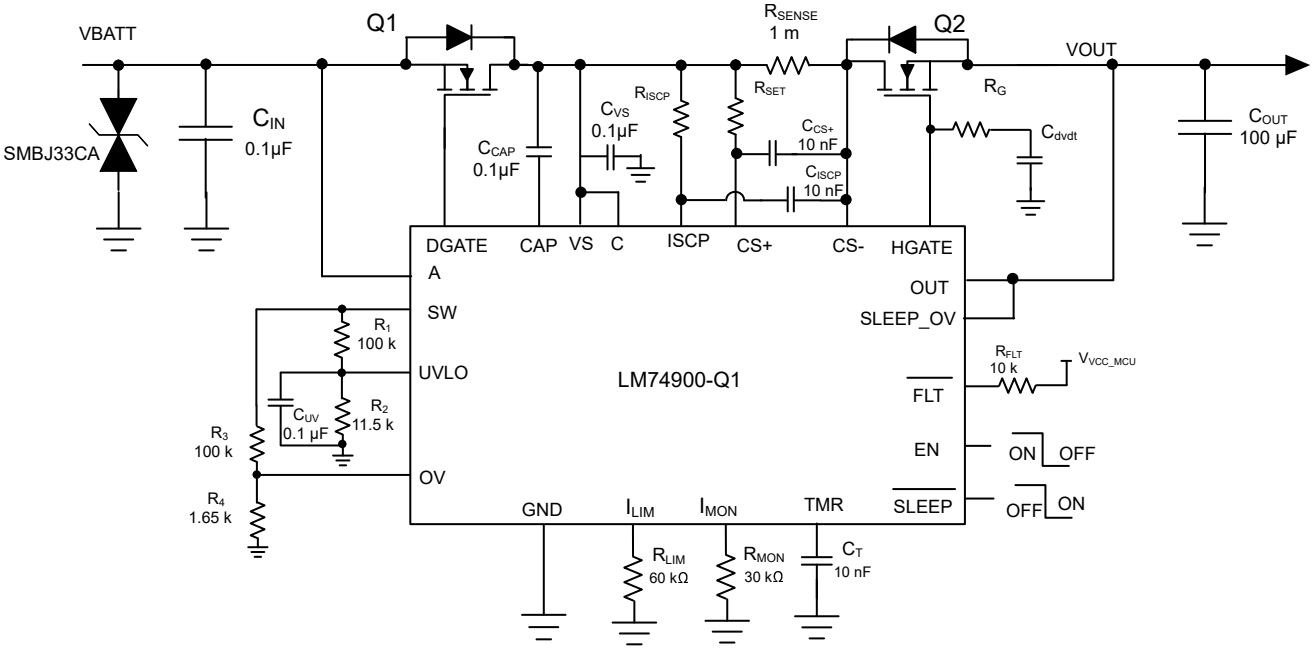


Figure 10-1. Typical Application Circuit – 12-V Reverse Battery Protection, Overcurrent Protection, and Overvoltage Protection

10.2.1 Design Requirements for 12-V Battery Protection

The system design requirements are listed in Table 10-1.

Table 10-1. Design Parameters – 12-V Reverse Battery Protection, Overcurrent Protection, and Overvoltage Protection

DESIGN PARAMETER	EXAMPLE VALUE
Operating input voltage range	12-V battery, 12-V nominal with 3.2-V cold crank and 35-V load dump
Output power	50 W
Output current range	4-A nominal, 5-A maximum
Input capacitance	0.1-µF minimum
Output capacitance	0.1-µF minimum, (optional 100 µF for E-10 functional class A performance)
Short circuit current limit	20 A
Overcurrent limit	10 A
Overvoltage cut-off	37.0 V, output cut-off > 37.0 V
Automotive Transient Immunity Compliance	ISO 7637-2, ISO 16750-2 and LV124

10.2.2 Automotive Reverse Battery Protection

The LM749x0-Q1 feature two separate gate control and driver outputs i.e DGATE and HGATE to drive back to back N-channel MOSFETs. This enables LM749x0-Q1 to provide comprehensive immunity with robust system protection during various automotive transient tests as per ISO 7637-2 and ISO 16750-2 standard as well as other automotive OEM standards. For more information, see the *Automotive EMC-compliant reverse-battery protection with ideal-diode controllers* article.

LM749x0-Q1 gate drive output DGATE controls MOSFET Q1 to provide reverse battery protection and true reverse current blocking functionality. HGATE controls MOSFET Q2 to turn off the power path during input overvoltage condition. Resistor network R1, R2 and R3, R4 connected from SW pin to ground can be configured for undervoltage and overvoltage protection. Bi-directional TVS D1 clamps the automotive transient input voltages on the 12-V battery, both positive and negative transients, to voltage levels safe for MOSFET Q1 and LM749x0-Q1.

Fast reverse current blocking response and quick reverse recovery enables LM749x0-Q1 to turn ON/OFF MOSFET Q1 during AC super imposed input specified by ISO 16750-2 and LV124 E-06 and provide active rectification of the AC input superimposed on DC battery voltage. Fast reverse current blocking response of LM749x0-Q1 helps to turn off MOSFET Q1 during negative transients inputs such as –150-V 2-ms Pulse 1 specified in ISO 7637-2 and input micro short conditions such as LV124 E-10 test.

10.2.2.1 Input Transient Protection: ISO 7637-2 Pulse 1

ISO 7637-2 Pulse 1 specifies negative transient immunity of electronic modules connected in parallel with an inductive load when the battery is disconnected. A typical pulse 1 specified in ISO 7637-2 starts with battery disconnection where supply voltage collapses to 0 V followed by –150 V 2 ms applied with a source impedance of 10 Ω at a slew rate of 1 µs on the supply input. LM749x0-Q1 blocks reverse current and prevents the output voltage from swinging negative, protecting the rest of the electronic circuits from damage due to negative transient voltage. MOSFET Q1 is quickly turned off within 0.5 µs by fast reverse comparator of LM749x0-Q1. A single bi-directional TVS is required at the input to clamp the negative transient pulse within the operating maximum voltage across cathode to anode of 85 V and does not violate the MOSFET Q1 drain-source breakdown voltage rating.

ISO 7637-2 Pulse 1 performance of LM749x0-Q1 is shown in Figure 10-2.

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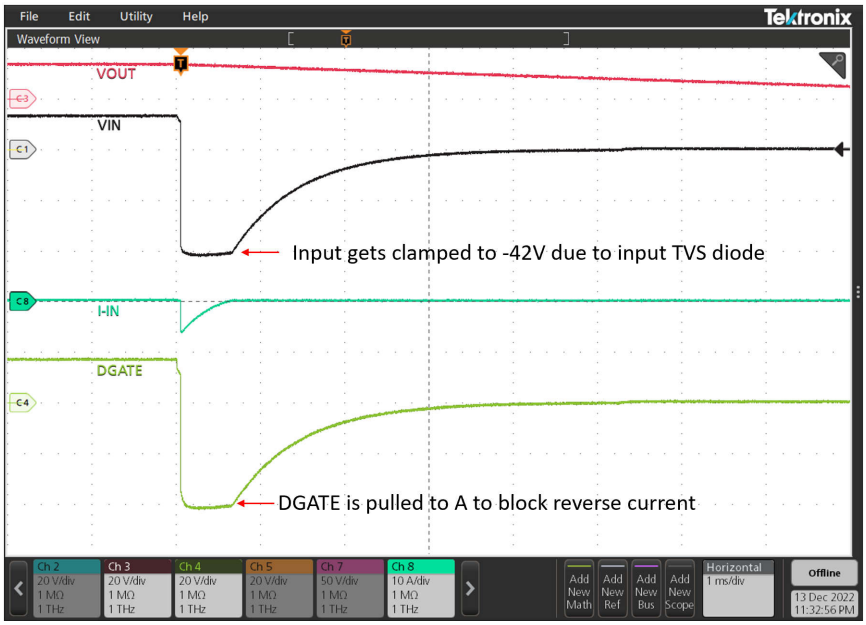


Figure 10-2. ISO 7637-2 Pulse 1

10.2.2.2 AC Super Imposed Input Rectification: ISO 16750-2 and LV124 E-06

Alternators are used to power the automotive electrical system and charge the battery during normal runtime of the vehicle. Rectified alternator output contains residual AC ripple voltage superimposed on the DC battery voltage due to various reasons which includes engine speed variation, regulator duty cycle with field switching ON/OFF and electrical load variations. On a 12-V battery supply, alternator output voltage is regulated by a voltage regulator between 14.5 V to 12.5 V by controlling the field current of alternator's rotor. All electronic modules are tested for proper operation with superimposed AC ripple on the DC battery voltage. AC super imposed test specified in ISO 16750-2 and LV124 E-06 requires AC ripple of 2-V peak-peak on a 13.5-V DC battery voltage, swept from 15 Hz to 30 kHz. LM74900-Q1 rectifies the AC superimposed voltage by turning the MOSFET Q1 OFF quickly to cut-off reverse current and turning the MOSFET Q1 ON quickly during forward conduction. Active rectification of 2-V peak-peak 30-kHz AC input by LM749x0-Q1 is shown in Figure 10-3. LM74910-Q1 has higher DGATE strength and is capable of achieving active rectification at AC superimpose frequency of 200-kHz as shown in Figure 10-4. Fast turn off and quick turn ON of the MOSFET reduces power dissipation in the MOSFET Q1 and active rectification reduces power dissipation in the output hold-up capacitor's ESR by half.

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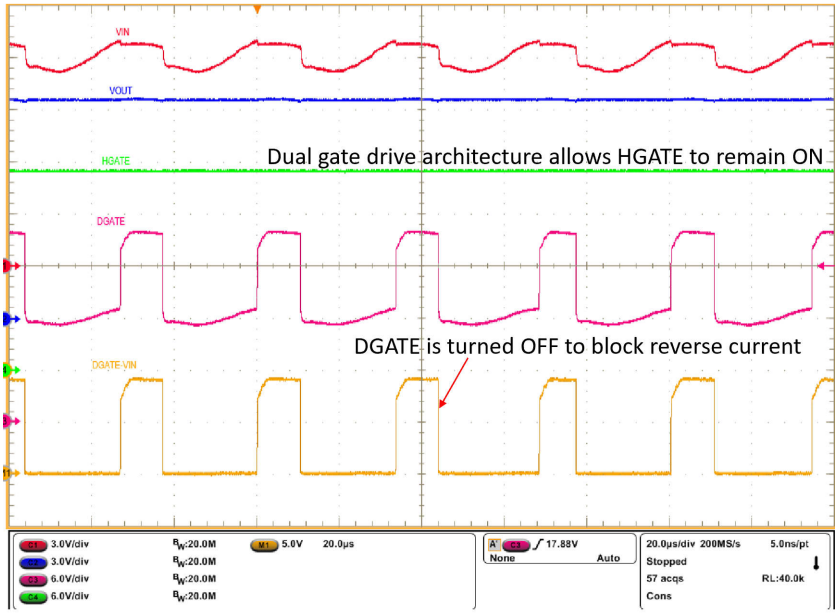


Figure 10-3. AC Super Imposed Test – 2-V Peak-Peak 30 kHz

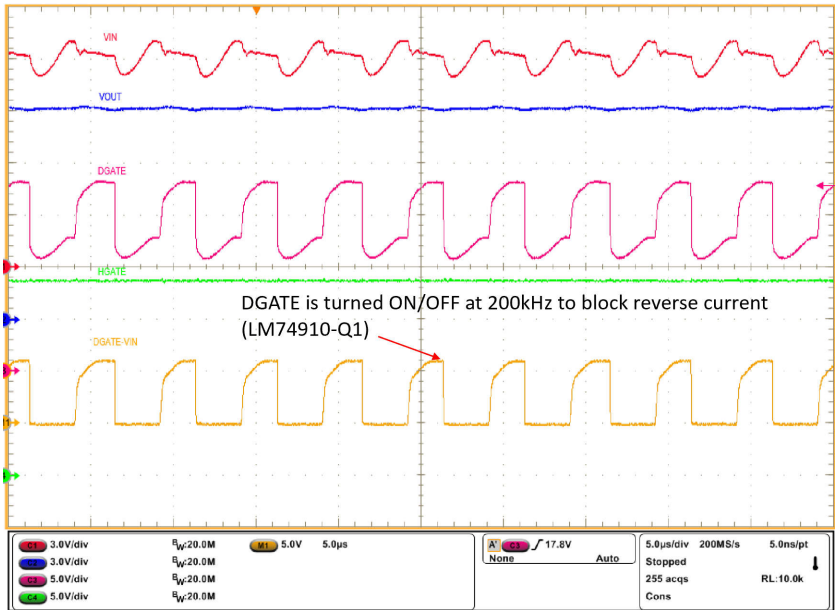


Figure 10-4. AC Super Imposed Test – 2-V Peak-Peak 200 kHz (LM74910-Q1)

10.2.2.3 Input Micro-Short Protection: LV124 E-10

E-10 test specified in LV124 standard checks for immunity of electronic modules to short interruptions in power supply input due to contact issues or relay bounce. During this test (case 2), micro-short is applied on the input for a duration as low as 10 µs to several ms. For a functional pass status A, electronic modules are required to run uninterrupted during the E-10 test (case 2) with 100-µs duration. Dual-Gate drive architecture of LM749x0-Q1, DGATE and HGATE, enables to achieve a functional pass status A with optimum hold up capacitance on the output when compared to a single gate drive controller. When input micro-short is applied for 100 µs, LM749x0-Q1 quickly turns off MOSFET Q1 by shorting DGATE to ANODE (source of MOSFET) within 0.5 µs to prevent the output from discharging and the HGATE remains ON keeping MOSFET Q2 ON, enabling fast recovery after the input short is removed.

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Performance of LM749x0-Q1 during E10 input power supply interruption test case 2 is shown in Figure 10-4. After the input short is removed, input voltage recovers and VAC voltage crosses forward turn on threshold (V_{AC_FWD}), MOSFET Q1 is turned back ON quickly. Note that dual-gate drive topology allows MOSFET Q2 to remain ON during the test and helps in restoring the input power faster. Output voltage remains unperturbed during the entire duration, achieving functional status A.

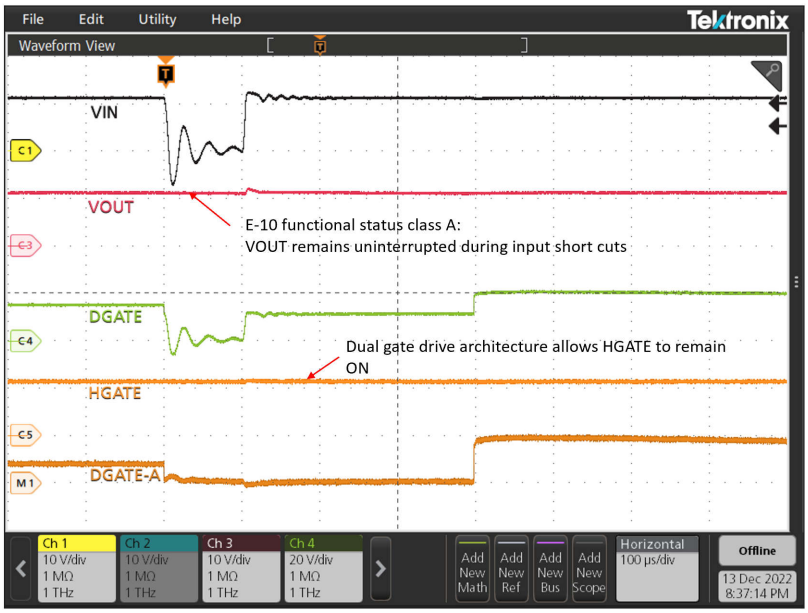


Figure 10-5. Input Micro-Short – LV124 E10 TC 2 100 µs

10.2.3 Detailed Design Procedure

10.2.3.1 Design Considerations

Table 10-1 summarizes the design parameters that must be known for designing an automotive reverse battery protection circuit with overvoltage cut-off. During power up, inrush current through MOSFET Q2 needs to be limited so that the MOSFET operates well within its SOA. Maximum load current, maximum ambient temperature and thermal properties of the PCB determine the R_{DSON} of the MOSFET Q2 and maximum operating voltage determines the voltage rating of the MOSFET Q2. Selection of MOSFET Q1 is determined mainly by the maximum operating load current, maximum ambient temperature, maximum frequency of AC super imposed voltage ripple and ISO 7637-2 pulse 1 requirements. overvoltage threshold is decided based on the rating of downstream DC/DC converter or other components after the reverse battery protection circuit. A single bi-directional TVS or two back-back uni-directional TVS are required to clamp input transients to a safe operating level for the MOSFETs Q1, Q2 and LM749x0-Q1.

10.2.3.2 Charge Pump Capacitance VCAP

Minimum required capacitance for charge pump VCAP is based on input capacitance of the MOSFET Q1, $C_{ISS(MOSFET_Q1)}$and input capacitance of Q2 $C_{ISS(MOSFET)}$.

Charge Pump VCAP: Minimum 0.1 µF is required; recommended value of VCAP (µF) ≥ 10 x ($C_{ISS(MOSFET_Q1)}$ + $C_{ISS(MOSFET_Q2)}$) (µF)

10.2.3.3 Input and Output Capacitance

A minimum input capacitance C_{IN} of 0.1 µF and output capacitance C_{OUT} of 0.1 µF is recommended.

10.2.3.4 Hold-Up Capacitance

Usually bulk capacitors are placed on the output due to various reasons such as uninterrupted operation during power interruption or micro-short at the input, hold-up requirements for doing a memory dump before turning of the module and filtering requirements as well. This design considers minimum bulk capacitors requirements for meeting functional status "A" during LV124 E10 test case 2 100-µs input interruption. To achieve functional pass status A, acceptable voltage droop in the output of LM74900-Q1 is based on the UVLO settings of downstream DC-DC converters. For this design, drop from 12 V to 6.5 V in output voltage for 100 µs is considered (assuming downstream converter with 5-V output) and the minimum hold-up capacitance required is calculated by

$$C_{HOLD_UP_MIN} = \frac{I_{LOAD} \times 100\ \mu s}{\Delta V_{OUT}} \tag{8}$$

Minimum hold-up capacitance required for 5.5-V drop in 100 µs is 100 µF. Note that the typical application circuit shows the hold-up capacitor as optional because not all designs require hold-up capacitance.

10.2.3.5 Selection of Current Sense Resistor, R_{SNS}

LM749x0-Q1 has integrated short circuit detection comparator with default sense threshold of 20 mV. For this application, short circuit limit is set to 20 A. The sense resistor value based on short circuit comparator can be calculated by Equation 9.

$$R_{SENSE} = \frac{V_{SENSE}}{I_{SCP}} \tag{9}$$

Select a 1-mΩ resistor with 1% tolerance to set short circuit protection limit of 20 A.

10.2.3.6 Selection of Scaling Resistor (R_{SET}) and Short-Circuit Protection Setting Resistor (R_{SCP})

R_{SET} is the resistor connected between VS and CS+ pins. This resistor scales the overcurrent protection threshold voltage and coordinates with R_{ILIM} and R_{IMON} to determine the overcurrent protection threshold and current monitoring output. The recommended range of RSET is 50 Ω to 100 Ω. RSET is selected as 50 Ω, 1% for this design example.

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LM749x0-Q1 default short circuit threshold of 20 mV can be shifted to higher value as given by Equation 10.

$$V_{SNS_SCP} = (10.5\ \mu A \times R_{ISCP}) + 20\ mV \quad (10)$$

For this application, ISCP pin is shorted directly to common drain point. User has a flexibility to populate suitable value of RSCP resistor to adjust short circuit protection current limit and also gives flexibility in terms of selecting different current sense resistor value.

An additional de-glitch filter (optional) consisting of R_{SCP} and C_{SCP} can be added from ISCP pin to CS– pin as shown in Figure 10-1 to avoid any false short circuit trigger in case of fast automotive transients such as Input Micro cuts (LV124, E-10), AC superimpose (LV124, E-06), ISO7637-2 Pulse 2 A.

10.2.3.7 Overcurrent Limit (ILIM), Circuit Breaker Timer (TMR), and Current Monitoring Output (IMON) Selection

Programming the Overcurrent Protection Threshold – R_{ILIM} Selection

The R_{ILIM} sets the overcurrent protection (circuit breaker detection) threshold, whose value can be calculated using Equation 11.

$$R_{(ILIM)} = \frac{12 \times R_{SET}}{R_{SENSE} \times I_{LIM}} \quad (11)$$

To set 10 A as overcurrent protection threshold, R_{ILIM} value is calculated to be 60 kΩ. Choose the closest available standard value: 60 kΩ, 1%.

Programming the Circuit Breaker Time – C_{TMR} Selection

For the design example under discussion, overcurrent transients are allowed for 1-ms duration. This blanking interval, T_{OC} (or circuit breaker interval, T_{CB}) can be set by selecting appropriate capacitor C_{TMR} from TMR pin to ground. The value of CTMR to set 1 ms for TOC can be calculated using Equation 12.

$$T_{(OC)} = 1.2 \times \frac{C_{TMR}}{82.3\ \mu A} \quad (12)$$

Choose closest available standard value: 68 nF, 10%.

Programming Current Monitoring Output – R_{IMON} Selection

Voltage at IMON pin V_{IMON} is proportional to the output load current. This can be connected to an ADC of the downstream system for monitoring the operating condition and health of the system. The R_{IMON} must be selected based on the maximum load current and the input voltage range of the ADC used. R_{IMON} is set using Equation 13.

$$V_{IMON} = \frac{0.9 \times V_{SENSE} \times R_{IMON}}{R_{SET}} \quad (13)$$

For this application example, VIMON is selected to be 2.7 V at full load current of 5 A. RIMON value of 30.1 kΩ, 1% is selected.

10.2.3.8 Overvoltage Protection and Battery Monitor

Resistors R_1, R_2 and R_3, R_4 connected from SW pin to ground is used to program the undervoltage and overvoltage threshold. The resistor values required for setting the undervoltage threshold (V_{UVLO} to 5.5 V) and overvoltage threshold (V_{OV} to 37.0 V) a are calculated by solving

$$V_{UVLOF} = \frac{R_2 \times V_{UVSET}}{(R_1 + R_2)} \quad (14)$$

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$$V_{OVR} = \frac{R_4 \times V_{OVSET}}{(R_3 + R_4)} \quad (15)$$

For minimizing the input current drawn from the battery through resistors R_1, R_2, and R_3; it is recommended to use higher value of resistance. Using high value resistors will add error in the calculations because the current through the resistors at higher value will become comparable to the leakage current into the OV pin. Maximum leakage current into the OV pin is 1 µA and choosing total ladder resistor < 120 kΩ ensures current through resistors is 100 times greater than leakage through OV pin.

Based on the device electrical characteristics, V_{UVLOF} is 0.55 V. Select R_1 = 100 kΩ. Solving Equation 14 gives R_2 = 11.5 kΩ. Solving Equation 15 with R3 selected as 100 kΩ and V_{OVR} = 0.6 V gives R_4 = 1.65 kΩ as standard 1% resistor values closest to the calculated resistor values.

An optional capacitor C_{UV} can be placed in parallel with R2 on UVLO resistor ladder in order to filter out any fast undervoltage transients on battery lines to avoid false UVLO trigger.

For this application example separate resistor ladder is selected to program overvoltage and undervoltage threshold. However common resistor ladder from SW pin to ground can also be used as shown in Figure 9-9.

10.2.4 MOSFET Selection: Blocking MOSFET Q1

For selecting the blocking MOSFET Q1, important electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, the maximum source current through body diode and the drain-to-source ON resistance R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current.

The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include all the automotive transient events and any anticipated fault conditions. It is recommended to use MOSFETs with V_{DS} voltage rating of 60 V along with a single bidirectional TVS or a V_{DS} rating 40-V maximum rating along with two unidirectional TVS connected back-back at the input.

The maximum V_{GS} LM74900-Q1 can drive is 14 V, so a MOSFET with 15-V minimum V_{GS} rating should be selected. If a MOSFET with < 15-V V_{GS} rating is selected, a zener diode can be used to clamp V_{GS} to safe level, but this would result in increased IQ current.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred, but selecting a MOSFET based on low $R_{DS(ON)}$ may not be beneficial always. Higher $R_{DS(ON)}$ will provide increased voltage information to LM74900-Q1's reverse comparator at a lower reverse current. Reverse current detection is better with increased $R_{DS(ON)}$. Choosing a MOSFET with < 50-mV forward voltage drop at maximum current is a good starting point.

For active rectification of AC super imposed ripple on the battery supply voltage, gate-source charge Q_{GS} of Q1 must be selected to meet the required AC ripple frequency. Maximum gate-source charge Q_{GS} (at 4.5-V V_{GS}) for active rectification every cycle is

$$Q_{GS_MAX} = \frac{1.3mA}{F_{AC_RIPPLE}} \quad (16)$$

Where 1.3 mA is minimum charge pump current at 7-V V_{DGATE}-V_A, F_{AC_RIPPLE} is frequency of the AC ripple superimposed on the battery and Q_{GS_MAX} is the Q_{GS} value specified in manufacturer datasheet at 6-V V_{GS}. For active rectification at F_{AC_RIPPLE} = 30 KHz, Q_{GS_MAX} = 43 nC.

Based on the design requirements, BUK7Y4R8-60E MOSFET is selected and its ratings are:

- 60-V $V_{DS(MAX)}$ and ±20-V $V_{GS(MAX)}$
- $R_{DS(ON)}$ 5.0-mΩ typical at 5-V V_{GS} and 2.9-mΩ rated at 10-V V_{GS}
- MOSFET Q_{GS} 17.4 nC

Thermal resistance of the MOSFET should be considered against the expected maximum power dissipation in the MOSFET to ensure that the junction temperature (T_J) is well controlled.

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10.2.5 MOSFET Selection: Hot-Swap MOSFET Q2

The V_{DS} rating of the MOSFET Q2 should be sufficient to handle the maximum system voltage along with the input transient voltage. For this 12-V design, transient overvoltage events are during suppressed load dump 35 V 400 ms and ISO 7637-2 pulse 2 A 50 V for 50 µs. Further, ISO 7637-2 Pulse 3B is a very fast repetitive pulse of 100 V 100 ns that is usually absorbed by the input and output ceramic capacitors and the maximum voltage on the 12-V battery can be limited to < 40 V the minimum recommended input capacitance of 0.1 µF. The 50-V ISO 7637-2 Pulse 2 A can also be absorbed by input and output capacitors and its amplitude could be reduced to 40-V peak by placing sufficient amount of capacitance at input and output. However for this 12-V design, maximum system voltage is 50 V and a 60-V V_{DS} rated MOSFET is selected.

The VGS rating of the MOSFET Q2 should be higher than that maximum HGATE-OUT voltage 15 V.

Inrush current through the MOSFET during input hot-plug into the 12-V battery is determined by output capacitance. External capacitor on HGATE, C_{DVDT} is used to limit the inrush current during input hot-plug or start-up. The value of inrush current determined by Equation 2 need to be selected to ensure that the MOSFET Q2 is operating well within its safe operating area (SOA). To limit inrush current to 0.5 A, C_{DVDT} value of 10.0 nF is chosen.

Duration of inrush current is calculated by Equation 17.

$$T_{INRUSH} = \frac{V_{IN} \times C_{OUT}}{I_{INRUSH}} \quad (17)$$

Calculated inrush current duration is 2.5 ms with 0.5-A inrush current.

MOSFET BUK7Y4R8-60E having 60-V V_{DS} and ±20-V V_{GS} rating is selected for Q2. Power dissipation during inrush is well within the MOSFET's safe operating area (SOA).

10.2.6 TVS Selection

A 600-W SMBJ TVS such as SMBJ33CA is recommended for input transient clamping and protection. For detailed explanation on TVS selection for 12-V battery systems, refer to *TVS Selection for 12-V Battery Systems*.

10.2.7 Application Curves

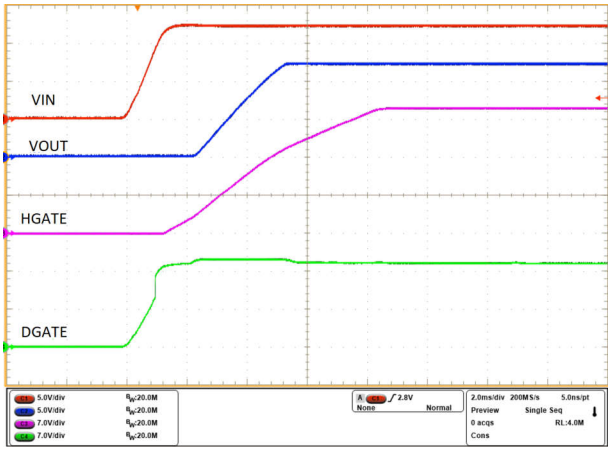


Figure 10-6. Start-Up 12 V With EN Pulled to VS

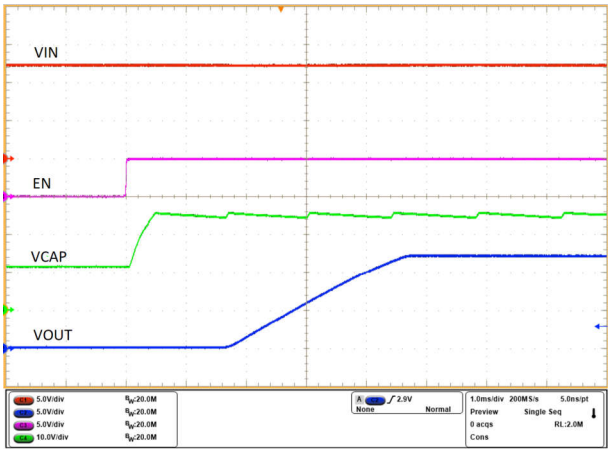


Figure 10-7. Start-Up 12 V With EN Going Low to High

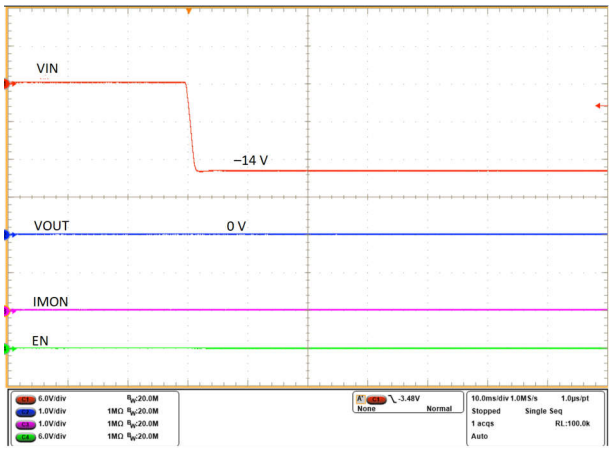


Figure 10-8. Reverse Input Voltage –14 V

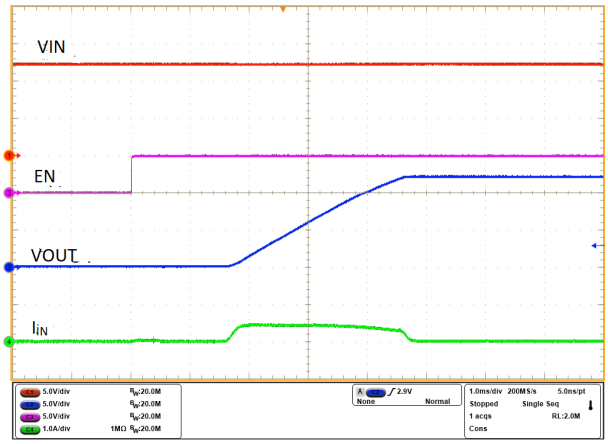


Figure 10-9. Inrush Current With No Load at Output

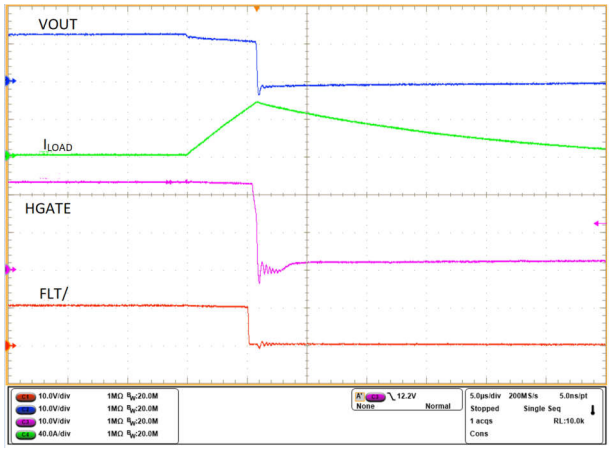


Figure 10-10. Output Short Circuit Protection (On-The-Fly)

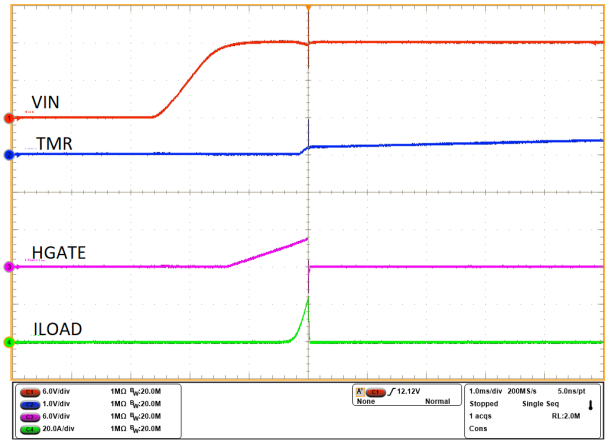


Figure 10-11. Device Start-Up With Output Short Circuit (TIMER Duration 1 ms)

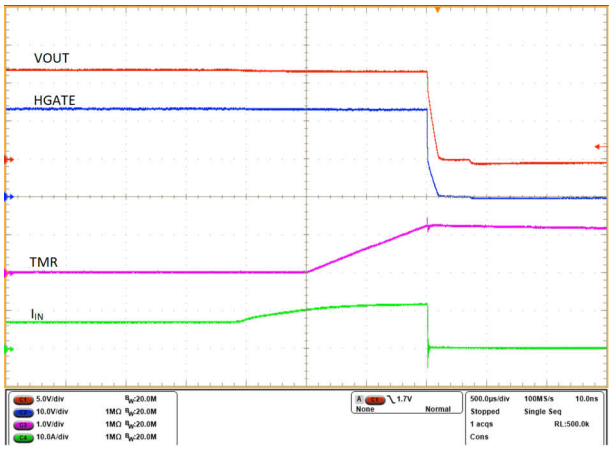


Figure 10-12. Output Overcurrent Protection (TIMER Duration 1 ms)

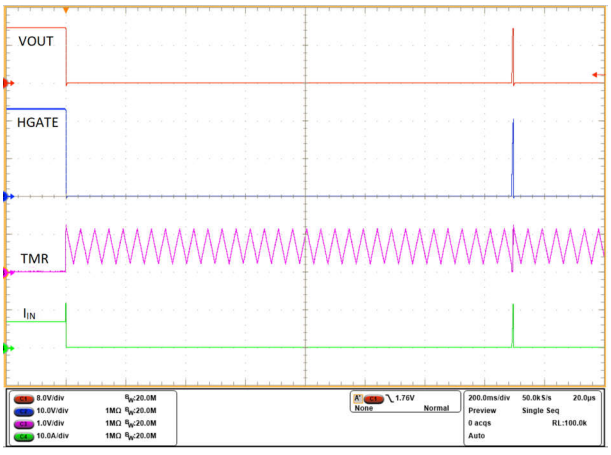


Figure 10-13. Output Overcurrent Protection (TIMER Duration 1 ms): Auto Retry

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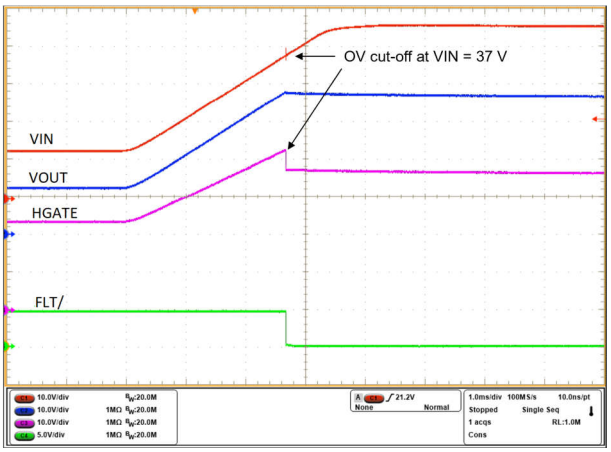


Figure 10-14. Overvoltage Protection

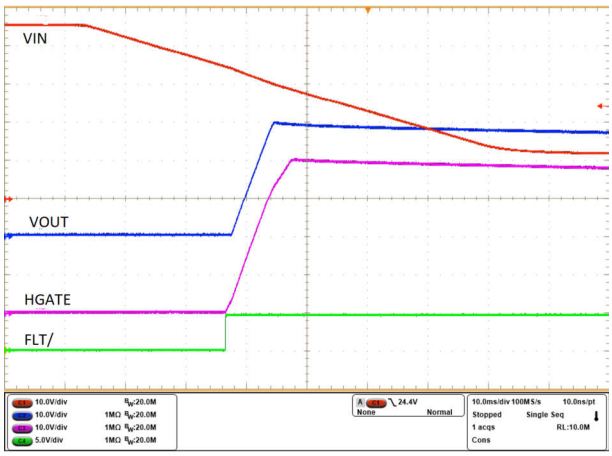


Figure 10-15. Overvoltage Recovery

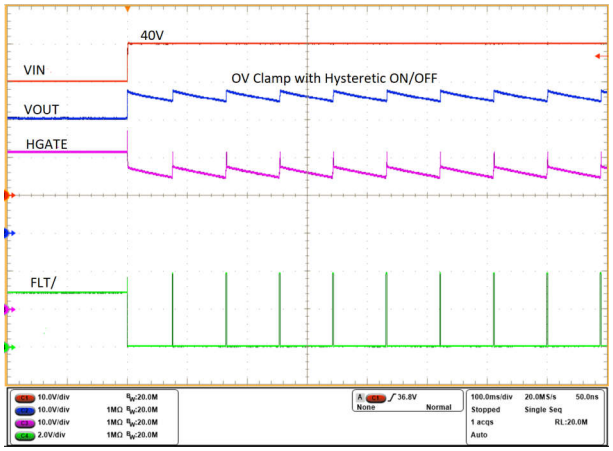


Figure 10-16. Overvoltage Clamp Response (OV Resistor Ladder Referred to VOUT)

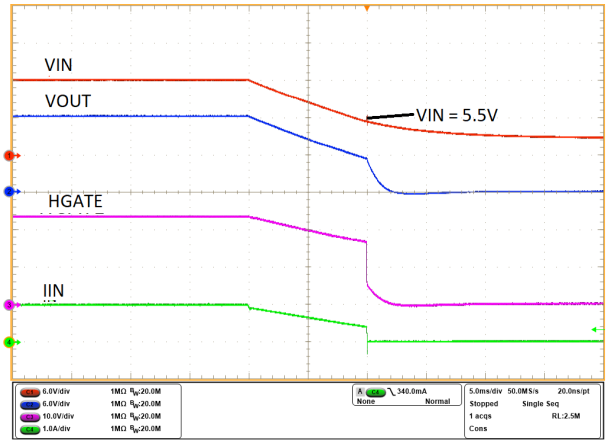


Figure 10-17. Undervoltage Lockout (UVLO) Protection (V_{IN_UVLO} = 5.5 V)

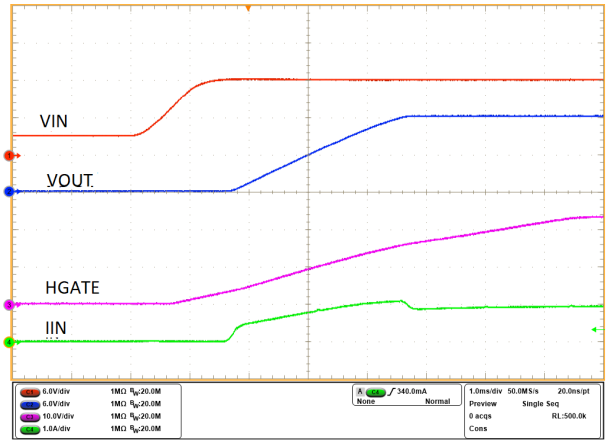


Figure 10-18. Undervoltage Lockout (UVLO) Recovery

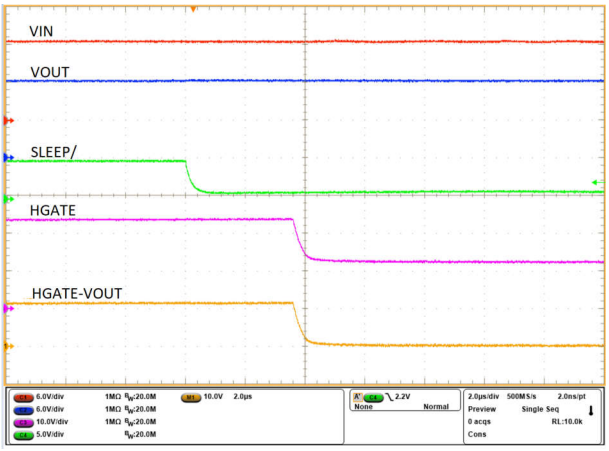


Figure 10-19. SLEEP Mode Entry ($\overline{SLEEP}$ = Low, EN = High)

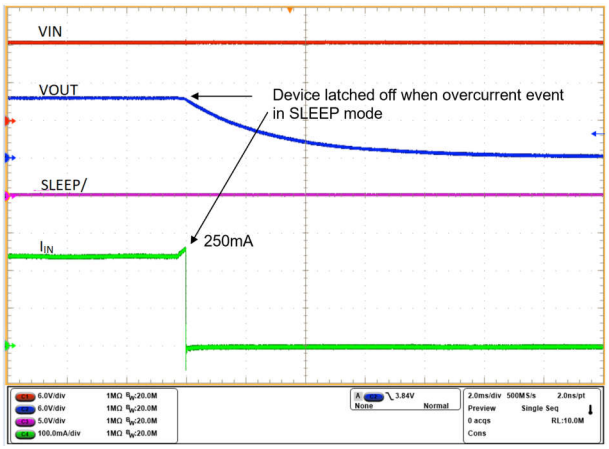


Figure 10-20. SLEEP Mode Overcurrent Protection (250 mA Typical)

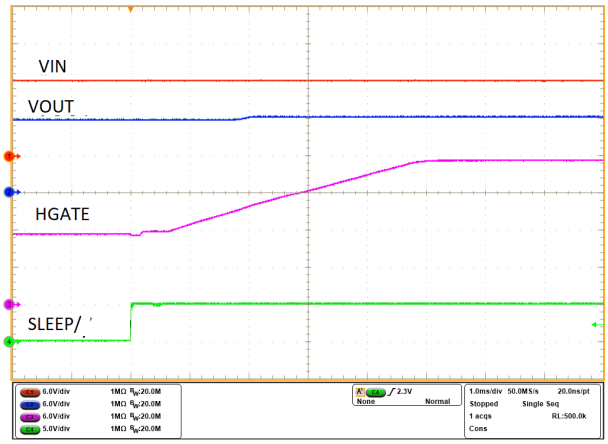


Figure 10-21. SLEEP Mode Exit ($\overline{\text{SLEEP}}$ = High, EN = High)

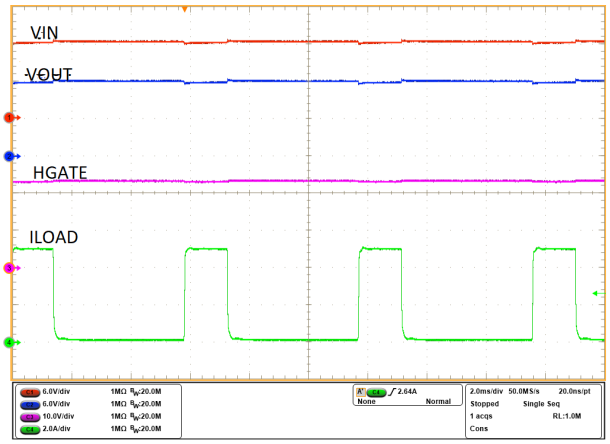


Figure 10-22. Load Transient 100 mA to 5 A

10.3 Addressing Automotive Input Reverse Battery Protection Topologies With LM749x0-Q1

The LM749x0-Q1 dual gate drive architecture can address various MOSFET control topologies such as ideal diode FET only, high-side switch controller only, dual OR-ing with load disconnect, and priority power muxing. This enables system designers to use LM749x0-Q1 as a plug and place component to meet various automotive front end protection solutions with a common controller. For additional details on overview of different automotive reverse battery protection topologies that can be addressed using LM749x0-Q1, refer to Addressing Automotive Reverse Battery Protection Toplogies using LM749x0-Q1.

10.4 Power Supply Recommendations

10.4.1 Transient Protection

When the external MOSFETs turn OFF during the conditions such as overvoltage cut-off, reverse current blocking, overcurrent cut-off, EN causing an interruption of the current flow, the input line inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device.
- Using large PCB GND plane.
- Use of a Schottky diode across the output and GND to absorb negative spikes.

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- A low value ceramic capacitor ($C_{(IN)}$ to approximately 0.1 µF) to absorb the energy and dampen the transients.

The approximate value of input capacitance can be estimated with Equation 8.

$$V_{spike(Absolute)} = V_{(IN)} + I_{(Load)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (18)$$

where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Some applications may require additional Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device. These transients can occur during EMC testing such as automotive ISO7637 pulses.

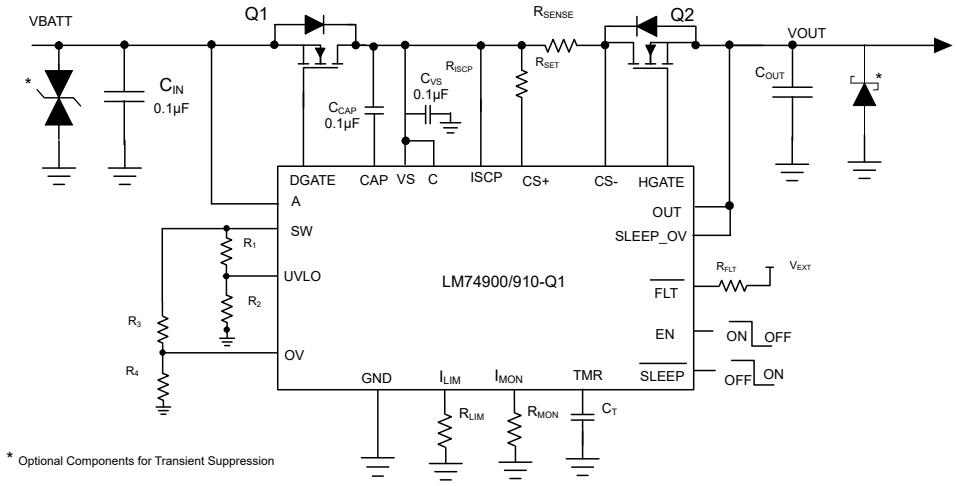


Figure 10-23. Typical Application Diagram

10.4.2 TVS Selection for 12-V Battery Systems

In selecting the TVS, important specifications are breakdown voltage and clamping voltage. The breakdown voltage of the TVS for positive transients must be higher than 24-V jump start voltage and 35-V suppressed load dump voltage and less than the maximum ratings of LM749x0-Q1 (65 V). The breakdown voltage of TVS for negative transients must be beyond than maximum reverse battery voltage –16 V, so that the TVS– is not damaged due to long time exposure to reverse connected battery.

Clamping voltage is the voltage the TVS diode clamps in high current pulse situations and this voltage is much higher than the breakdown voltage. In the case of an ISO 7637-2 pulse 1, the input voltage goes up to –150 V with a generator impedance of 10 Ω. This action translates to 15 A flowing through the TVS–, and the voltage across the TVS is close to its clamping voltage.

The next criterion is that the absolute maximum rating of cathode to anode voltage of the LM749x0-Q1 (85 V) and the maximum VDS rating MOSFET are not exceeded. In the design example, 60-V rated MOSFET is chosen and maximum limit on the cathode to anode voltage is 60 V.

During ISO 7637-2 pulse 1, the anode of LM749x0-Q1 is pulled down by the ISO pulse, clamped by TVS– and the MOSFET Q1 is turned off quickly to prevent reverse current from discharging the bulk output capacitors. When the MOSFET turns off, the cathode to anode voltage seen is equal to (TVS Clamping voltage + Output capacitor voltage). If the maximum voltage on output capacitor is 16 V (maximum battery voltage), then the clamping voltage of the TVS– must not exceed, (60 V – 16) V = –44 V.

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The SMBJ33CA TVS diode can be used for 12-V battery protection application. The breakdown voltage of 36.7 V meets the jump start, load dump requirements on the positive side and 16-V reverse battery connection on the negative side. During ISO 7637-2 pulse 1 test, the SMBJ33CA clamps at –44 V with 12 A of peak surge current as shown in and it meets the clamping voltage ≤ 44 V. SMBJ series of TVS' are rated up to 600-W peak pulse power levels and are sufficient for ISO 7637-2 pulses.

10.5 Layout

10.5.1 Layout Guidelines

- For the ideal diode stage, connect A, DGATE, and C pins of LM749x0-Q1 close to the MOSFET SOURCE, GATE and, DRAIN pins.
- For the load disconnect stage, connect HGATE and OUT pins of LM749x0-Q1 close to the MOSFET GATE and SOURCE pins.
- The high current path of for this solution is through the MOSFET, therefore it is important to use thick and short traces for source and drain of the MOSFET to minimize resistive losses.
- Follow kelvin connection for connecting CS+ and CS- pin to external current sense resistor.
- The DGATE pin of the LM749x0-Q1 must be connected to the MOSFET GATE with short trace.
- Place transient suppression components close to LM749x0-Q1.
- Place the decoupling capacitor, C_{VS} close to VS pin and chip GND.
- The charge pump capacitor across CAP and VS pins must be kept away from the MOSFET to lower the thermal effects on the capacitance value.

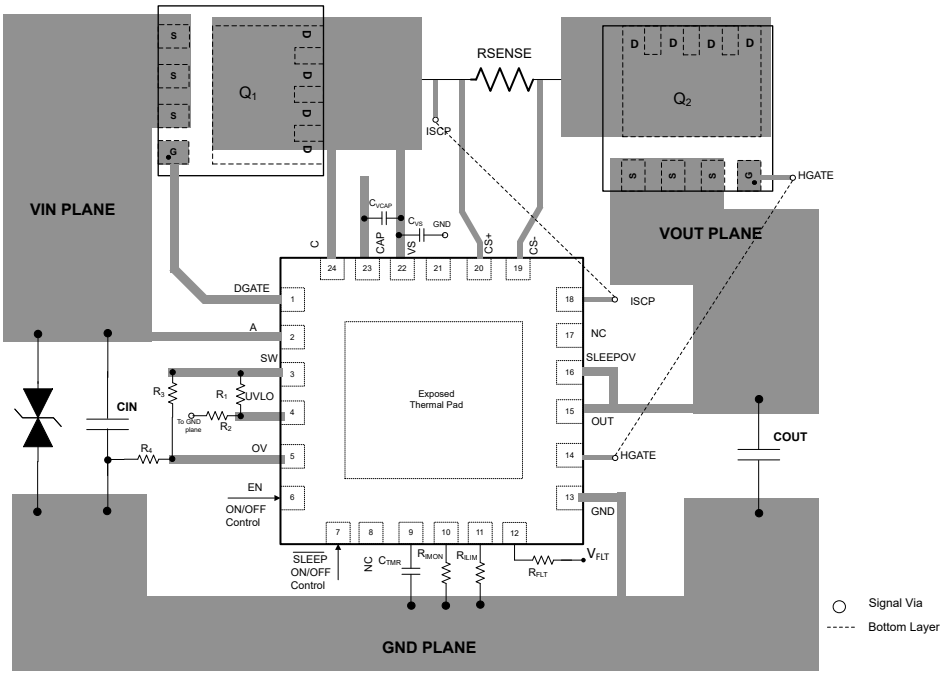


Figure 10-24. Example Layout

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11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM74900QRGERQ1	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM 74900Q	Samples
LM74910QRGERQ1	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM 74910Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

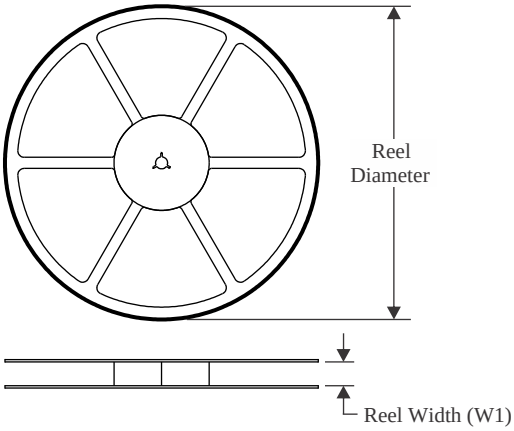
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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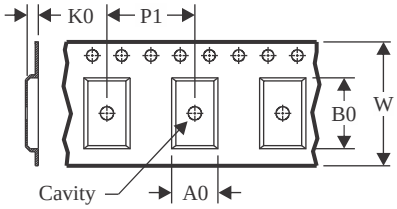
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

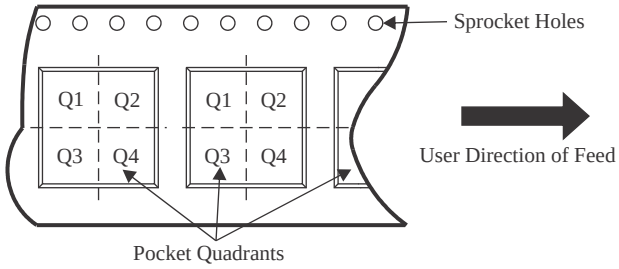


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

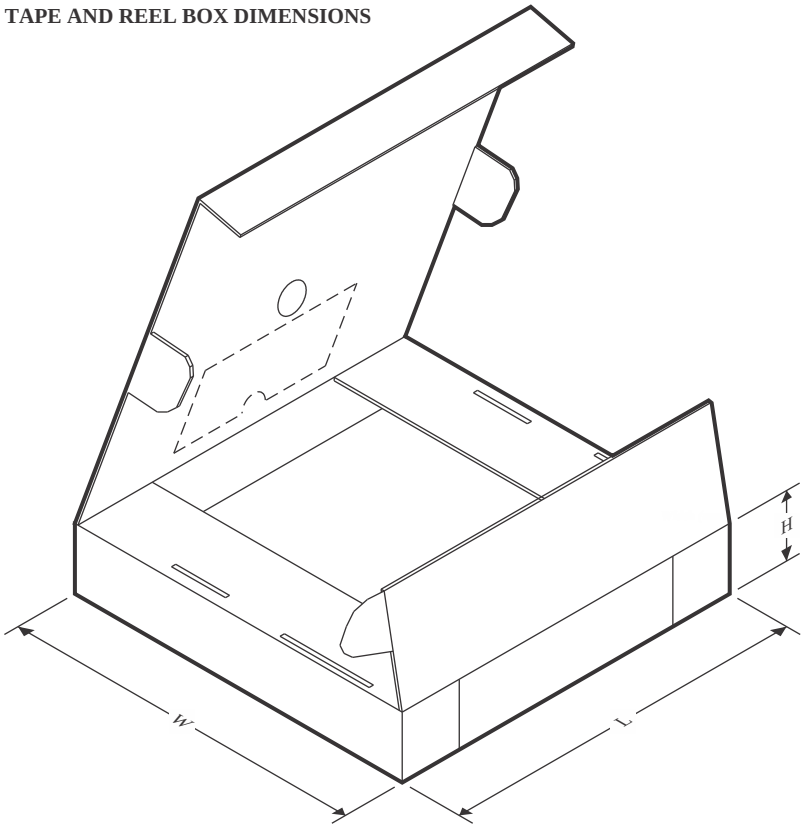
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM74900QRGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
LM74910QRGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



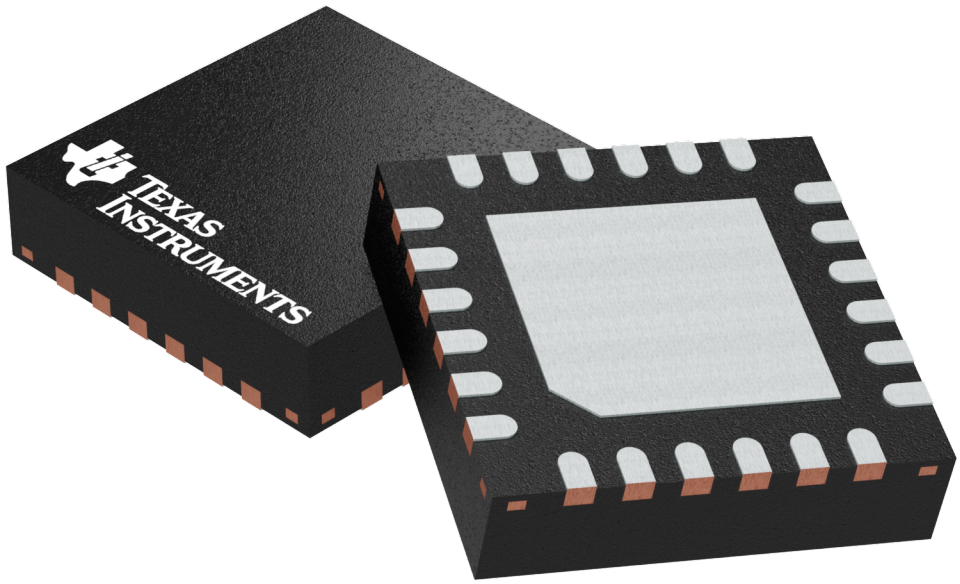
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM74900QRGERQ1	VQFN	RGE	24	3000	367.0	367.0	35.0
LM74910QRGERQ1	VQFN	RGE	24	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

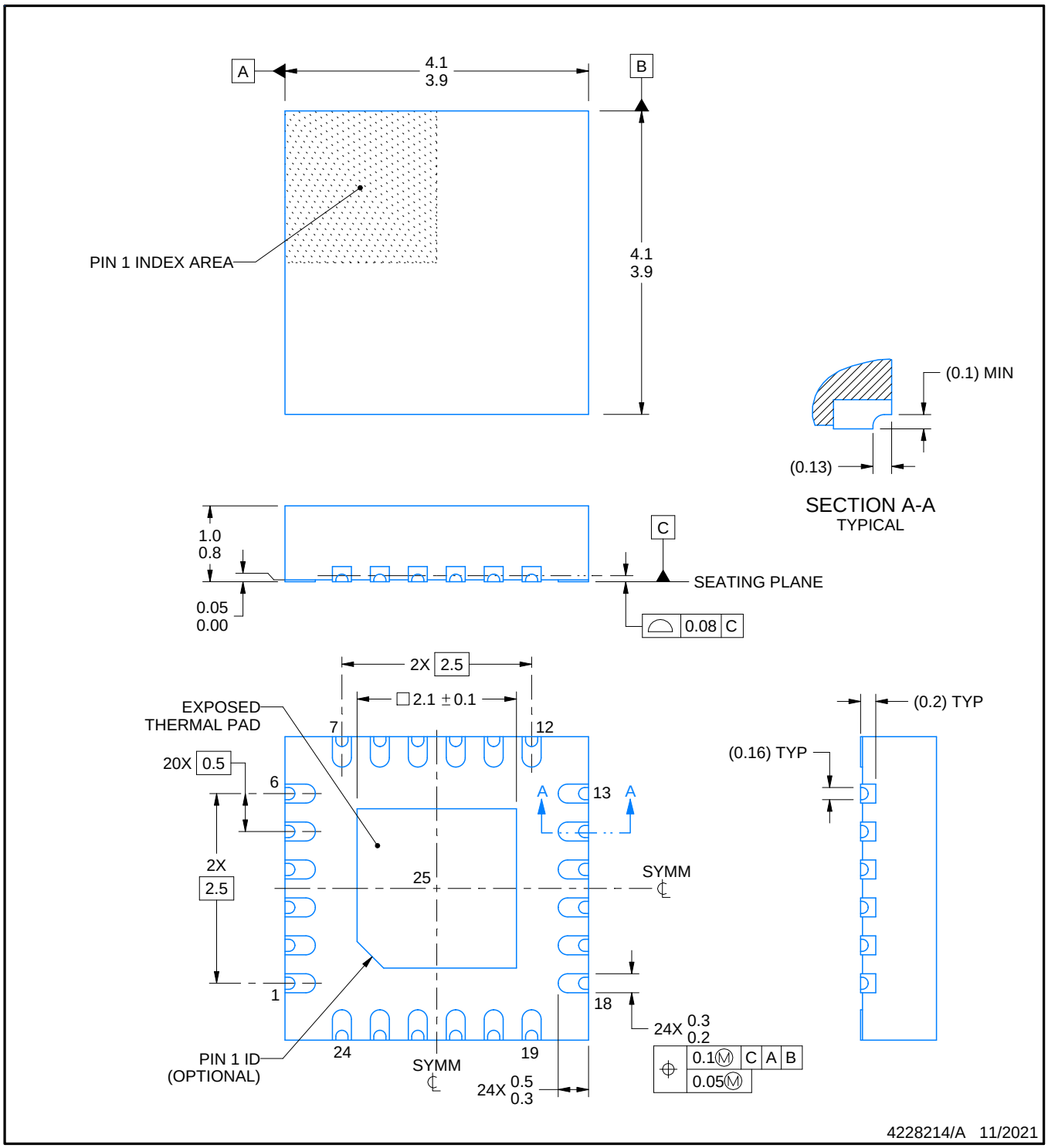
4204104/H

RGE0024T

PACKAGE OUTLINE

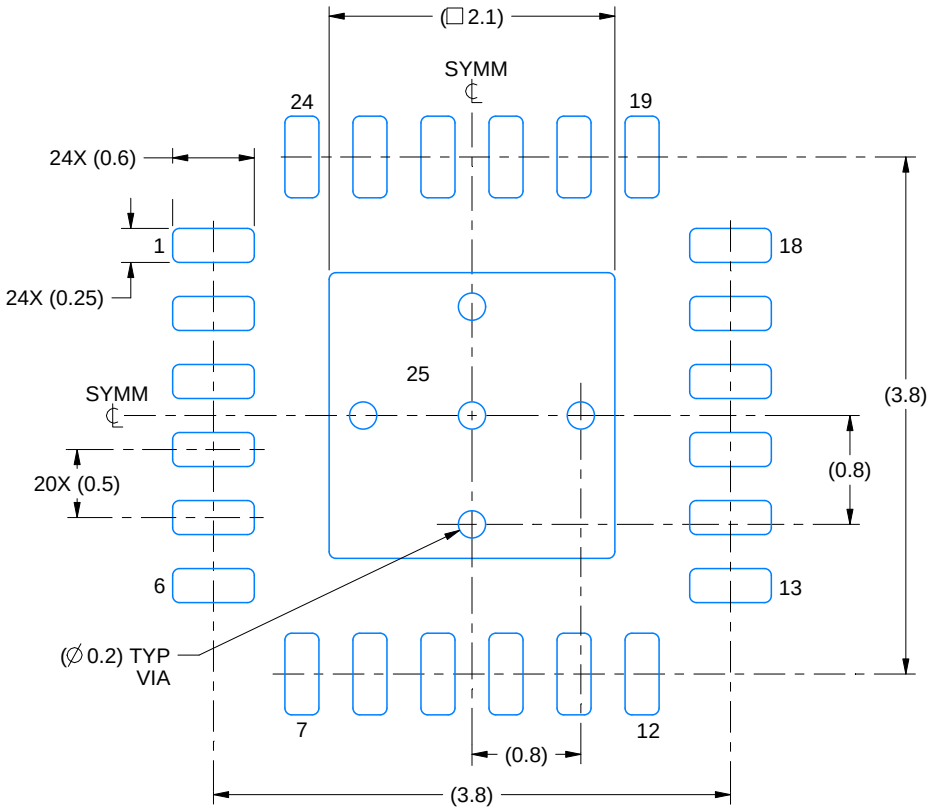
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

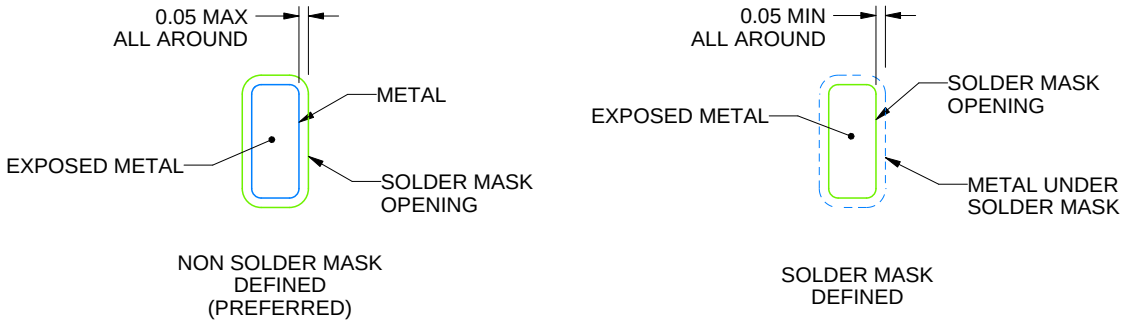


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

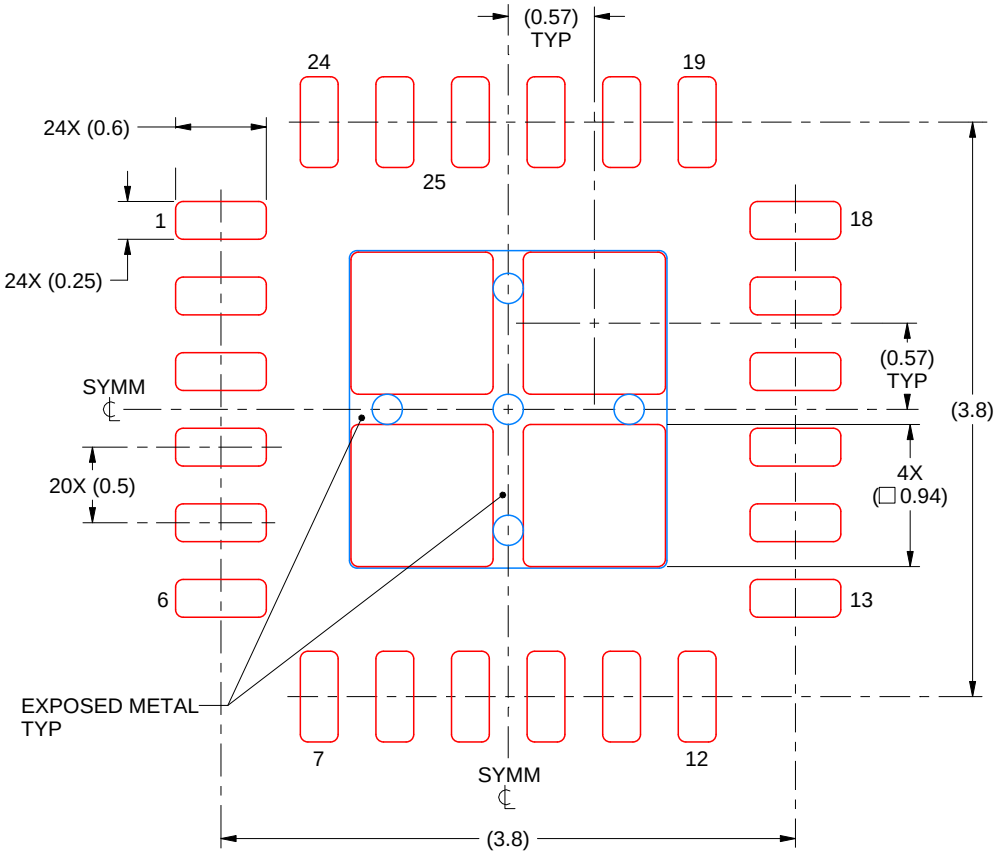


SOLDER MASK DETAILS

4228214/A 11/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

THERMAL PAD 25:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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