SN74AC244-Q1 Automotive Octal Buffers or Drivers With 3-State Outputs

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Available in wettable flank QFN (RKS) package
- Wide operating range of 1.5V to 6V
- Inputs accept voltages up to 6V
- Continuous ±24mA output drive at 5V
- Supports up to ±75mA output drive at 5V in short bursts
- Drives 50Ω transmission lines
- Maximum t_{pd} of 6.8ns at 5V

2 Applications

- Enable or disable a digital signal
- Eliminate slow or noisy input signals
- Hold a signal during controller reset
- Debounce a switch

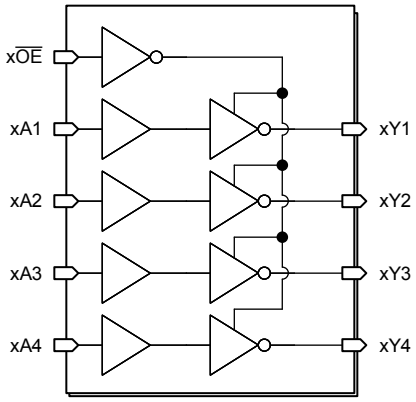
3 Description

The SN74AC244-Q1 is an octal buffer with 3-state outputs and Schmitt-trigger inputs. The device is configured into two banks of four drivers, each controlled by an output enable pin.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74AC244-Q1	DGS (VSSOP, 20)	5.1mm × 4.9mm	5.1mm × 3mm
	RKS (VQFN, 20)	4.5mm × 2.5mm	4.5mm × 2.5mm
	PW (TSSOP, 20)	6.5mm × 6.4mm	6.5mm × 4.4mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

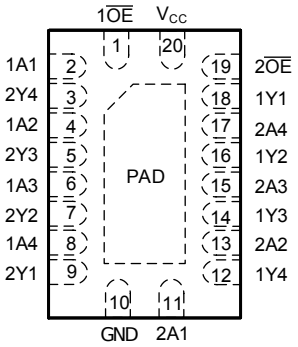


Figure 4-1. RKS Package, 20-Pin VQFN (Top View)

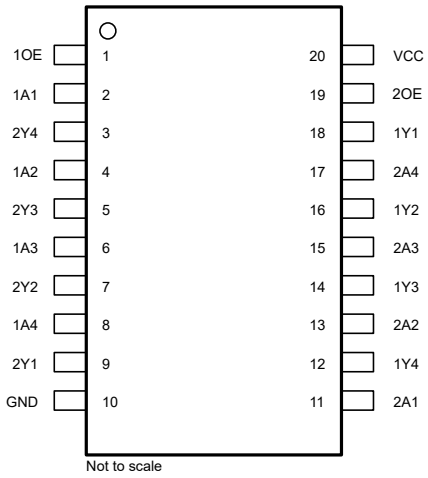


Figure 4-2. DGS or PW Package, 20-Pin VSSOP or TSSOP (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1$\overline{OE}$	1	I	Bank 1, output enable, active low
1A1	2	I	Bank 1, channel 1 input
2Y4	3	O	Bank 2, channel 4 output
1A2	4	I	Bank 1, channel 2 input
2Y3	5	O	Bank 2, channel 3 output
1A3	6	I	Bank 1, channel 3 input
2Y2	7	O	Bank 2, channel 2 output
1A4	8	I	Bank 1, channel 4 input
2Y1	9	O	Bank 2, channel 1 output
GND	10	G	Ground
2A1	11	I	Bank 2, channel 1 input
1Y4	12	O	Bank 1, channel 4 output
2A2	13	I	Bank 2, channel 2 input
1Y3	14	O	Bank 1, channel 3 output
2A3	15	I	Bank 2, channel 3 input
1Y2	16	O	Bank 1, channel 2 output
2A4	17	I	Bank 2, channel 4 input
1Y1	18	O	Bank 1, channel 1 output
2$\overline{OE}$	19	I	Bank 2, output enable, active low
V_{CC}	20	P	Positive supply
Thermal pad[2]		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply

(1) I = input, O = output, I/O = input or output, G = ground, P = power.
(2) RKS package only.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
V_I	Input voltage range(2)		-0.5	V_{CC} + 0.5 V	V
V_O	Output voltage range(2)		-0.5	V_{CC} + 0.5 V	V
I_{IK}	Input clamp current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V		±20	mA
I_{OK}	Output clamp current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V		±50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±50	mA
	Continuous output current through V_{CC} or GND			±200	mA
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.5	6	V
V_{IH}	High-level input voltage	V_{CC} = 1.5 V	1.2		V
		V_{CC} = 1.8 V	1.26		
		V_{CC} = 2.5 V	1.75		
		V_{CC} = 3 V	2.1		
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-Level input voltage	V_{CC} = 1.5 V		0.3	V
		V_{CC} = 1.8 V		0.54	
		V_{CC} = 2.5 V		0.75	
		V_{CC} = 3 V		0.9	
		V_{CC} = 4.5 V		1.35	
		V_{CC} = 5.5 V		1.65	
V_I	Input Voltage		0	V_{CC}	V
V_O	Output Voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.8 V		-1	mA
I_{OH}	High-level output current	V_{CC} = 2.5 V		-2	mA
I_{OH}	High-level output current	V_{CC} = 3 V		-12	mA
		V_{CC} = 4.5 V to 5.5 V		-24	
I_{OL}	Low-level output current	V_{CC} = 1.8 V		1	mA
I_{OL}	Low-level output current	V_{CC} = 2.5 V		2	mA
I_{OL}	Low-level output current	V_{CC} = 3 V		12	mA
		V_{CC} = 4.5 V to 5.5 V		24	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.5 V to 3 V		50	ns/V
		V_{CC} = 3.6 V to 5.5 V		20	
T_A	Operating free-air temperature		-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report: Implications of Slow or Floating CMOS Inputs.

5.4 Thermal Information

THERMAL METRIC(1)		SN74AC244-Q1			UNIT
		DGS (VSSOP)	PW (TSSOP)	RKS (VQFN)	
		20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	123.5	126.2	67.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.1	68.7	72.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.5	77.3	40.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.8	22.3	10.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	78.0	76.9	40.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	24.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = -50 uA	1.5 V	1.4			1.4			V
		1.8 V	1.7	1.79		1.7			
		2.5 V	2.4	2.49		2.4			
		3 V	2.9	2.99		2.9			
		4.5 V	4.4	4.49		4.4			
		5.5 V	5.4	5.49		5.4			
	I_{OH} = -1 mA	1.8 V	1.53			1.44			
	I_{OH} = -2mA	2.5 V	2.13			2			
	I_{OH} = -4 mA	3 V	2.58			2.4			
	I_{OH} = -12 mA	3 V	2.58			2.4			
	I_{OH} = -24 mA	4.5 V	3.94			3.7			
	I_{OH} = -24 mA	5.5 V	4.94			4.7			
	I_{OH} = -75 mA(1)	5.5 V	3.85						
	I_{OH} = -50 mA(1)	5.5 V				3.85			
V_{OL}	I_{OL} = 50 uA	1.5 V			0.1			0.1	V
		1.8 V			0.1			0.1	
		2.5 V			0.1			0.1	
		3 V		0.002	0.1			0.1	
		4.5 V		0.001	0.1			0.1	
		5.5 V		0.001	0.1			0.1	
	I_{OL} = 1 mA	1.8 V			0.2			0.36	
	I_{OL} = 2 mA	2.5 V			0.36			0.5	
	I_{OL} = 4 mA	3 V			0.36			0.5	
	I_{OL} = 12 mA	3 V			0.36			0.5	
	I_{OL} = 24 mA	4.5 V			0.36			0.5	
	I_{OL} = 24 mA	5.5 V			0.36			0.5	
	I_{OL} = 75 mA(1)	5.5 V			1.65				
	I_{OL} = 50 mA(1)	5.5 V						1.65	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1			±1	µA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.25			±5	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2			20	µA
C_I	V_I = V_{CC} or GND	5 V		2.5	5.1		3	5.3	pF
C_{PD} (2) (3)	C_L = 50 pF, F = 1Mhz	5 V		45			45		pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms
(2) C_{PD} is used to determine the dynamic power consumption, per channel
(3) $P_D = V_{CC}^2 \times F_I \times (C_{PD} + C_L)$ where F_I= input frequency, C_L= output load capacitance, V_{CC}= supply voltage

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5.6 Switching Characteristics 1.5-V V_{CC}

C_L = 50 pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).
See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	Y	1	18.3	62	1		85	ns
t_{PHL}	A	Y	1	18.3	62	1		85	ns
t_{PZH}	$\overline{OE}$	Y	1	24	71	1		150	ns
t_{PZL}	$\overline{OE}$	Y	1	24	71	1		150	ns
t_{PHZ}	$\overline{OE}$	Y	1	25.4	71	1		150	ns
t_{PLZ}	$\overline{OE}$	Y	1	25.4	71	1		150	ns

5.7 Switching Characteristics 1.8-V V_{CC}

C_L = 50 pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).
See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	Y	1	12.0	28	1		41.2	ns
t_{PHL}	A	Y	1	12.0	28	1		41.2	ns
t_{PZH}	$\overline{OE}$	Y	1	15.3	36	1		54.5	ns
t_{PZL}	$\overline{OE}$	Y	1	15.3	36	1		54.5	ns
t_{PHZ}	$\overline{OE}$	Y	1	13.6	37	1		44.8	ns
t_{PLZ}	$\overline{OE}$	Y	1	13.6	37	1		44.8	ns

5.8 Switching Characteristics 2.5-V V_{CC}

C_L = 50 pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).
See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	Y	1	7.5	16	1		20.8	ns
t_{PHL}	A	Y	1	7.5	16	1		20.8	ns
t_{PZH}	$\overline{OE}$	Y	1	9.6	22	1		27.4	ns
t_{PZL}	$\overline{OE}$	Y	1	9.6	22	1		27.4	ns
t_{PHZ}	$\overline{OE}$	Y	1	7.3	16	1		20.7	ns
t_{PLZ}	$\overline{OE}$	Y	1	7.3	16	1		20.7	ns

5.9 Switching Characteristics 3.3-V V_{CC}

C_L = 50 pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).
See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	Y	1	6	8	1		9.5	ns
t_{PHL}	A	Y	1	5.5	8	1		9.5	ns
t_{PZH}	$\overline{OE}$	Y	1	6	10.5	1		11.5	ns
t_{PZL}	$\overline{OE}$	Y	1	7	10	1		13	ns
t_{PHZ}	$\overline{OE}$	Y	1	7	10	1		12.5	ns

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5.9 Switching Characteristics 3.3-V V_{CC} (continued)

C_L = 50 pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).
See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLZ}	$\overline{OE}$	Y	1	7	10.5	1		13	ns

5.10 Switching Characteristics 5-V V_{CC}

C_L = 50 pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).
See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	Y	1	4.5	6.5	1		6.8	ns
t_{PHL}	A	Y	1	4.5	6	1		6.8	ns
t_{PZH}	$\overline{OE}$	Y	1	5	7	1		9	ns
t_{PZL}	$\overline{OE}$	Y	1	5.5	8	1		10.5	ns
t_{PHZ}	$\overline{OE}$	Y	1	6.5	9	1		10.5	ns
t_{PLZ}	$\overline{OE}$	Y	1	6	9	1		11	ns

5.11 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		1		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}				V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4		V

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5.12 Typical Characteristics

T_A = 25°C (unless otherwise noted)

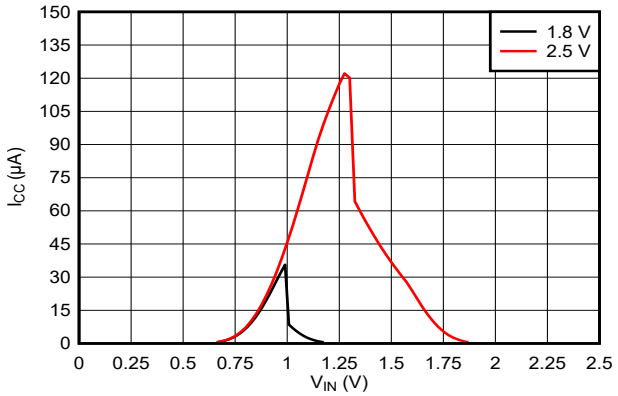


Figure 5-1. Supply Current Across Input Voltage 1.8-V and 2.5-V Supply

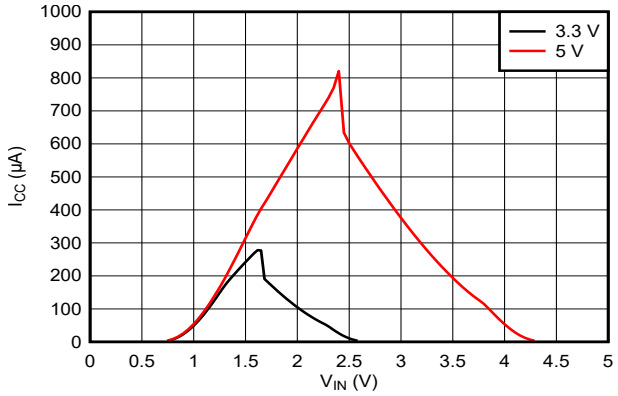


Figure 5-2. Supply Current Across Input Voltage 3.3-V and 5.0-V Supply

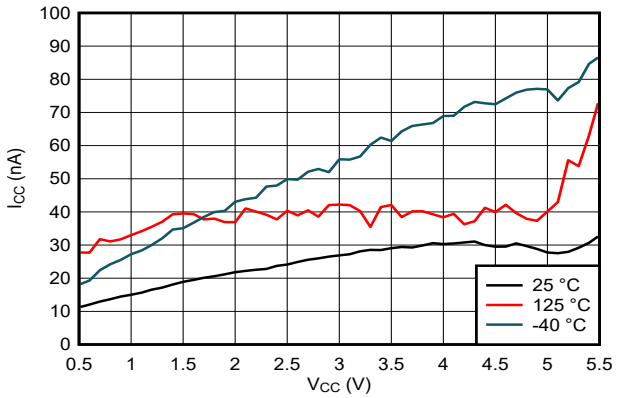


Figure 5-3. Supply Current Across Supply Voltage

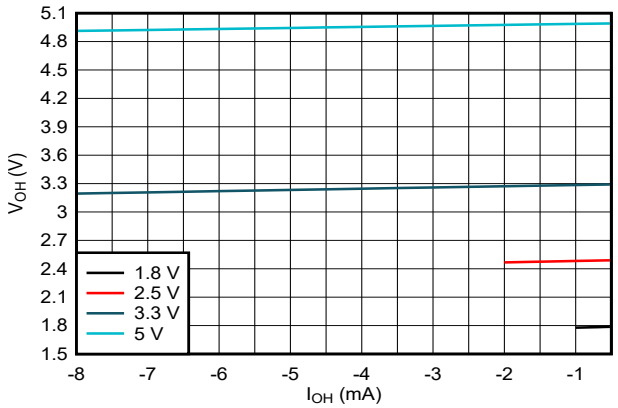


Figure 5-4. Output Voltage vs Current in HIGH State

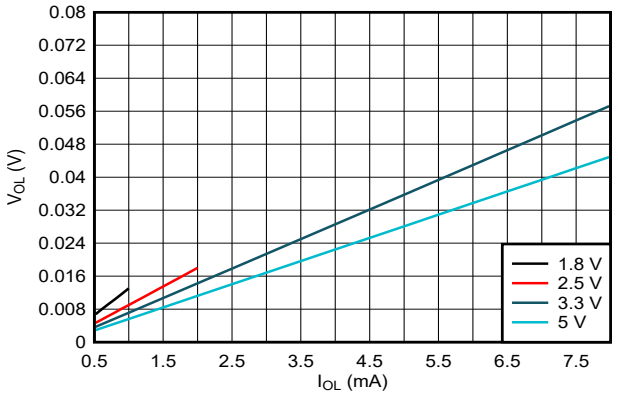


Figure 5-5. Output Voltage vs Current in LOW State

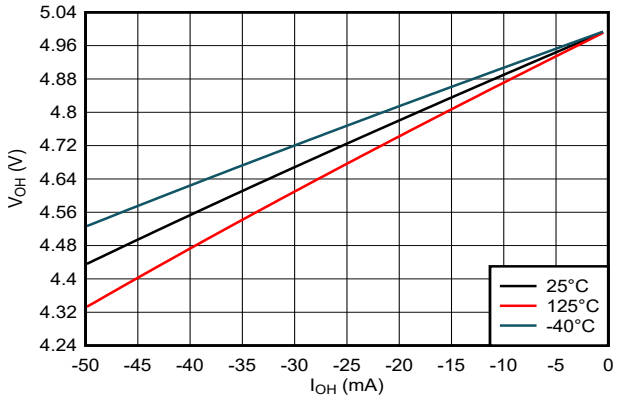


Figure 5-6. Output Voltage vs Current in HIGH State; 5-V Supply

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5.12 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

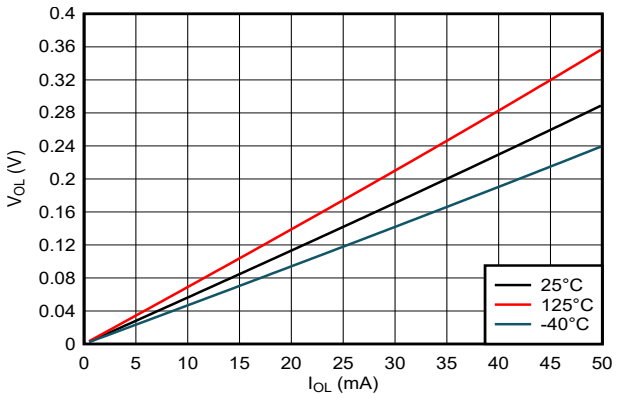


Figure 5-7. Output Voltage vs Current in LOW State; 5-V Supply

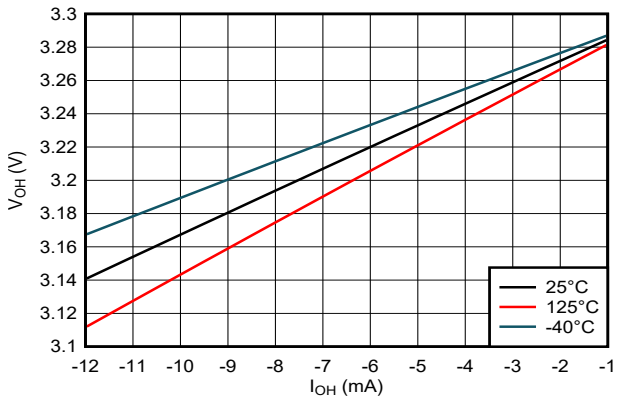


Figure 5-8. Output Voltage vs Current in HIGH State; 3.3-V Supply

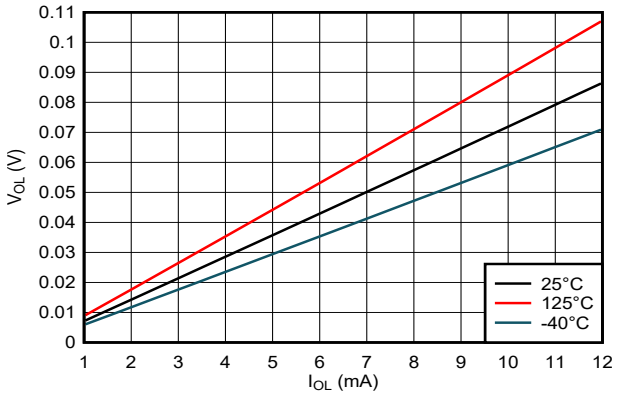


Figure 5-9. Output Voltage vs Current in LOW State; 3.3-V Supply

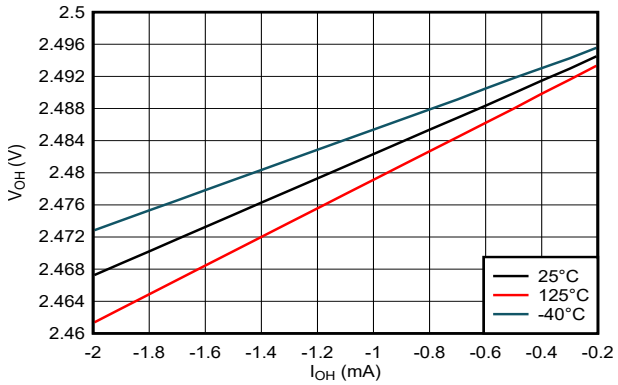


Figure 5-10. Output Voltage vs Current in HIGH State; 2.5-V Supply

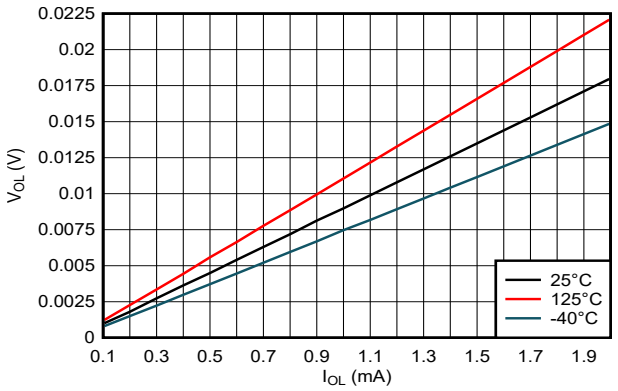


Figure 5-11. Output Voltage vs Current in LOW State; 2.5-V Supply

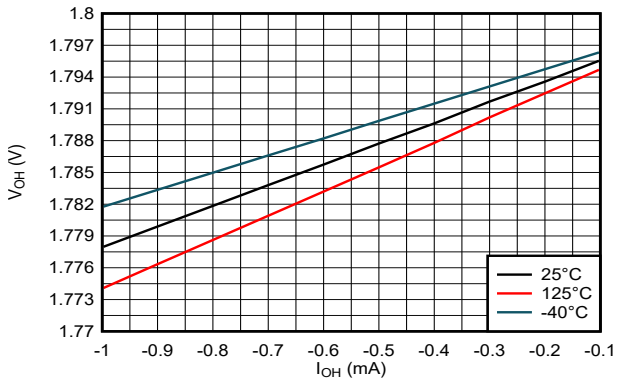


Figure 5-12. Output Voltage vs Current in HIGH State; 1.8-V Supply

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5.12 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

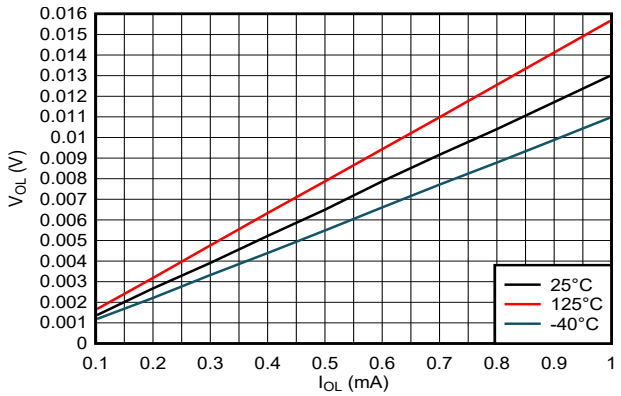


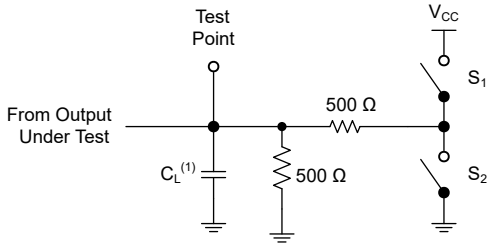
Figure 5-13. Output Voltage vs Current in LOW State; 1.8-V Supply

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 2.5 ns.

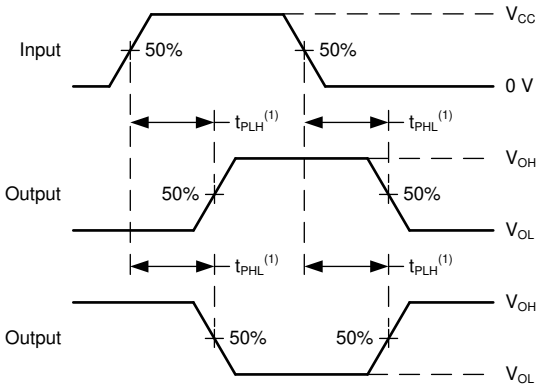
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



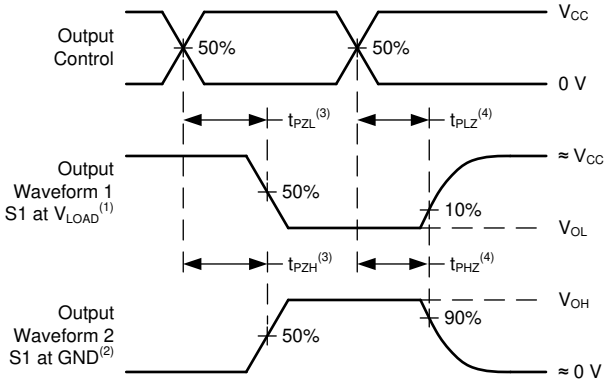
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-2. Voltage Waveforms Propagation Delays



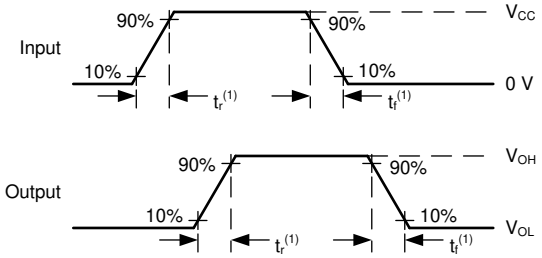
(1) S1 = CLOSED, S2 = OPEN.

(2) S1 = OPEN, S2 = CLOSED.

(3) The greater between t_{PZL} and t_{PZH} is the same as t_{en}.

(4) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis}.

Figure 6-3. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-4. Voltage Waveforms, Input and Output Transition Times

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7 Detailed Description

7.1 Overview

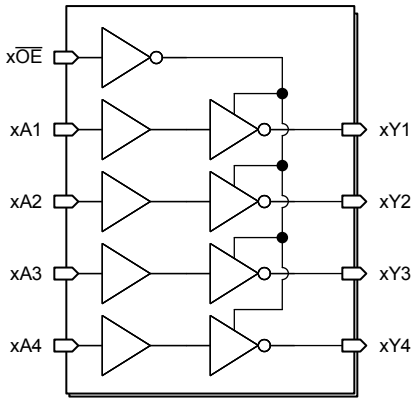
The SN74AC244-Q1 contains 8 individual high speed CMOS buffers with Schmitt-trigger inputs and 3-state outputs.

Each buffer performs the boolean logic function xYn = xAn, with *x* being the bank number and *n* being the channel number.

Each output enable ($x\overline{OE}$) controls four buffers. When the $x\overline{OE}$ pin is in the low state, the outputs of all buffers in the bank x are enabled. When the $x\overline{OE}$ pin is in the high state, the outputs of all buffers in the bank x are disabled. All disabled output are placed into the high-impedance state.

To put the device in the high-impedance state during power up or power down, tie both $\overline{OE}$ pins to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver and the leakage of the pin as defined in the *Electrical Characteristics* table.

7.2 Functional Block Diagram



Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

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7.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10kΩ resistor, however, is recommended and will typically meet all requirements.

7.3.3 Clamp Diode Structure

As shown in Figure 7-1, the inputs and outputs to this device have both positive and negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

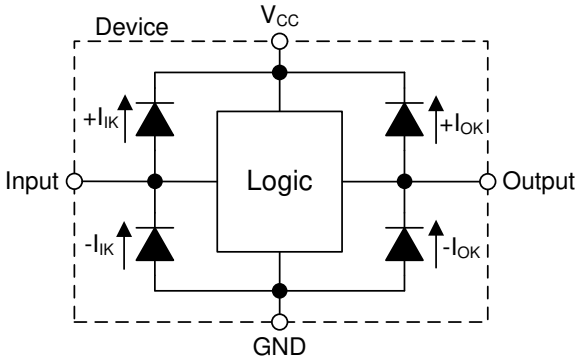


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet where packages include this feature.

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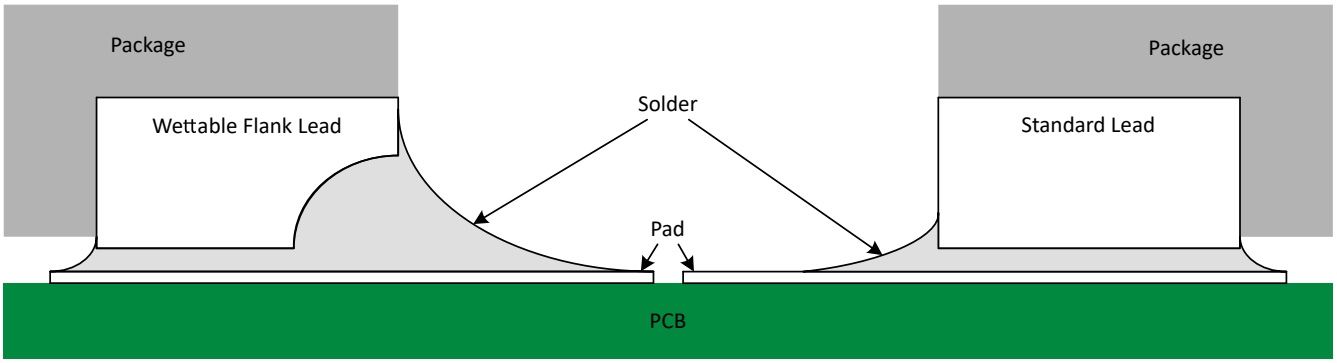


Figure 7-2. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in Figure 7-2, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74AC244-Q1.

Table 7-1. Function Table

INPUTS(1)		OUTPUTS
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care, Z = High-Impedance State

8 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AC244-Q1 can be used to drive signals over relatively long traces or transmission lines. To reduce ringing caused by impedance mismatches between the driver, transmission line, and receiver, a series damping resistor placed in series with the transmitter's output can be used. The plot in the *Application Curve* section shows the received signal with three separate resistor values. Just a small amount of resistance can make a significant impact on signal integrity in this type of application.

8.2 Typical Application

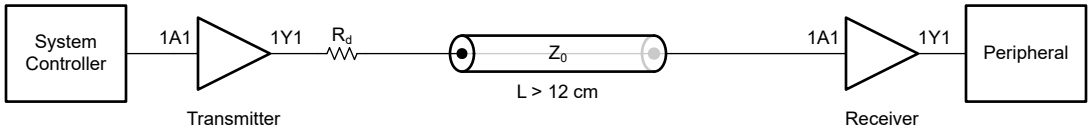


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AC244-Q1 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AC244-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74AC244-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74AC244-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

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CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AC244-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74AC244-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74AC244-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

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8.2.3 Application Curves

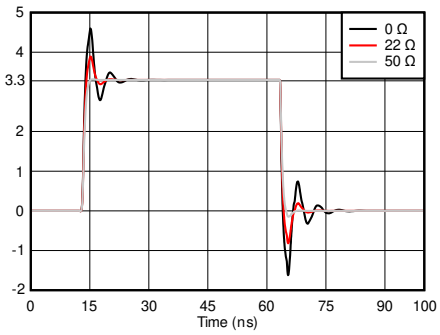


Figure 8-2. Simulated Signal Integrity at the Receiver With Different Damping Resistor (R_d) Values

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or VCC, whichever makes more sense for the logic function or is more convenient.

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8.4.2 Layout Example

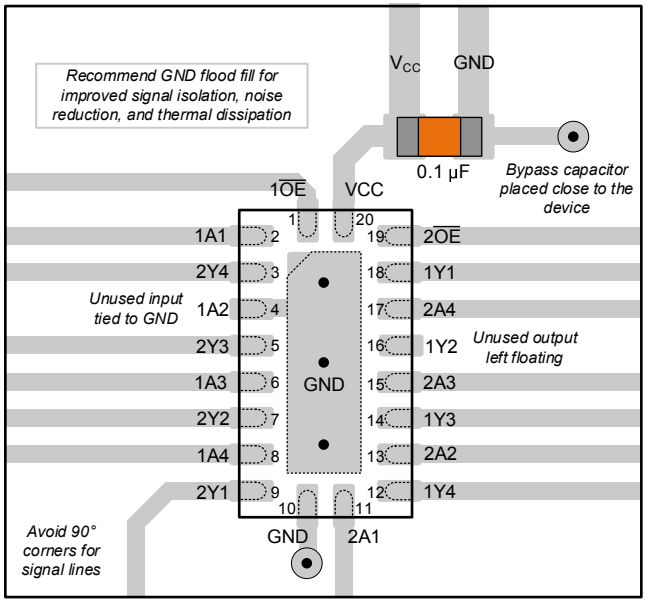


Figure 8-3. Example Layout for the SN74AC244-Q1

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (November 2023) to Revision D (March 2024)	Page
• Added DGS package to *Device Information* table, *Pin Configuration and Functions* section and *Thermal Information* table	1

Changes from Revision B (August 2023) to Revision C (November 2023)	Page
• Added *PW* package information	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PSN74AC244QWRKSRQ1	ACTIVE	VQFN	RKS	20	3000	TBD	Call TI	Call TI	-40 to 125		Samples
SN74AC244QDGSRQ1	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	244Q	Samples
SN74AC244QPWRQ1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC244Q	Samples
SN74AC244QWRKSRQ1	ACTIVE	VQFN	RKS	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC244Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AC244-Q1 :

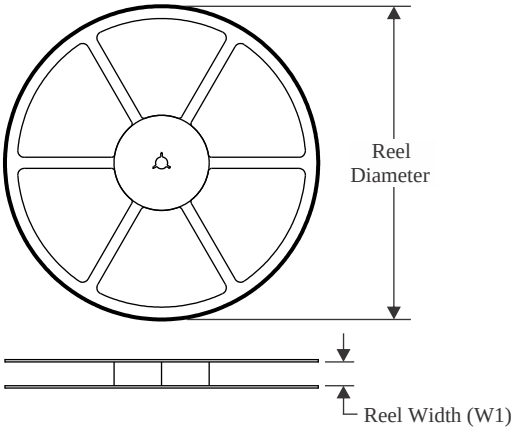
- Catalog : SN74AC244
- Enhanced Product : SN74AC244-EP
- Military : SN54AC244

NOTE: Qualified Version Definitions:

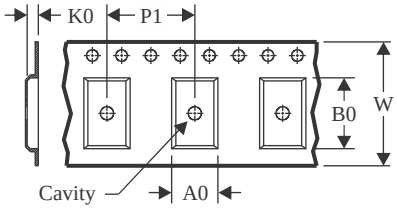
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

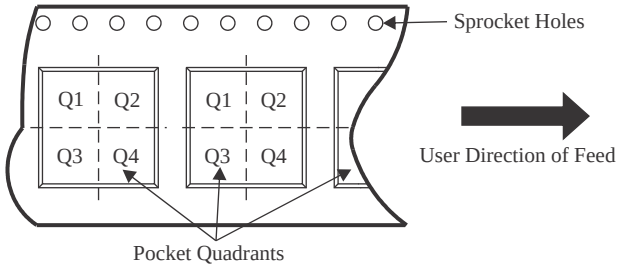


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

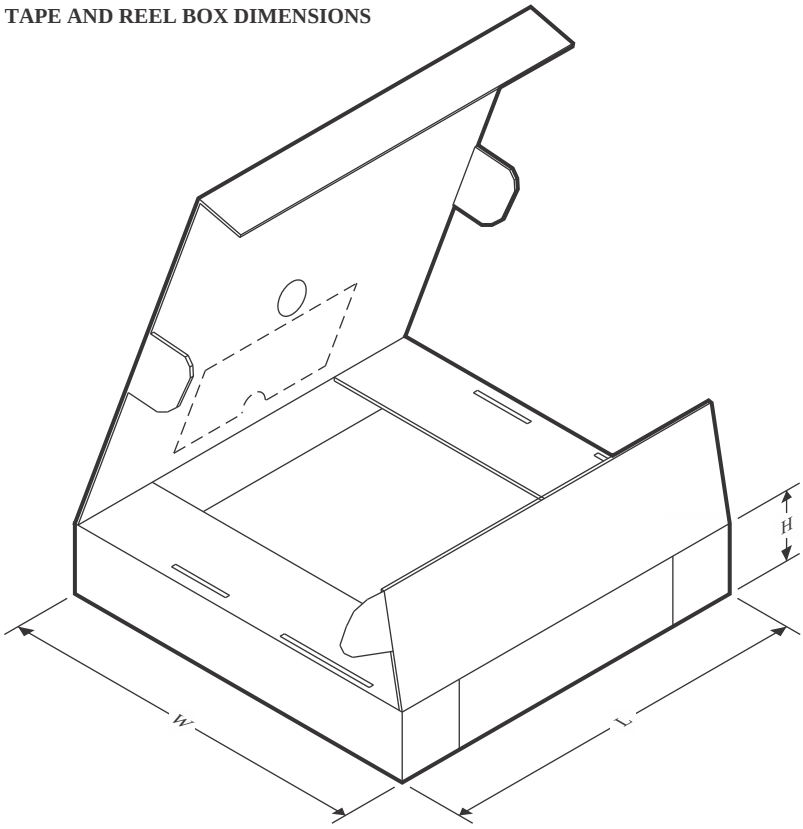
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC244QDGSRQ1	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74AC244QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AC244QWRKSRQ1	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC244QDGSRQ1	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74AC244QPWRQ1	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74AC244QWRKSRQ1	VQFN	RKS	20	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

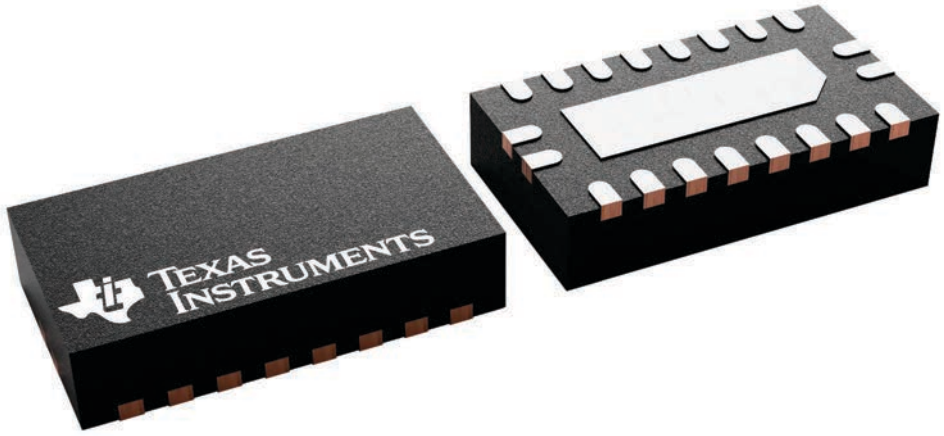
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



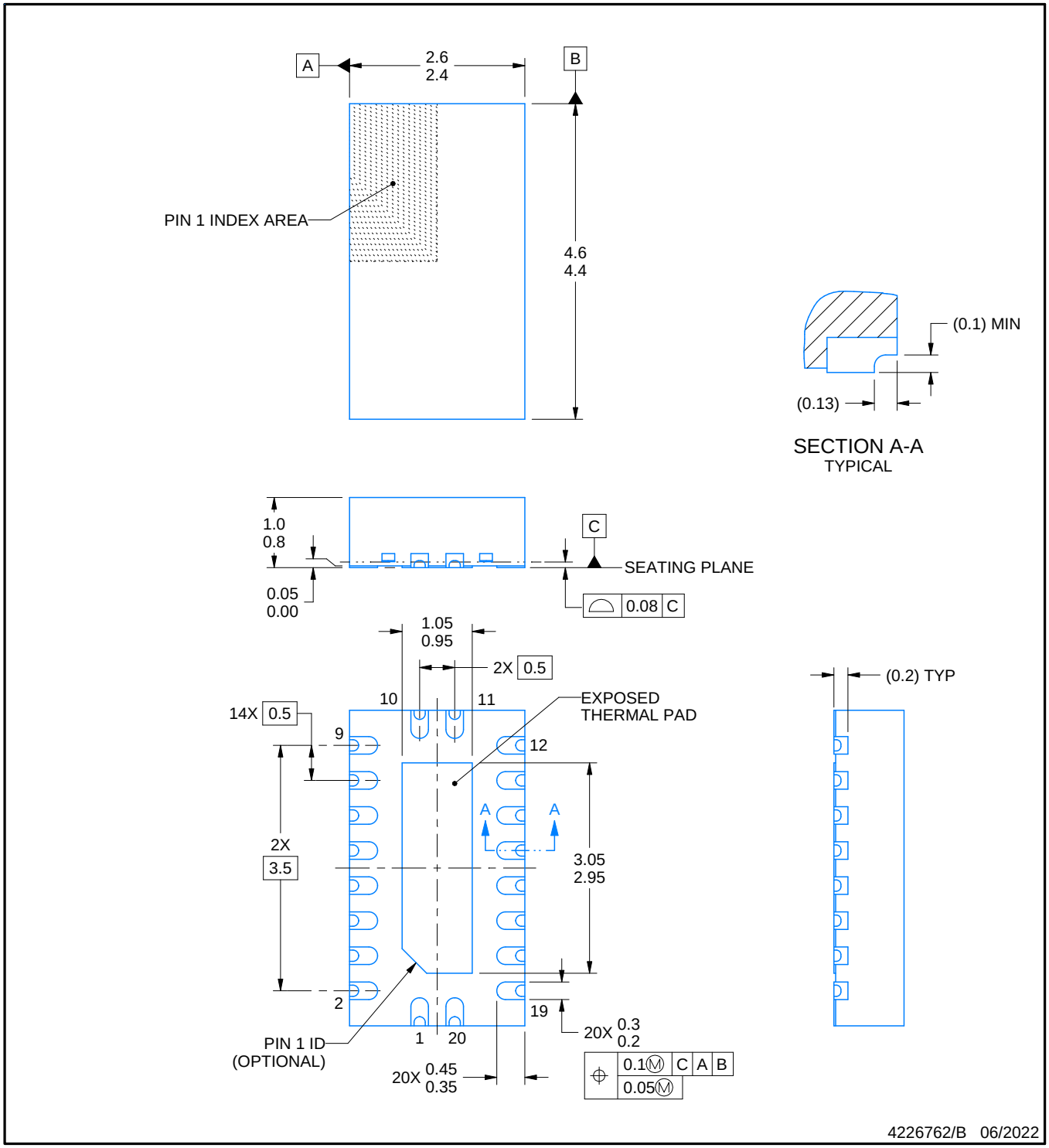
RKS0020B



PACKAGE OUTLINE

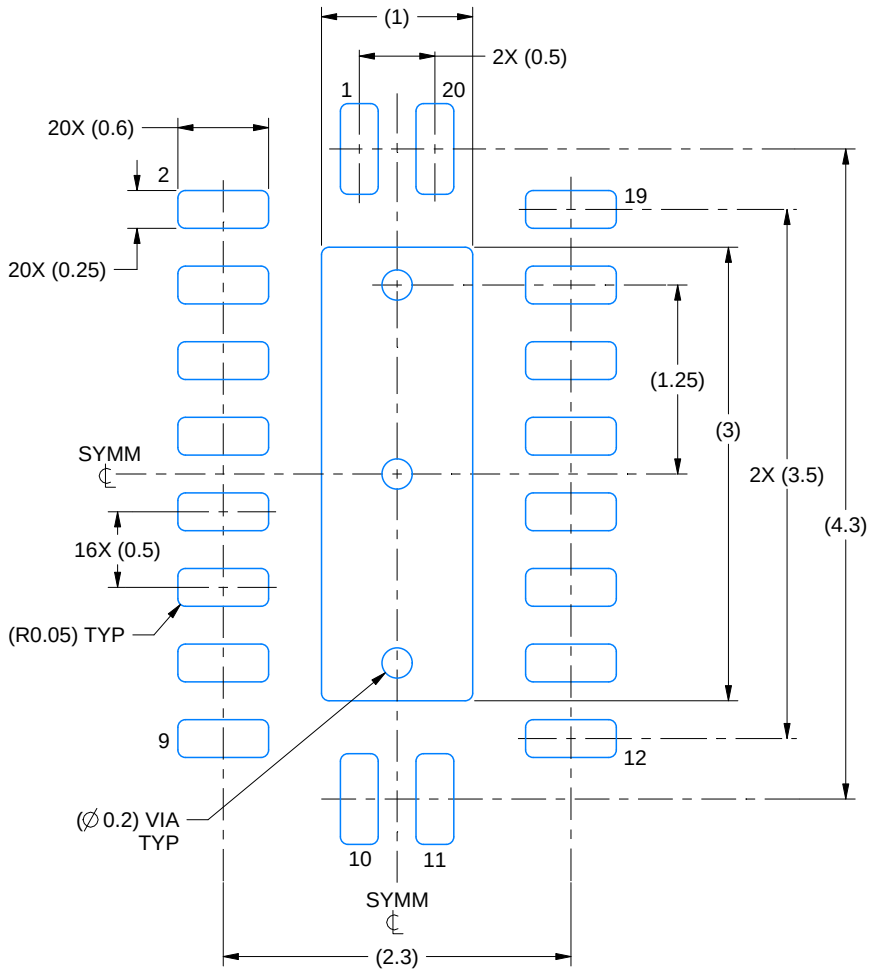
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



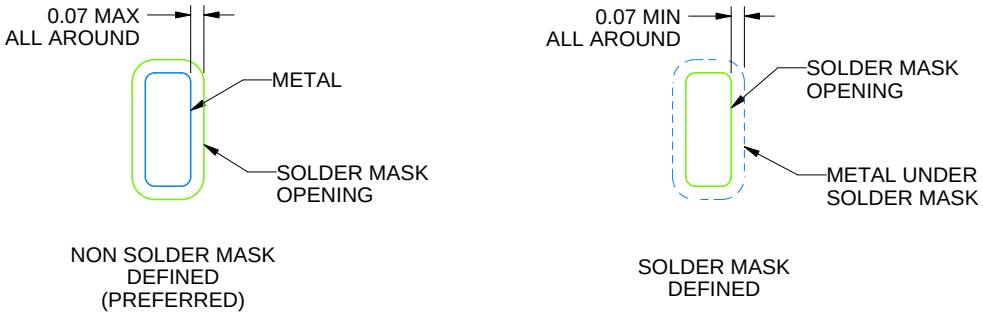
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE:20X

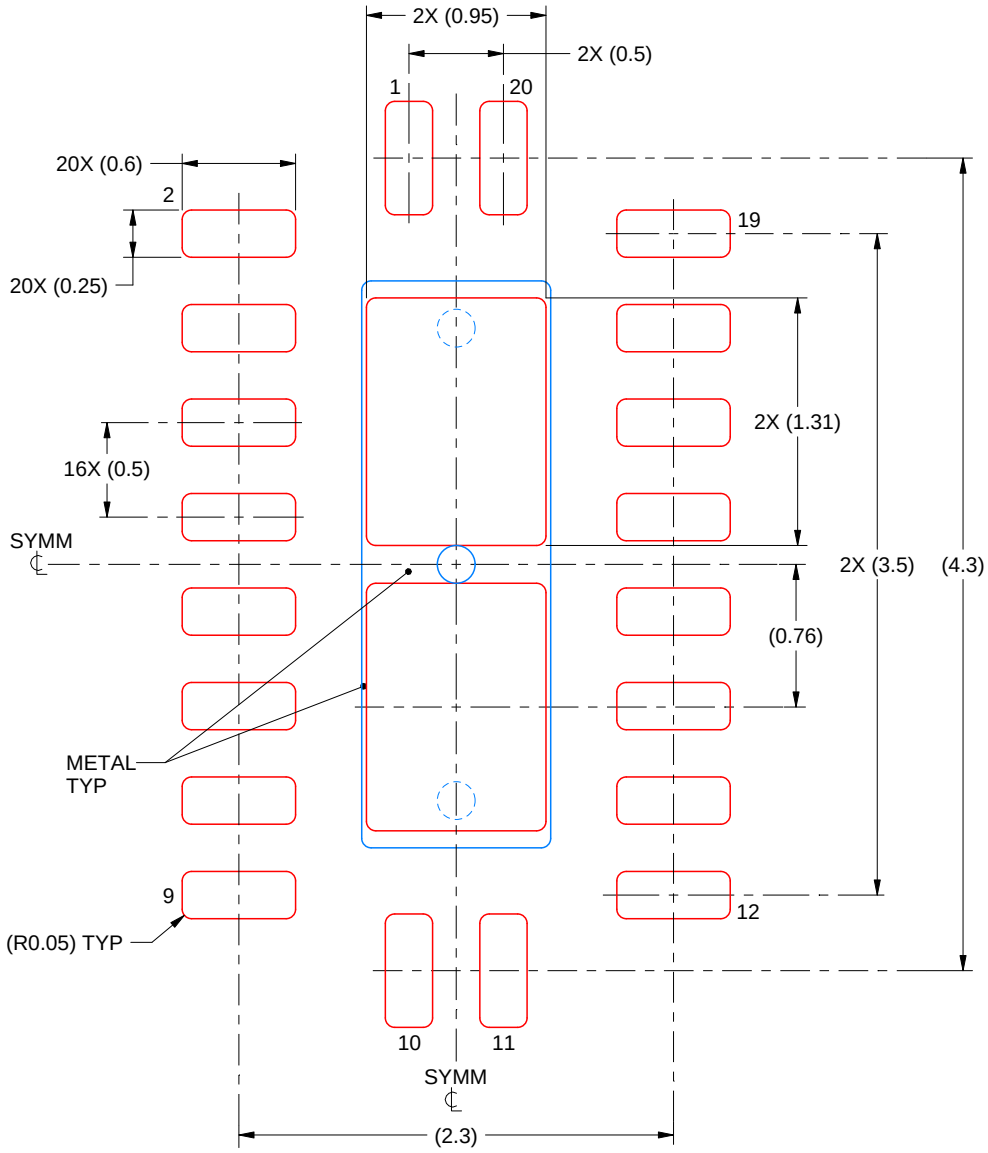


SOLDER MASK DETAILS

4226762/B 06/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4226762/B 06/2022

NOTES: (continued)

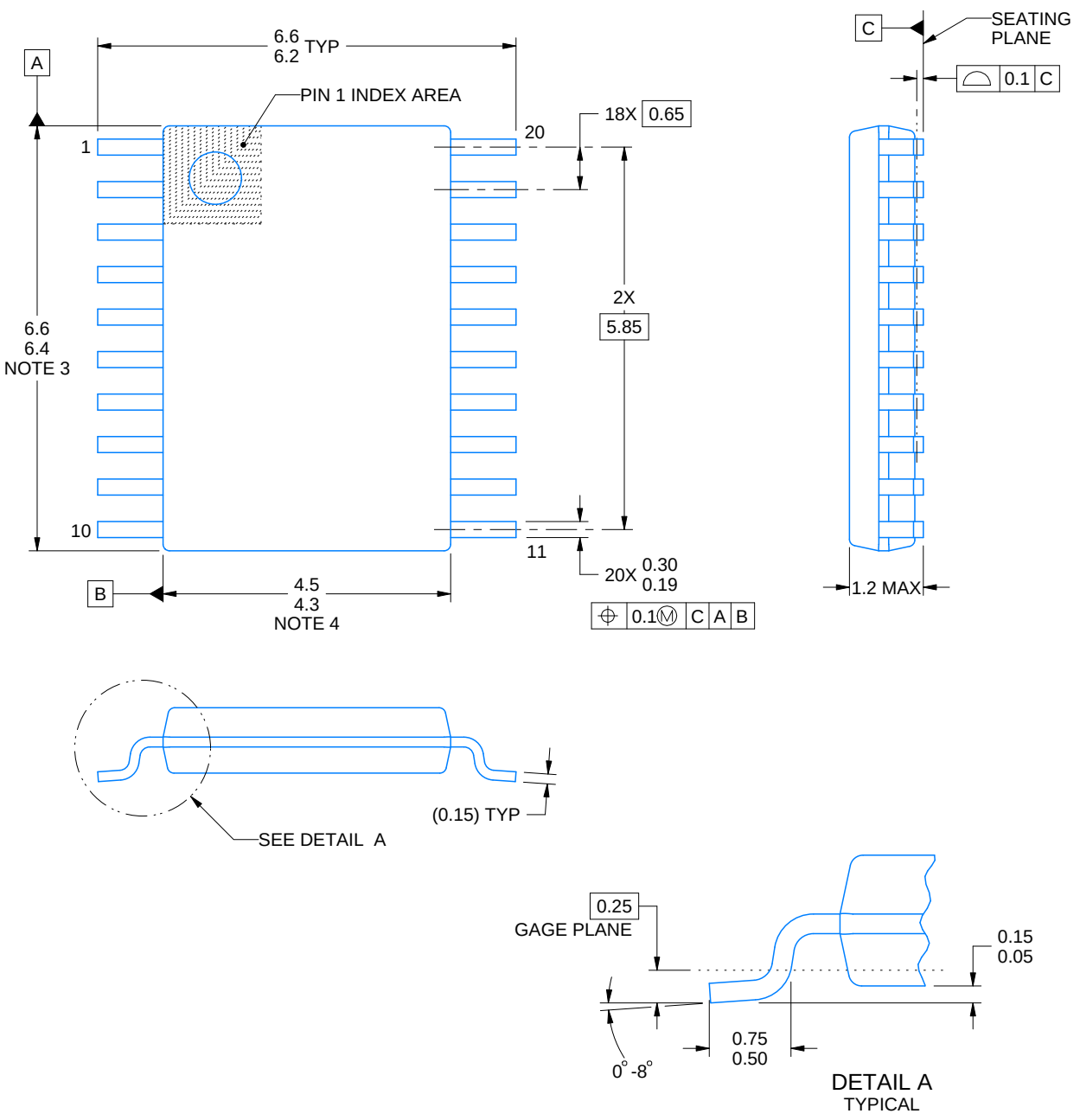
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0020A

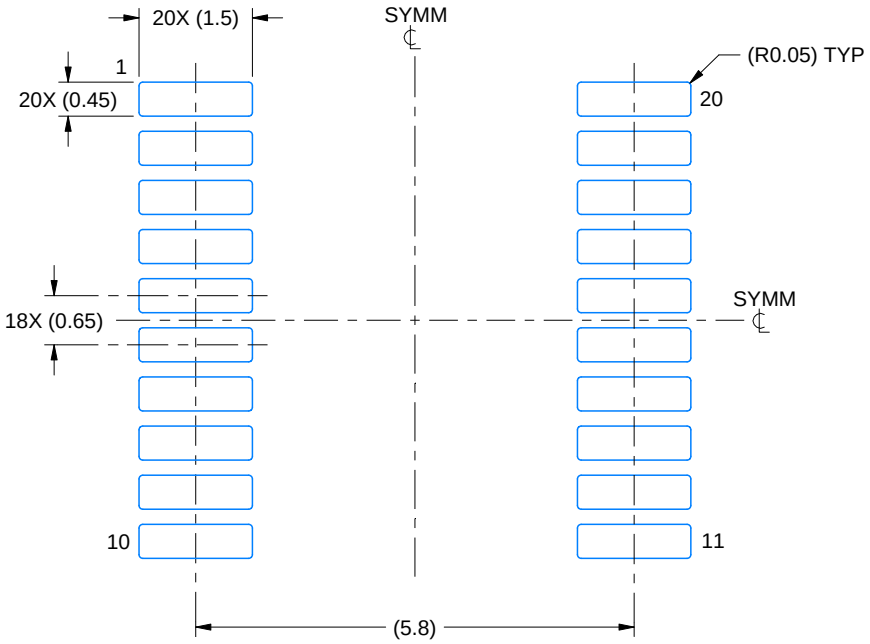
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

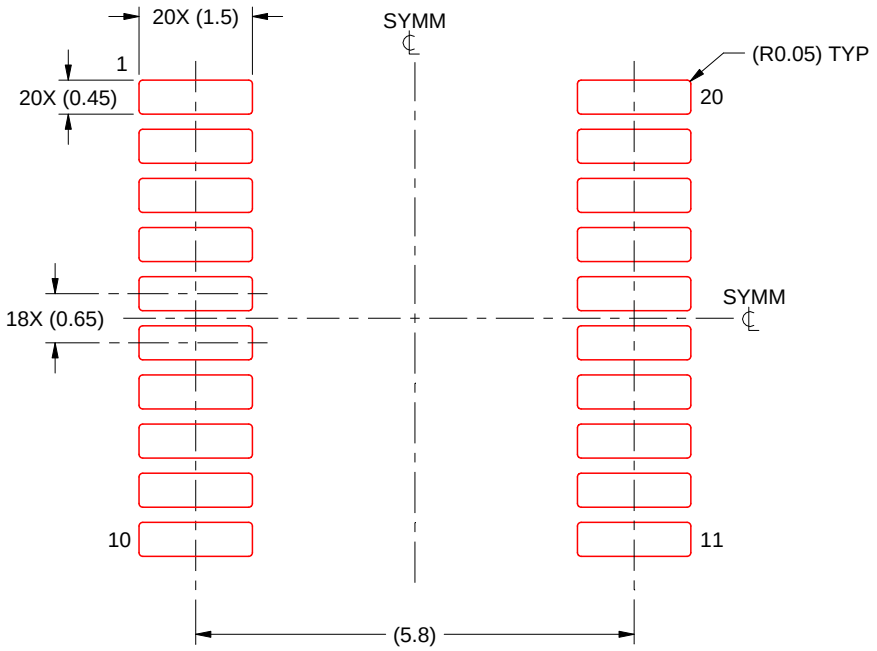


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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