TPS653850A-Q1 and TPS653852A-Q1 Multirail Power Supply for Microcontrollers in Safety-Relevant Applications

1 Device Overview

1.1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Input Voltage Range
  - 7 to 36-V for Initial Battery Power Up
  - 4 to 36-V Full Functionality After Initial Battery Power Up
  - Minimum 2.3 V During Operation After Wake-up
- Supply Rails (With Internal FETs)
  - 6-V Synchronous Buck-Boost Preregulator
  - 5-V, 285-mA LDO (CAN, Peripherals or ADC REF 1% accuracy with 20 to 120 mA load)
  - 3.3-V or 5-V, 350-mA LDO (MCU) TPS653850A-Q1. 3.3-V 350-mA or 5-V 500 mA LDO (MCU) TPS653852A-Q1
  - 2 LDOs Protected for Sensor Supply or Peripherals
    - 120 mA for Sensor Supply 1 (VSOUT1), 100 mA for Sensor Supply 2 (VSOUT2)
    - Configurable Tracking Mode (Tracking Input Pin), or 3.3-V or 5-V Fixed Output Voltage
    - Short-to-Ground and Battery Protection
  - Charge Pump: 6-V Minimum, 11-V Maximum Above Battery Voltage
- Monitoring and Protection
  - Independent Undervoltage and Overvoltage Monitoring on All Regulator Outputs, Battery Voltage, and Internal Supplies
  - Voltage Monitoring Circuitry, Including Independent Bandgap Reference, Supplied from Separate Battery Voltage Input Pin
  - Self-Check on All Voltage Monitoring (During Power-Up and After Power-Up Initiated by External MCU)
  - All Supplies Protected With Current Limit and Overtemperature Prewarning and Shutdown
- Microcontroller Interface
  - Open and Close Window or Question-Answer Watchdog Function
  - Monitor for Functional Safety MCU Fault output (PWM or level), MCU Error-Signal Monitor
  - DIAGNOSTIC state for Performing Device Self-Tests and System Diagnostics
  - SAFE State for Device and System Protection upon Detected System Failure
  - Clock Monitor for Internal Oscillator
  - Analog and Logic Built-In Self-Test
  - CRC on Non-Volatile Memory as well as Device and System Configuration Registers and SPI Communications
  - Reset Circuit for MCU
  - Diagnostic Output Pin
- SPI With CRC on Command Plus Data
- Error Reporting Through SPI Registers for Errors on System Level and Device Level
- Enable-Drive Output for Disabling External Power-Stages on Any Detected System Failure
- Wake-up through IGN Pin (ignition) or CAN_WU Pin (transceiver or other function)
- 48-Pin HTSSOP PowerPAD™ IC Package

1.2 Applications

- Automotive Safety-Relevant Applications
- Industrial Safety-Relevant Applications

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

1.3 Description

The TPS653850A-Q1 and TPS653852A-Q1 device is a multirail power supply designed to supply microcontrollers in safety relevant applications, such as those found in the automotive industry. The device supports functional safety microcontrollers with dual-core lockstep (LS) and other multi-core architectures.

The TPS653850A-Q1 and TPS653852A-Q1 device integrates multiple supply rails to power the MCU, CAN or FlexRay, and external sensors. A buck-boost converter with internal FETs converts the input battery voltage between 2.3 V and 36 V to a 6-V preregulator output that supplies the other regulators. An integrated charge pump provides an overdrive voltage for the internal regulators, and can also be used to drive an external NMOS FET as reverse battery protection. The device supports wake-up from an ignition signal (IGN pin) or wake-up from a CAN transceiver or other signal (CAN_WU pin).

An independent voltage monitoring unit inside the device monitors undervoltage and overvoltage on all internal supply rails and regulator outputs of the battery supply. Regulator current limits and temperature protections are also implemented. The TPS653850A-Q1 and TPS653852A-Q1 device features a question-answer watchdog, MCU error-signal monitor, clock monitoring on internal oscillator, self-check on clock monitor, cyclic redundancy check (CRC) on non-volatile memory and SPI communication, a diagnostic output pin allowing MCU to observe device internal analog and digital signals, a reset circuit for the MCU (NRES pin) and a safing output (ENDRV pin) to disable external power-stages on any detected system-failure. The device automatically runs a built-in self-test (BIST) at start up and the MCU may re-run the BIST during system run time through software control if needed. A dedicated DIAGNOSTIC state allows the MCU to check TPS653850A-Q1 and TPS653852A-Q1 functionality.

The TPS653850A-Q1 and TPS653852A-Q1 device also has an error reporting capability through the SPI register. The device has separate status bits in the SPI register for each specific error on the system level or device level. When the device detects a particular error condition, it sets the appropriate status bit and keeps this status bit set until the MCU reads-out the SPI register in which this status bit was set. Based on which status bit was set, the MCU can decide whether it must keep the system in a safe state or whether it can resume with the operation of the system.

The TPS653850A-Q1 and TPS653852A-Q1 device is available in a 48-pin HTSSOP PowerPAD™ IC package.

Table 1-1. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
TPS653850A-Q1 and TPS653852A-Q1	HTSSOP (48)	12.50 mm × 6.10 mm

(1) For more information, see Section 4, *Mechanical Packaging and Orderable Information*.

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1.4 Typical Application Diagram

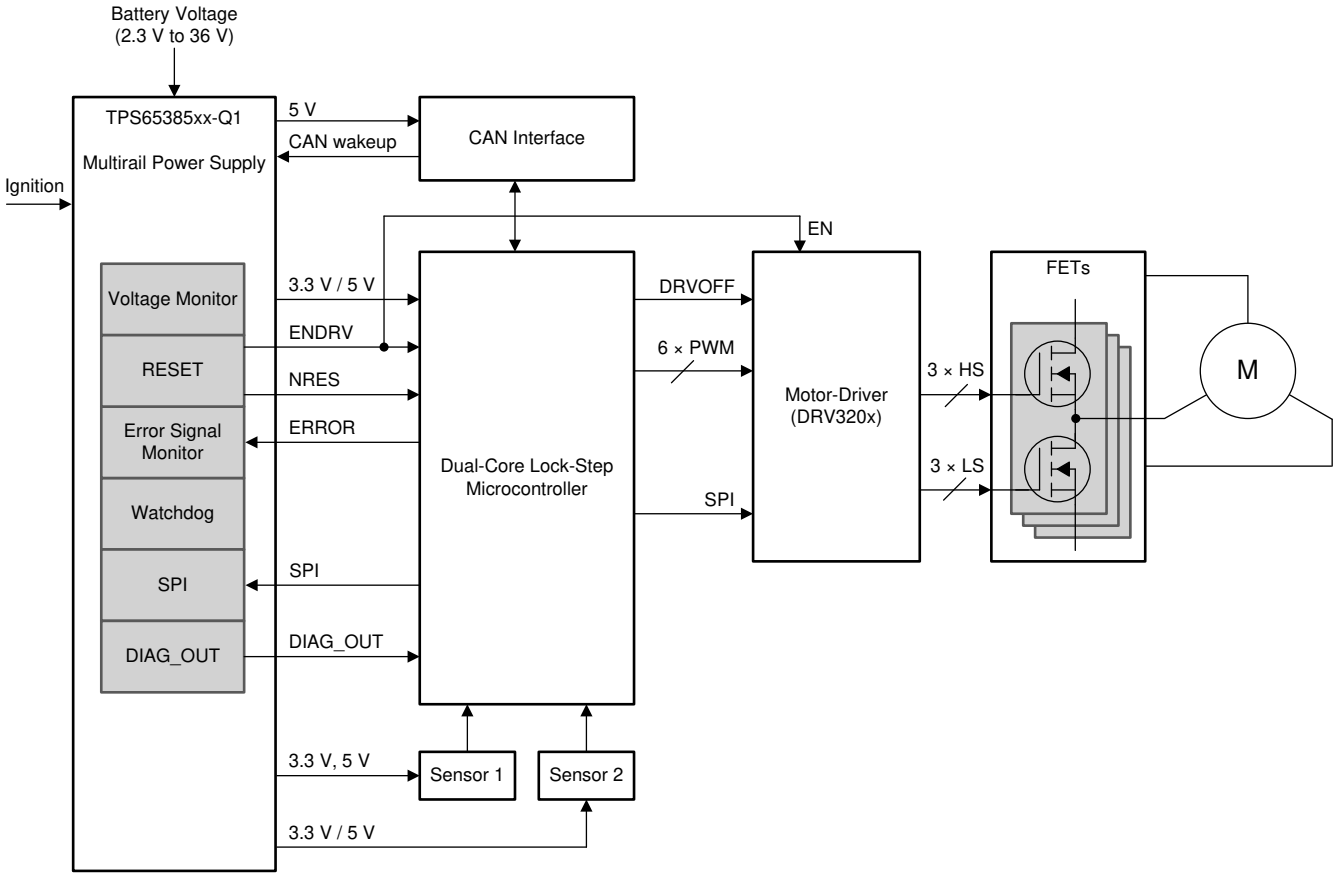


Figure 1-1. Typical Application Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2020	*	Initial Release

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3 Device and Documentation Support

3.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 3-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS653850A-Q1	Click here	Click here	Click here	Click here	Click here
TPS653852A-Q1	Click here	Click here	Click here	Click here	Click here

3.2 Documentation Support

3.2.1 Related Documentation

For related documentation see the following:

- Texas instruments, *DRV3201-Q1 3 Phase Motor Driver-IC for Automotive Safety Applications* data sheet
- Texas instruments, *DRV3205-Q1 Three-Phase Automotive Gate Driver With Three Integrated Current Shunt Amplifiers and Enhanced Protection, Diagnostics, and Monitoring* data sheet

3.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

3.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

3.5 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.

3.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

3.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

4 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
O3850AQDCARQ1	ACTIVE	HTSSOP	DCA	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	O3850A	Samples
O3852AQDCARQ1	PREVIEW	HTSSOP	DCA	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	O3852A	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

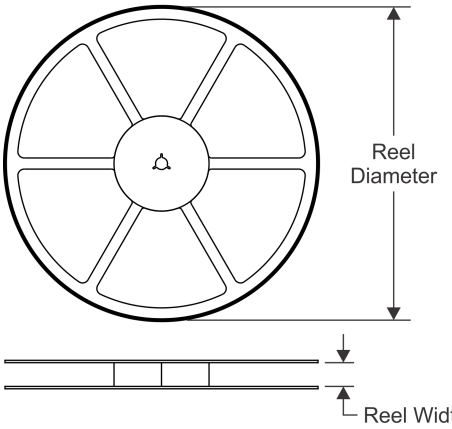
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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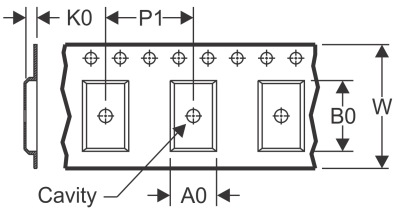
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

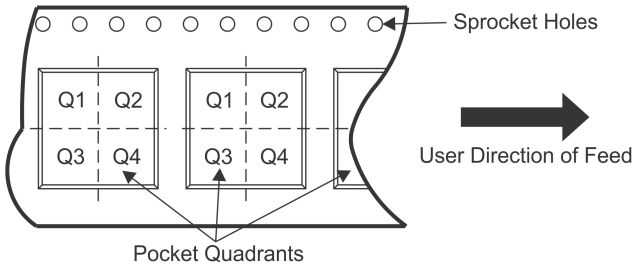


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

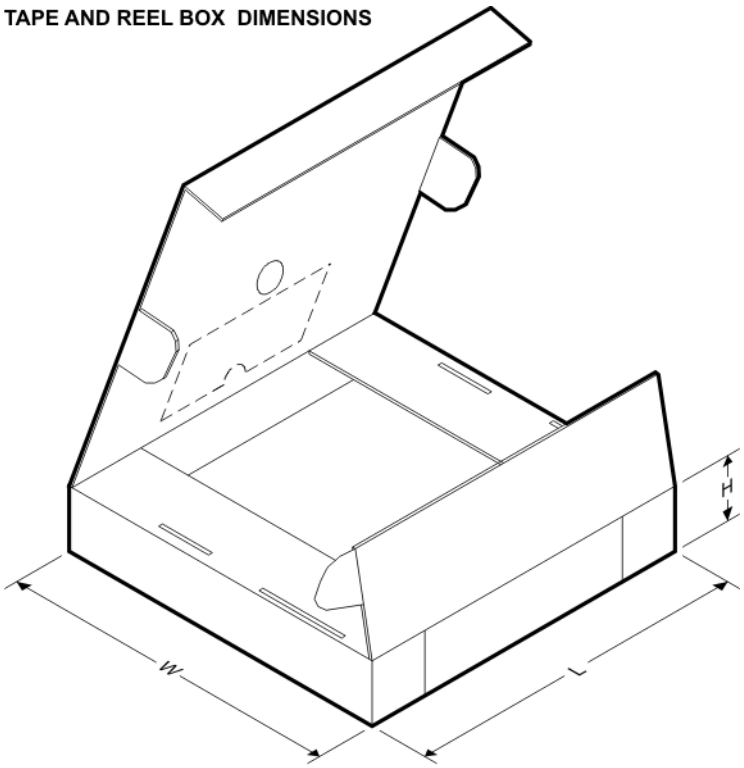
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
O3850AQDCARQ1	HTSSOP	DCA	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

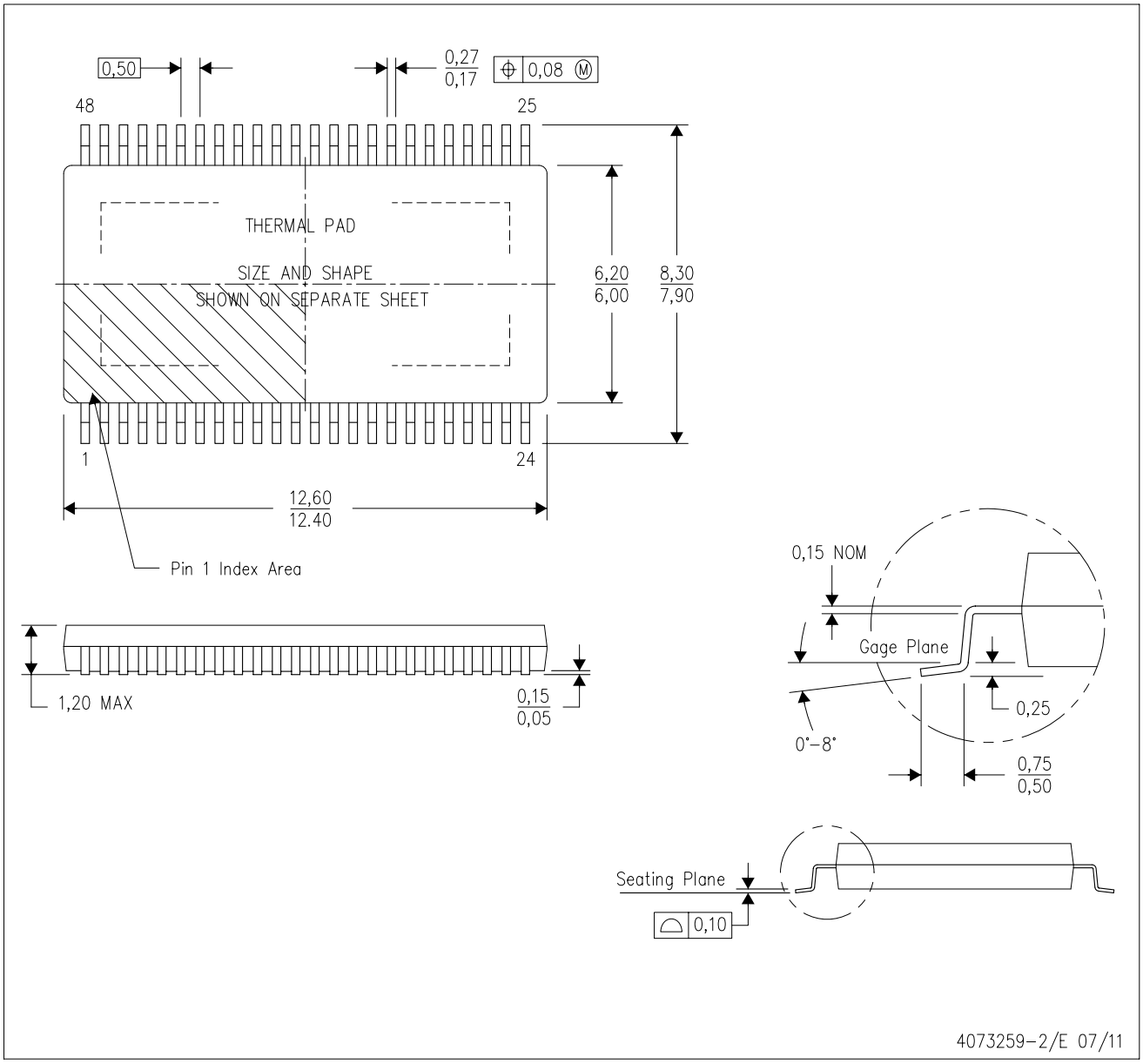
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
O3850AQDCARQ1	HTSSOP	DCA	48	2000	350.0	350.0	43.0

DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

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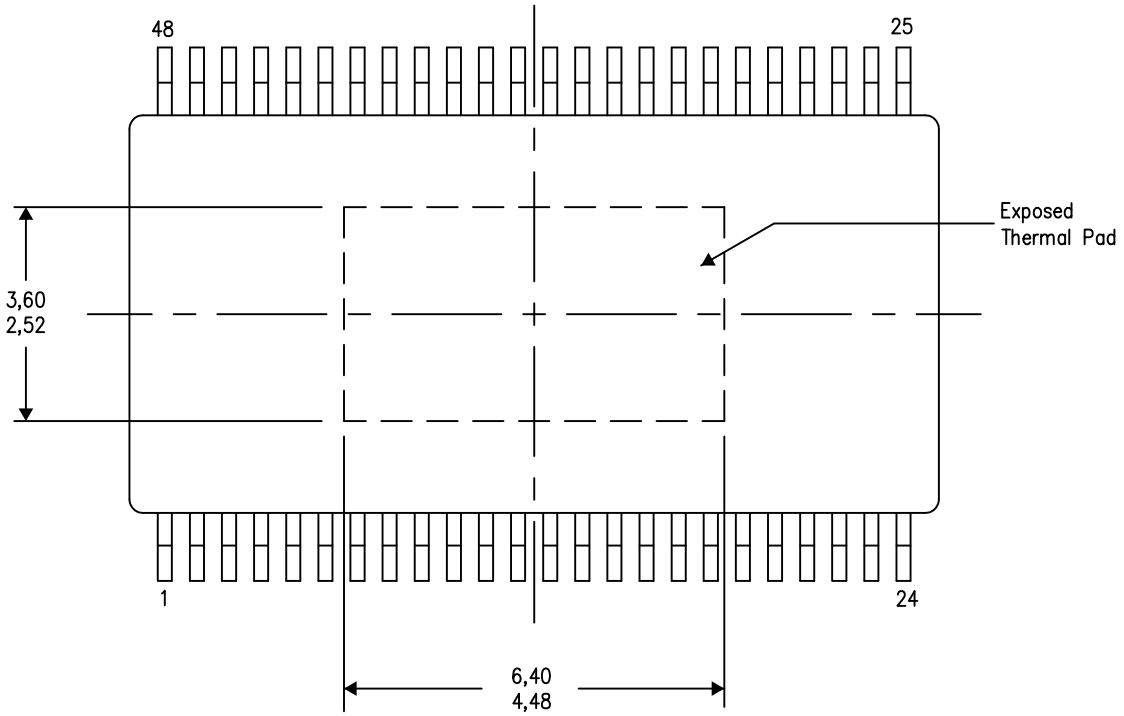
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

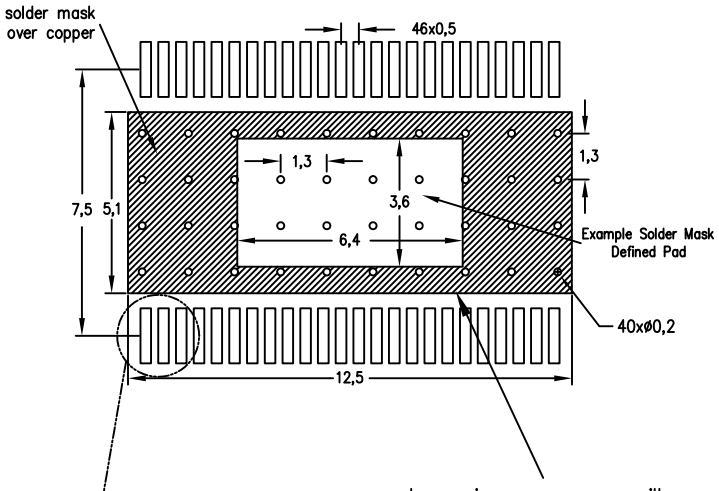
4206320–4/S 11/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

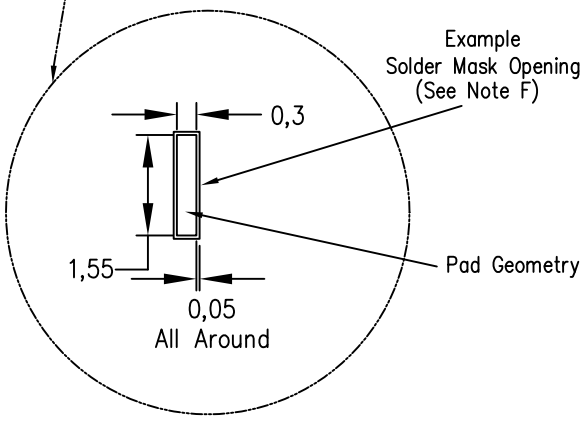
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints

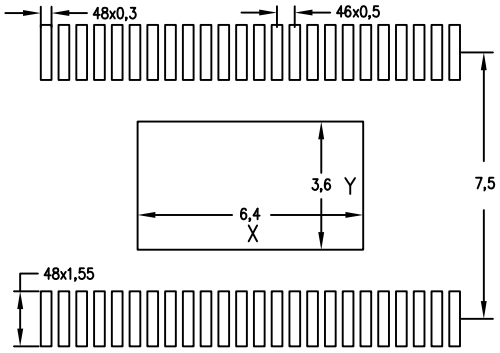


Increasing copper area will
enhance thermal performance
(See Note D)

Example
Non Soldermask Defined Pad



Stencil openings based
on a stencil thickness of .127mm
Reference table below for other
solder stencil thicknesses



(See Note E)

Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	7.21	4.06
0.127mm	6.40	3.60
0.152mm	5.85	3.29
0.178mm	5.41	3.04

4208546–3/H 11/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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LP3990TLX-1.8/NOPB TS5V330CDBQR LM431CIM/NOPB LMP7731MA/NOPB LP38691DT-3.3 OPA4137P
OPA4243EA/2K5 LP3882EMR-1.5/NOPB REG101NA-2.85/3K SN65LBC171DB UC3854BDW
SN74AHC594D TPS73018DBVR LM2671N-3.3/NOPB LM2831YSD/NOPB TMS320DM6437ZWT6
TPS566250DDA LM2852XMXAX-2.5/NOPB LP2989AIM-1.8/NOPB TPS2056AD TPS70751MPWPREP
GD75323DWR SCAN926260TUFX/NOPB TPS51462RGER CSD95410RRB DS90UB903QSQ/NOPB