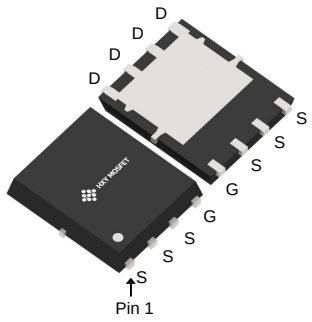
# SI7388DP-T1-GE3

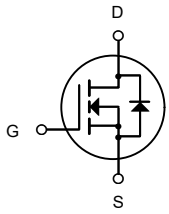
N-Channel Enhancement Mode MOSFET

## Description

The SI7388DP-T1-GE3 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.




DFN5X6-8L




N-Channel MOSFET

## General Features

$V_{DS}$ = 30V $I_D$ = 60A

$R_{DS(ON)}$ < 7mΩ $V_{GS}$=10V

## Application

Battery protection

Load switch

Uninterruptible power supply

## Package Marking and Ordering Information

| Product ID | Pack | Brand | Qty(PCS) |
|---|---|---|---|
| SI7388DP-T1-GE3 | DFN5X6-8L | HXY MOSFET | 5000 |

## Absolute Maximum Ratings ($T_C$=25°C unless otherwise noted)

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage | 30 | V |
| $V_{GS}$ | Gate-Source Voltage | ±20 | V |
| $I_D$@$T_C$=25°C | Continuous Drain Current, $V_{GS}$ @ 10V[1] | 60 | A |
| $I_D$@$T_C$=100°C | Continuous Drain Current, $V_{GS}$ @ 10V[1] | 42 | A |
| $I_{DM}$ | Pulsed Drain Current[2] | 160 | A |
| EAS | Single Pulse Avalanche Energy[3] | 115.2 | mJ |
| $I_{AS}$ | Avalanche Current | 48 | A |
| $P_D$@$T_C$=25°C | Total Power Dissipation[4] | 59 | W |
| $T_{STG}$ | Storage Temperature Range | -55 to 150 | °C |
| $T_J$ | Operating Junction Temperature Range | -55 to 150 | °C |
| $R_{\theta JA}$ | Thermal Resistance Junction-Ambient [1] | 62 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance Junction-Case[1] | 2.1 | °C/W |

## Electrical Characteristics ($T_J$=25°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V , $I_D$=250uA | 30 | --- | --- | V |
| $\triangle BV_{DSS}/\triangle T_J$ | BVDSS Temperature Coefficient | Reference to 25℃ , $I_D$=1mA | --- | 0.028 | --- | V/°C |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance[2] | $V_{GS}$=10V , $I_D$=30A | --- | 5.7 | 7 | mΩ |
| | | $V_{GS}$=4.5V , $I_D$=15A | --- | 11 | 13 | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS}$=$V_{DS}$ , $I_D$ =250uA | 1.2 | --- | 2.5 | V |
| $\triangle V_{GS(th)}$ | $V_{GS(th)}$ Temperature Coefficient | | --- | -6.16 | --- | mV/°C |
| $I_{DSS}$ | Drain-Source Leakage Current | $V_{DS}$=24V , $V_{GS}$=0V , $T_J$=25°C | --- | --- | 1 | uA |
| | | $V_{DS}$=24V , $V_{GS}$=0V , $T_J$=55°C | --- | --- | 5 | |
| $I_{GSS}$ | Gate-Source Leakage Current | $V_{GS}$=±20V , $V_{DS}$=0V | --- | --- | ±100 | nA |
| gfs | Forward Transconductance | $V_{DS}$=5V , $I_D$=30A | --- | 43 | --- | S |
| $R_g$ | Gate Resistance | $V_{DS}$=0V , $V_{GS}$=0V , f=1MHz | --- | 1.7 | --- | Ω |
| $Q_g$ | Total Gate Charge (4.5V) | $V_{DS}$=15V , $V_{GS}$=4.5V , $I_D$=15A | --- | 20 | --- | nC |
| $Q_{gs}$ | Gate-Source Charge | | --- | 7.6 | --- | |
| $Q_{gd}$ | Gate-Drain Charge | | --- | 7.2 | --- | |
| $T_{d(on)}$ | Turn-On Delay Time | $V_{DD}$=15V , $V_{GS}$=10V , $R_G$=3.3Ω $I_D$=15A | --- | 7.8 | --- | ns |
| $T_r$ | Rise Time | | --- | 15 | --- | |
| $T_{d(off)}$ | Turn-Off Delay Time | | --- | 37.3 | --- | |
| $T_f$ | Fall Time | | --- | 10.6 | --- | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$=15V , $V_{GS}$=0V , f=1MHz | --- | 2295 | --- | pF |
| $C_{oss}$ | Output Capacitance | | --- | 267 | --- | |
| $C_{rss}$ | Reverse Transfer Capacitance | | --- | 210 | --- | |
| $I_S$ | Continuous Source Current[1,5] | $V_G$=$V_D$=0V , Force Current | --- | --- | 81 | A |
| $I_{SM}$ | Pulsed Source Current[2,5] | | --- | --- | 160 | A |
| $V_{SD}$ | Diode Forward Voltage[2] | $V_{GS}$=0V , $I_S$=1A , $T_J$=25°C | --- | --- | 1 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$=30A, dI/dt=100A/μs , $T_J$=25℃ | --- | 14 | --- | nS |
| $Q_{rr}$ | Reverse Recovery Charge | | --- | 5 | --- | nC |

Note :
1.The data tested by surface mounted on a 1 inch$^2$ FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is $V_{DD}$=25V,$V_{GS}$=10V,L=0.1mH,$I_{AS}$=48A
4.The power dissipation is limited by 150°C junction temperature
5.The data is theoretically the same as $I_D$ and $I_{DM}$ , in real applications , should be limited by total power dissipation.

## Typical Characteristics

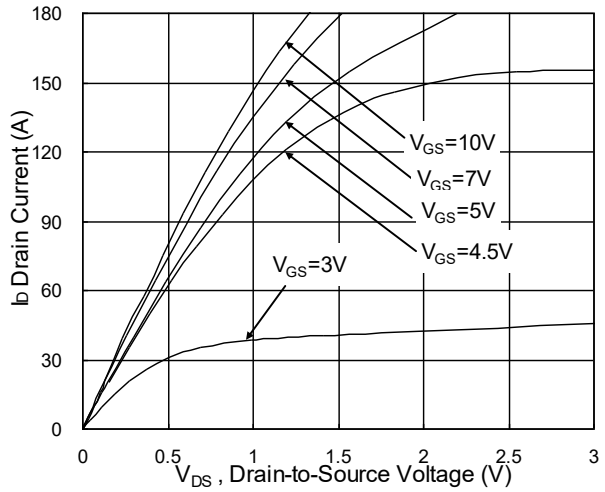



**Fig.1 Typical Output Characteristics**

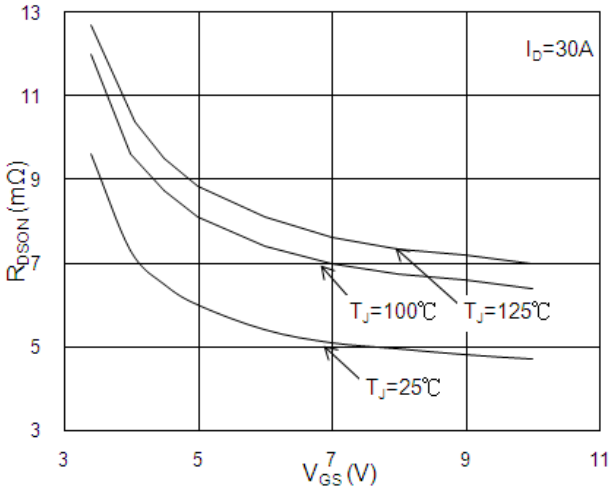



**Fig.2 On-Resistance vs. G-S Voltage**

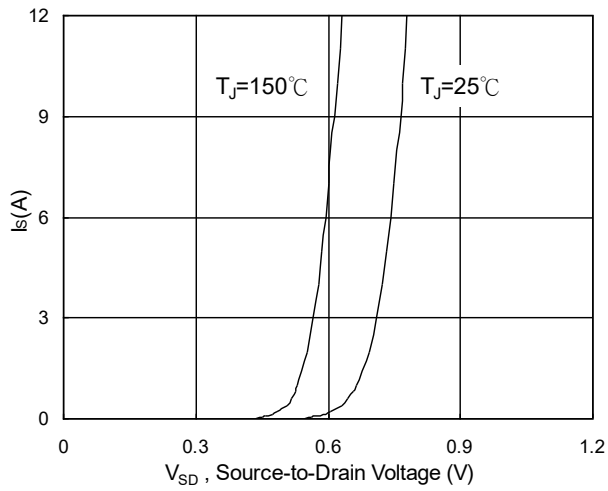



**Fig.3 Forward Characteristics of Reverse**

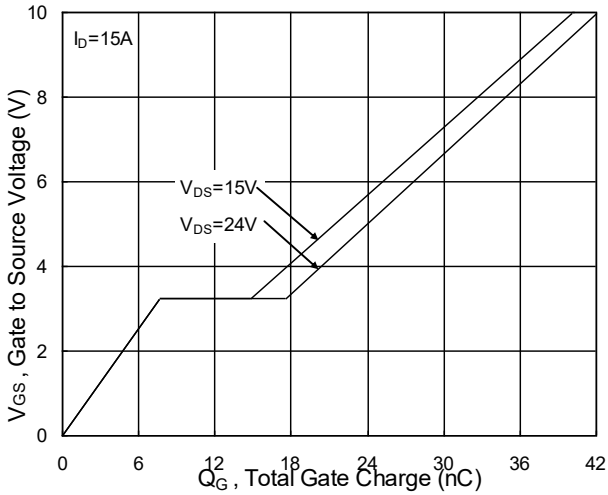



**Fig.4 Gate-Charge Characteristics**

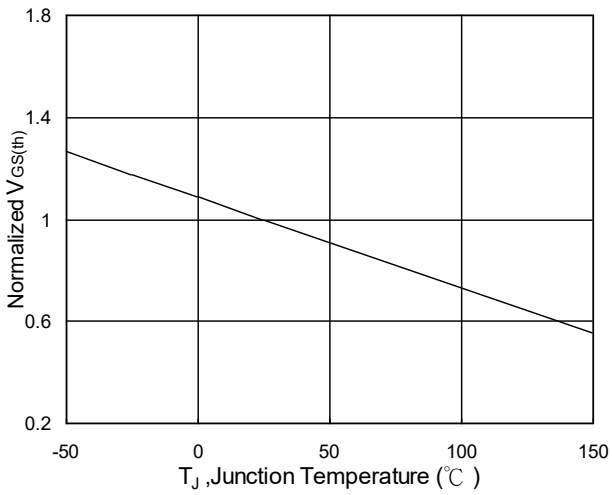



**Fig.5 Normalized $V_{GS(th)}$ vs. $T_J$**

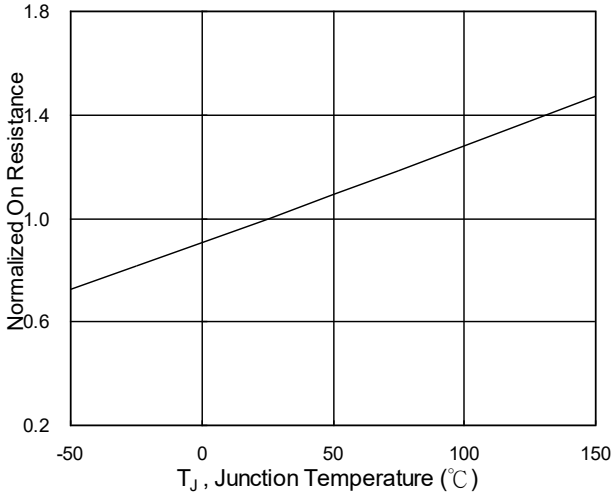



**Fig.6 Normalized $R_{DSON}$ vs. $T_J$**

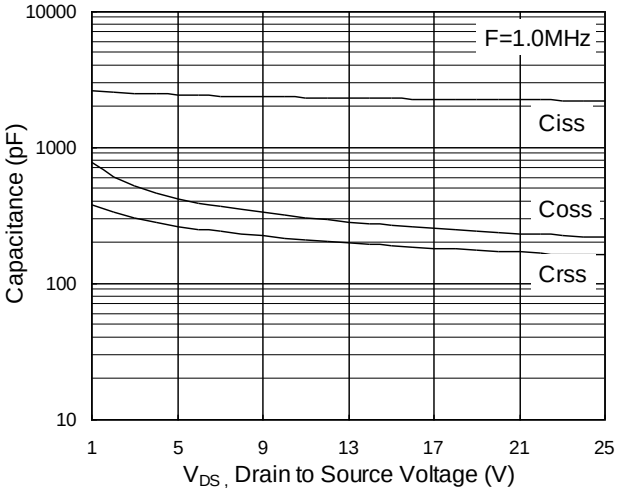



**Fig.7 Capacitance**

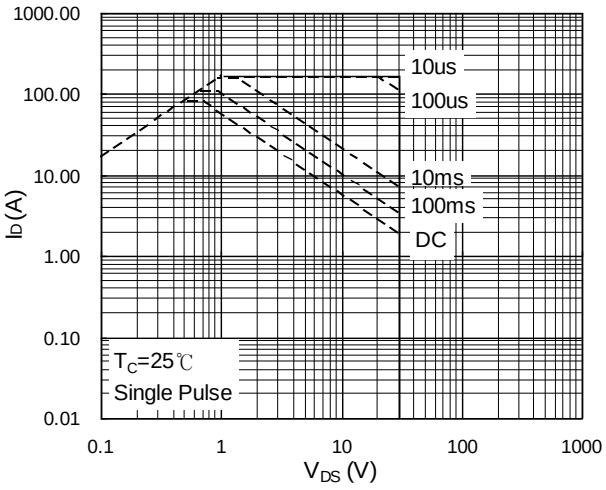



**Fig.8 Safe Operating Area**

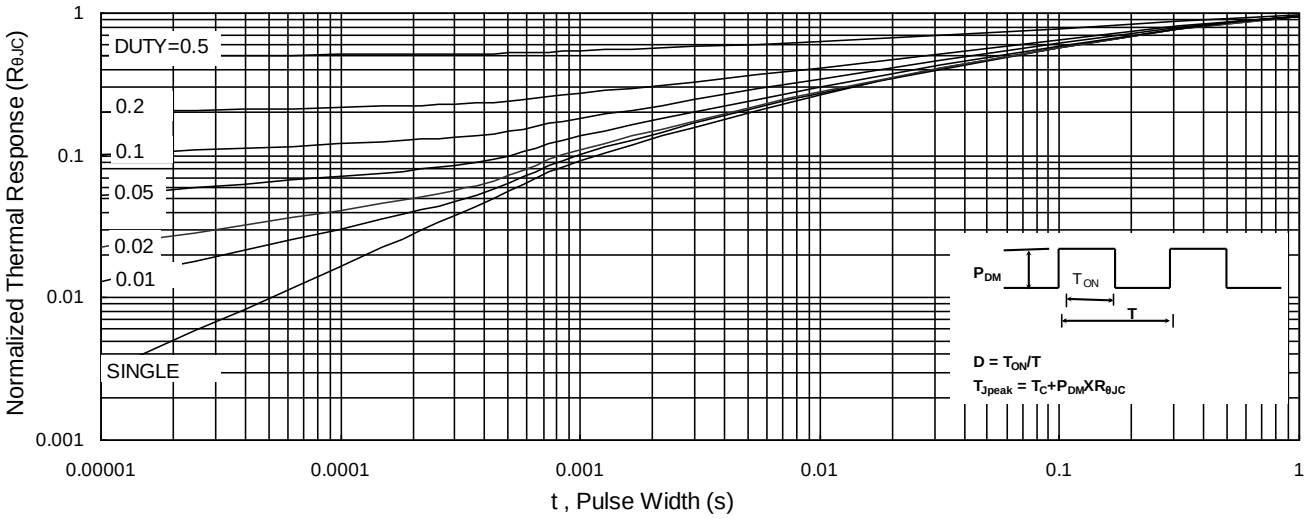



**Fig.9 Normalized Maximum Transient Thermal Impedance**

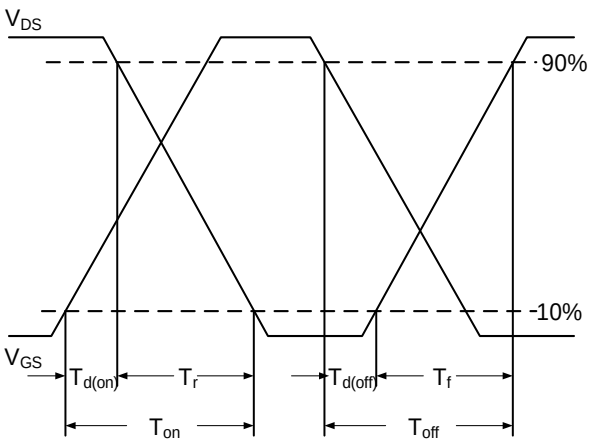



**Fig.10 Switching Time Waveform**

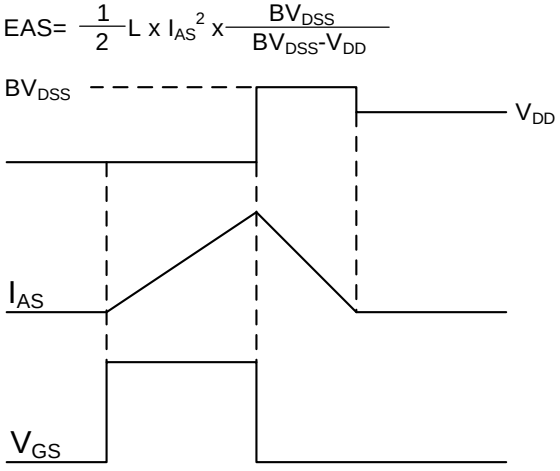
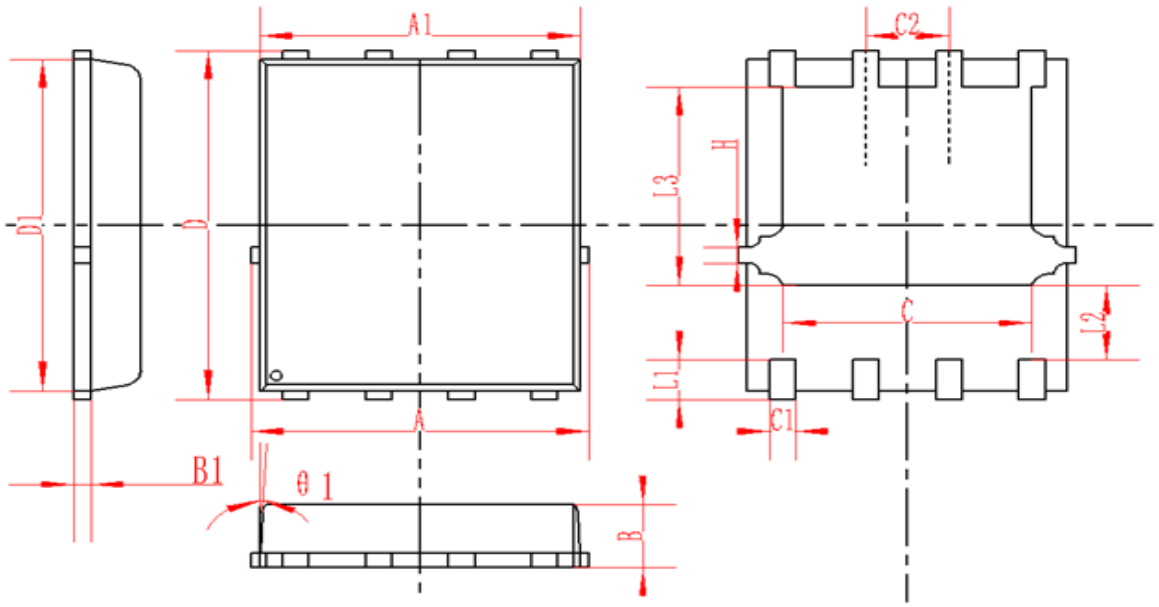



**Fig.11 Unclamped Inductive Switching Waveform**

## DFN5X6-8L Package Information




| SYMBOL | MM | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 4.95 | 5 | 5.05 | 0.195 | 0.197 | 0.199 |
| A1 | 4.82 | 4.9 | 4.98 | 0.190 | 0.193 | 0.196 |
| D | 5.98 | 6 | 6.02 | 0.235 | 0.236 | 0.237 |
| D1 | 5.67 | 5.75 | 5.83 | 0.223 | 0.226 | 0.230 |
| B | 0.9 | 0.95 | 1 | 0.035 | 0.037 | 0.039 |
| B1 | 0.254REF | | | 0.010REF | | |
| C | 3.95 | 4 | 4.05 | 0.156 | 0.157 | 0.159 |
| C1 | 0.35 | 0.4 | 0.45 | 0.014 | 0.016 | 0.018 |
| C2 | 1.27TYP | | | 0.5TYP | | |
| θ1 | 8° | 10° | 12° | 8° | 10° | 12° |
| L1 | 0.63 | 0.64 | 0.65 | 0.025 | 0.025 | 0.026 |
| L2 | 1.2 | 1.3 | 1.4 | 0.047 | 0.051 | 0.055 |
| L3 | 3.415 | 3.42 | 3.425 | 0.134 | 0.135 | 0.135 |
| H | 0.24 | 0.25 | 0.26 | 0.009 | 0.010 | 0.010 |

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