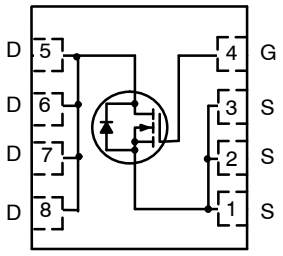
# MOSFET – N-Channel, UltraFET Trench

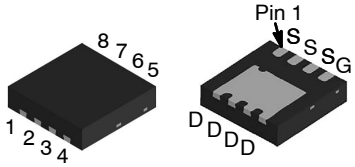
## 220 V, 7.0 A, 366 mΩ

# FDMC2674

| $V_{DS}$ | $R_{DS(ON)}$ MAX | $I_D$ MAX |
|---|---|---|
| 220 V | 366 mΩ @ 10 V | 7.0 A |




**N-CHANNEL MOSFET**




**WDFN8 3.3 × 3.3, 0.65P**
**CASE 511DH**

### General Description

UltraFET device combines characteristics that enable benchmark efficiency in power conversion applications. Optimized for $R_{DS(on)}$, low ESR, low total and Miller gate charge, these devices are ideal for high frequency DC to DC converters.

### Features

- Max $R_{DS(on)}$ = 366 mΩ at $V_{GS}$ = 10 V, $I_D$ = 1.0 A
- Typ $Q_g$ = 12.7 nC at $V_{GS}$ = 10 V
- Low Miller Charge
- Low $Q_{rr}$ Body Diode
- Optimized Efficiency at High Frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)
- Pb−Free, Halide Free and RoHS Compliant

### Applications

- DC−DC Converters and Off−Line UPS
- Distributed Power Architectures

### MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted)

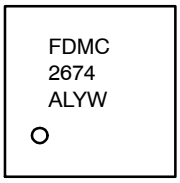
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | 220 | V |
| $V_{GS}$ | Gate to Source Voltage | ±20 | V |
| $I_D$ | Drain Current:<br>Continuous (Silicon limited) $T_C$ = 25°C<br>Continuous (Note 1b) $T_A$ = 25°C<br>Pulsed | <br>7.0<br>1.0<br>13.8 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy (Note 3) | 11 | mJ |
| $P_D$ | Power Dissipation:<br>$T_C$ = 25°C<br>$T_A$ = 25°C (Note 1a) | <br>42<br>2.1 | W |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | −55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case (Note 1) | 3.0 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 60 | |

### MARKING DIAGRAM




FDMC2674 = Specific Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| FDMC2674 | WDFN8 (Pb−Free, Halide Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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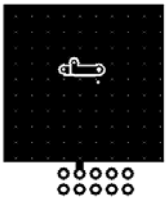
## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 220 | – | – | V |
| $\Delta BV_{DSS}$ /$\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C | – | 248 | – | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 176 V, $V_{GS}$ = 0 V | – | – | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | – | – | ±100 | nA |
| **ON CHARACTERISTICS** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 2 | 3.4 | 4 | V |
| $\Delta V_{GS(th)}$ /$\Delta T_J$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C | – | –10.2 | – | mV/°C |
| $R_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 1.0 A | – | 305 | 366 | mΩ |
| | | $V_{GS}$ = 10 V, $I_D$ = 1.0 A, $T_J$ = 150°C | – | 678 | 814 | |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 100 V, $V_{GS}$ = 0 V, f = 1 MHz | – | 880 | 1180 | pF |
| $C_{oss}$ | Output Capacitance | | – | 70 | 95 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 11 | 20 | pF |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 100 V, $I_D$ = 1.0 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 2.4 Ω | – | 9 | 18 | ns |
| $t_r$ | Rise Time | | – | 13 | 23 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | – | 15 | 27 | ns |
| $t_f$ | Fall Time | | – | 21 | 34 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge at 10 V | $V_{GS}$ = 0 V to 10 V, $V_{DD}$ = 15 V, $I_D$ = 1.0 A | – | 12.7 | 18 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | $V_{DD}$ = 15 V, $I_D$ = 1.0 A | – | 3.8 | – | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | $V_{DD}$ = 15 V, $I_D$ = 1.0 A | – | 2.9 | – | nC |
| **DRAIN-SOURCE DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.2 A (Note 2) | – | 0.8 | 1.5 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 1.0 A, di/dt = 100 A/μs | – | – | 60 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | – | – | 109 | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 $in^2$ oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user’s board design.
   (a) $R_{\theta JA}$ = 60°C/W when mounted on a 1 $in^2$ pad of 2 oz copper, 1.5’ × 1.5’ × 0.062’ thick PCB.
   (b) $R_{\theta JA}$ = 135°C/W when mounted on a minimum pad of 2 oz copper.



a) 60°C/W when mounted on a 1 $in^2$ pad of 2 oz copper.



b) 135°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting $T_J$ = 25°C; N-ch: L = 1 mH, $I_{AS}$ = 4.7 A, $V_{DD}$ = 25 V, $V_{GS}$ = 10 V.

## TYPICAL CHARACTERISTICS

($T_J$ = 25°C unless otherwise noted)

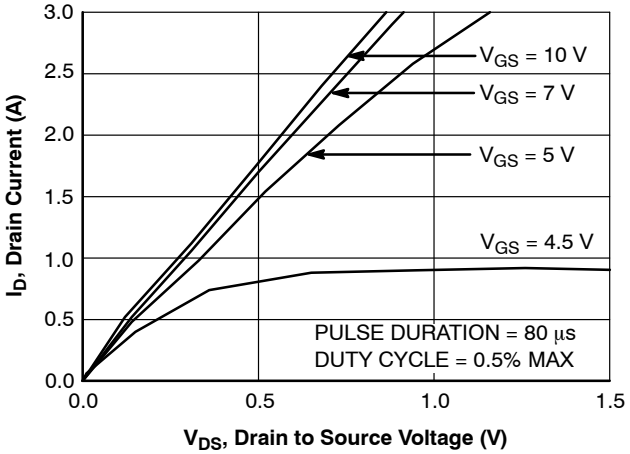



**Figure 1. On−Region Characteristics**

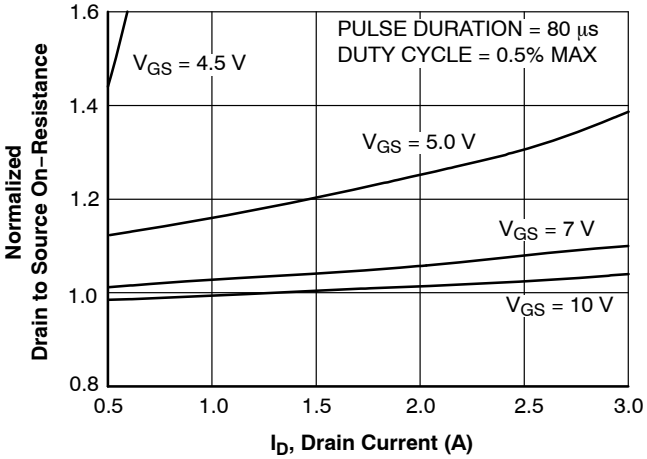



**Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage**

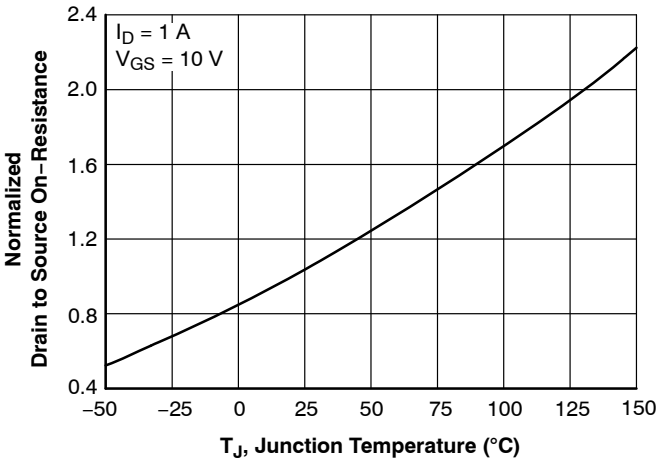



**Figure 3. Normalized On−Resistance vs. Junction Temperature**

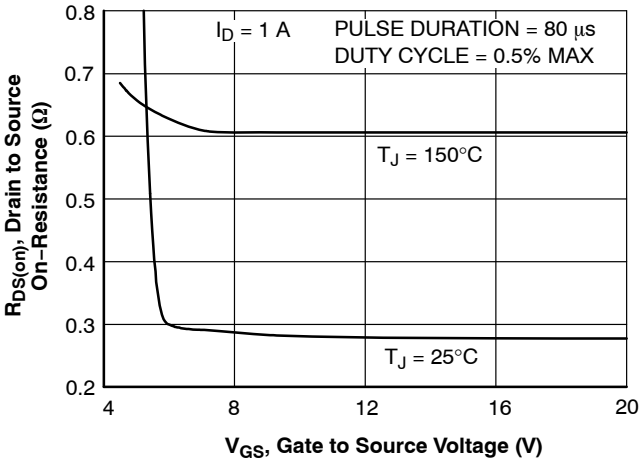



**Figure 4. On−Resistance vs. Gate to Source Voltage**

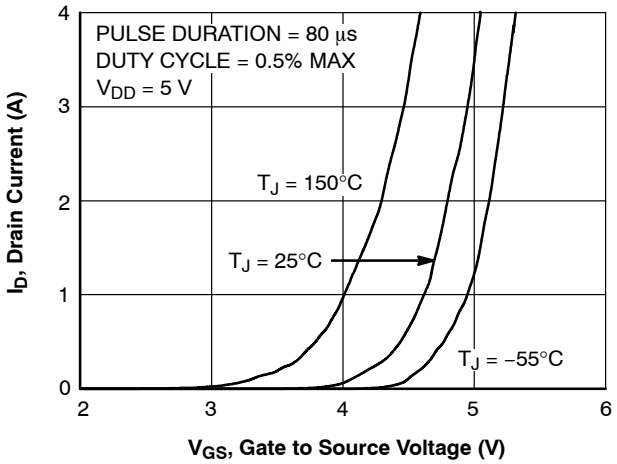



**Figure 5. Transfer Characteristics**

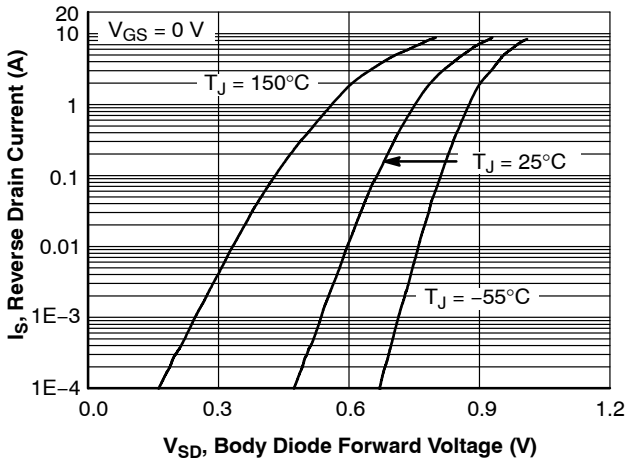



**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

## TYPICAL CHARACTERISTICS (continued)

($T_J$ = 25°C unless otherwise noted)

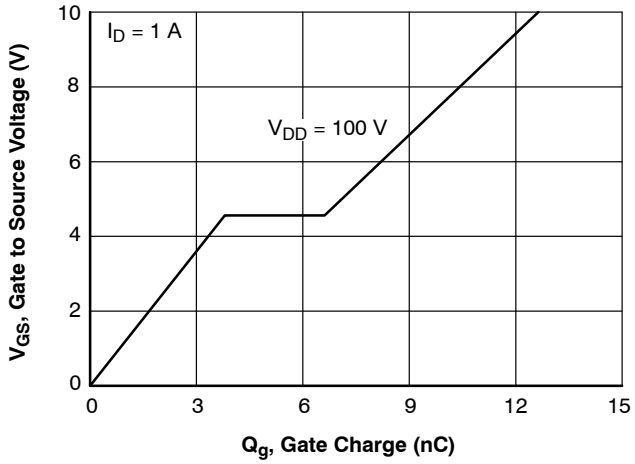



Figure 7. Gate Charge Characteristics

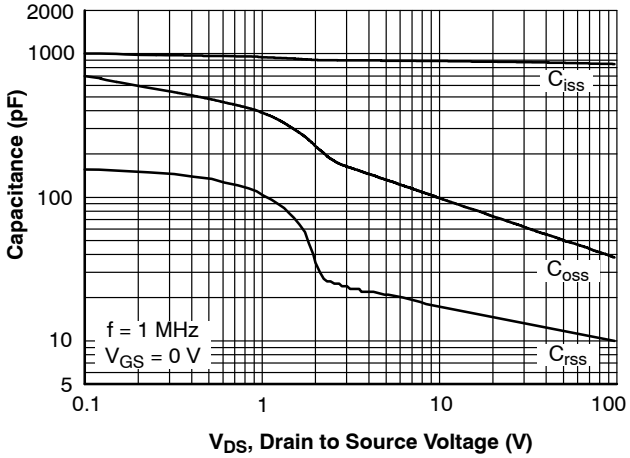



Figure 8. Capacitance vs. Drain to Source Voltage

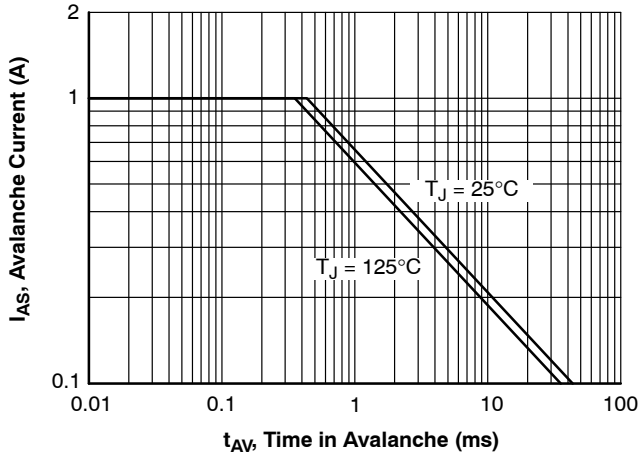



Figure 9. Unclamped Inductive Switching Capability

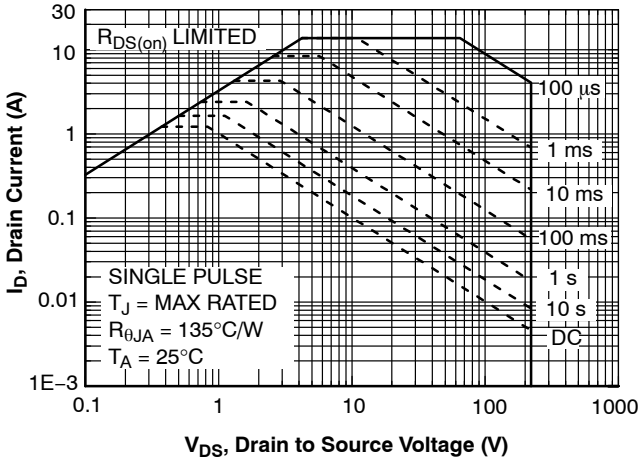



Figure 10. Forward Bias Safe Operating Area

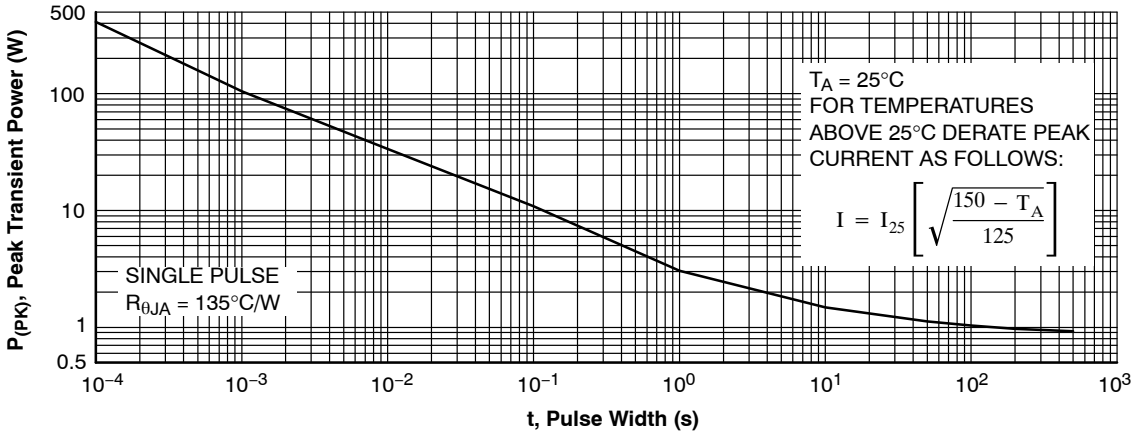



Figure 11. Single Pulse Maximum Power Dissipation

## TYPICAL CHARACTERISTICS (continued)

($T_J$ = 25°C unless otherwise noted)

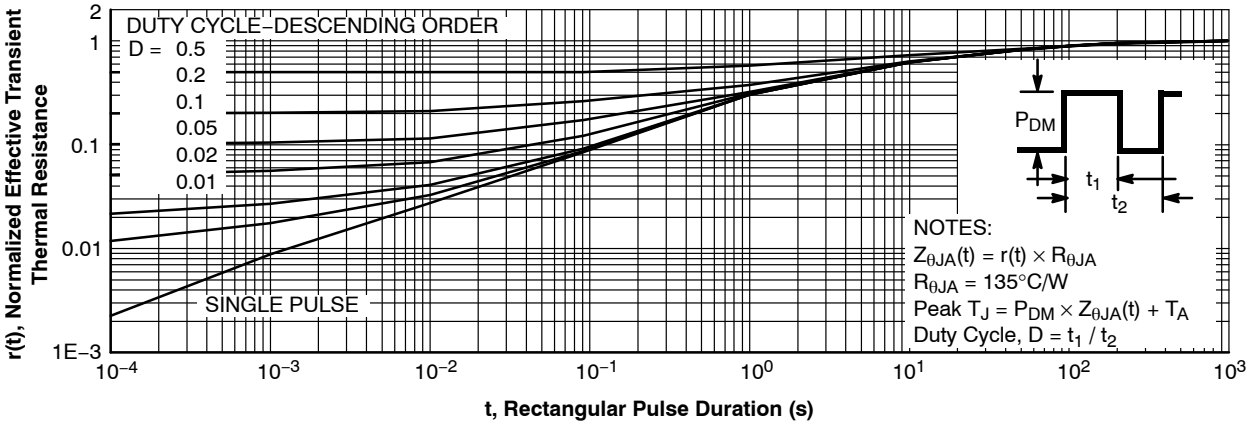
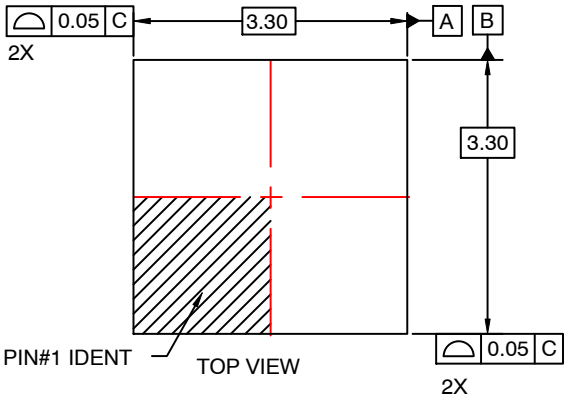
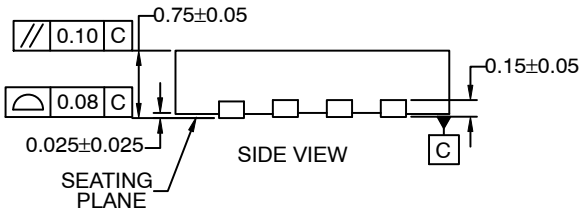


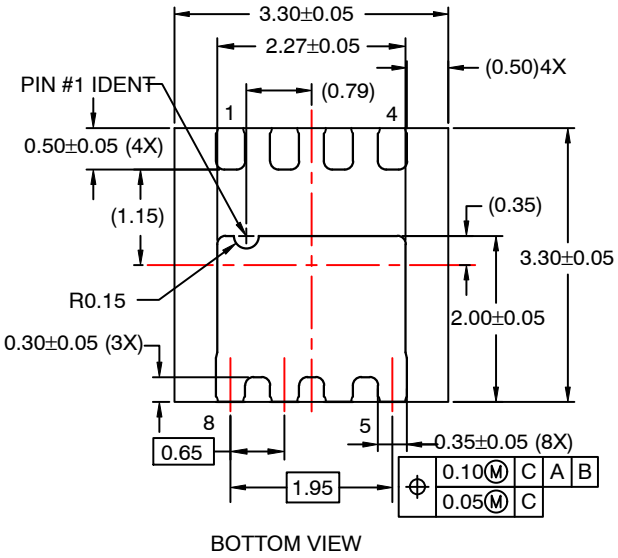

**Figure 12. Transient Thermal Response Curve**

**WDFN8 3.3x3.3, 0.65P**
CASE 511DH
ISSUE O

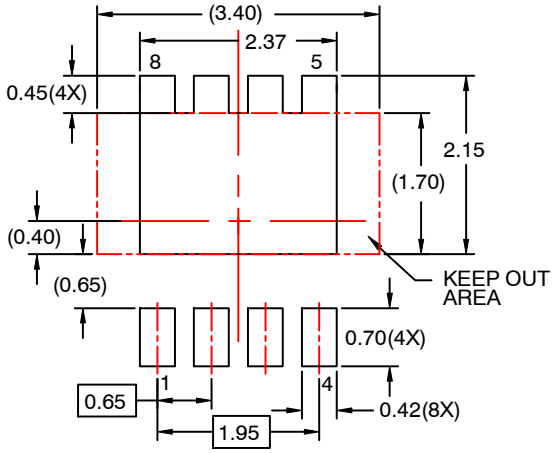
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BOTTOM VIEW




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