# Dual N-Channel Advanced Power MOSFET

## Features

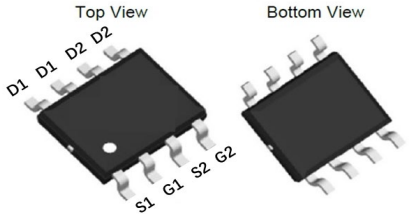
- $V_{DS}$= 60V, $I_D$= 5 A
  $R_{DS(ON)}$ < 30 mΩ @ $V_{GS}$ = 10V
  $R_{DS(ON)}$ < 36 mΩ @ $V_{GS}$ = 4.5V

## General Features

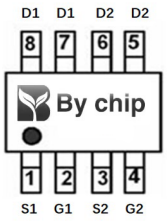
- Advanced Trench Technology
- Provide Excellent RDS(ON) and Low Gate Charge
- Lead Free and Green Available

*100% UIS TESTED!*
*100% ΔVds TESTED!*

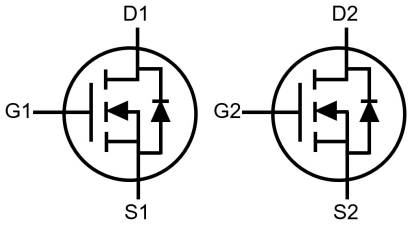
RoHS




SOP-8 (Dual)




Pin Assignment




Schematic diagram

## Absolute Maximum Ratings ($T_A$=25℃ unless otherwise specified)

| Symbol | Parameter | | Max. | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 60 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | V |
| $I_D$ | Continuous Drain Current | $T_A$= 25℃ | 5 | A |
| | | $T_A$= 100℃ | 3.3 | A |
| $I_{DM}$ | Pulsed Drain Current note1 | | 20 | A |
| EAS | Single Pulsed Avalanche Energy note2 | | 20 | mJ |
| $P_D$ | Power Dissipation | $T_A$= 25℃ | 1.74 | W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | | 72 | ℃/W |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | -55 to +150 | ℃ |

## Electrical Characteristics ($T_J$=25℃ unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V, $I_D$=250μA | 60 | - | - | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=60V, $V_{GS}$ = 0V, | - | - | 1.0 | μA |
| $I_{GSS}$ | Gate to Body Leakage Current | $V_{DS}$=0V, $V_{GS}$ = ±20V | - | - | ±100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_D$=250μA | 1.0 | | 2.5 | V |
| $R_{DS(on)}$ | Static Drain-Source on-Resistance note3 | $V_{GS}$=10V, $I_D$=5A | - | | 30 | mΩ |
| | | $V_{GS}$=4.5V, $I_D$=3A | - | | 36 | |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$=25V, $V_{GS}$=0V, f=1.0MHz | - | 853 | - | pF |
| $C_{oss}$ | Output Capacitance | | - | 60 | - | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | - | 29 | - | pF |
| $Q_g$ | Total Gate Charge | $V_{DD}$=30V, $I_D$=2.5A, $V_{GS}$=10V | - | 20 | - | nC |
| $Q_{gs}$ | Gate-Source Charge | | - | 3 | - | nC |
| $Q_{gd}$ | Gate-Drain(“Miller”) Charge | | - | 4.5 | - | nC |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DD}$=30V, $I_D$=5A, $R_{GEN}$=1.8Ω, $V_{GS}$=10V | - | 6 | - | ns |
| $t_r$ | Turn-on Rise Time | | - | 6 | - | ns |
| $t_{d(off)}$ | Turn-off Delay Time | | - | 19 | - | ns |
| $t_f$ | Turn-off Fall Time | | - | 2.5 | - | ns |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain to Source Diode Forward Current | | - | - | 5 | A |
| $I_{SM}$ | Maximum Pulsed Drain to Source Diode Forward Current | | - | - | 20 | A |
| $V_{SD}$ | Drain to Source Diode Forward Voltage | $V_{GS}$=0V, $I_S$=5A | - | - | 1.2 | V |
| trr | Body Diode Reverse Recovery Time | $I_F$=5A, dI/dt=100A/μs | - | 13 | - | ns |
| Qrr | Body Diode Reverse Recovery Charge | | - | 9 | - | nC |

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition :Starting $T_J$=25℃,$V_{DD}$=30V,$V_{GS}$=10V,L=0.5mH,Rg=25Ω,$I_{AS}$=9A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

## Typical Performance Characteristics

**Figure 1:** Output Characteristics

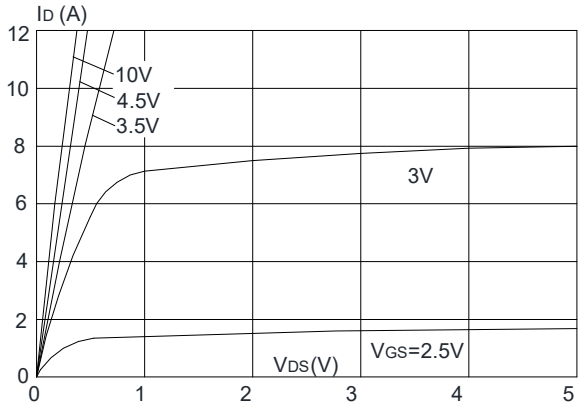



**Figure 2:** Typical Transfer Characteristics

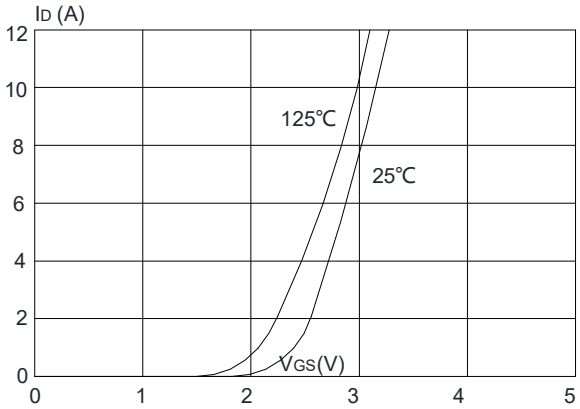



**Figure 3:** On-resistance vs. Drain Current

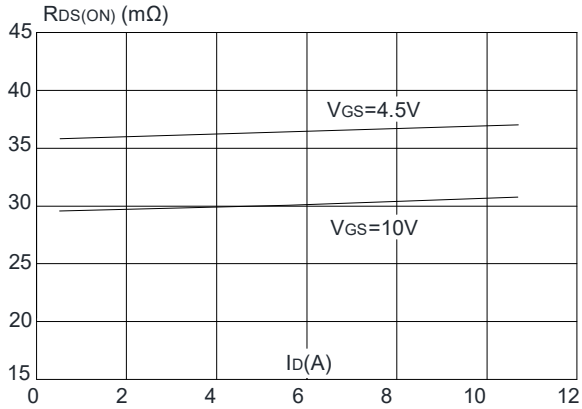



**Figure 4:** Body Diode Characteristics

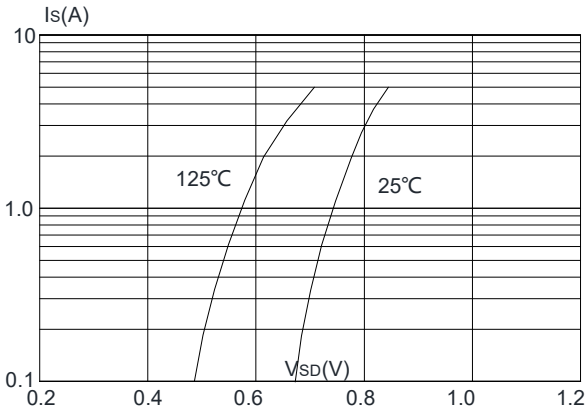



**Figure 5:** Gate Charge Characteristics

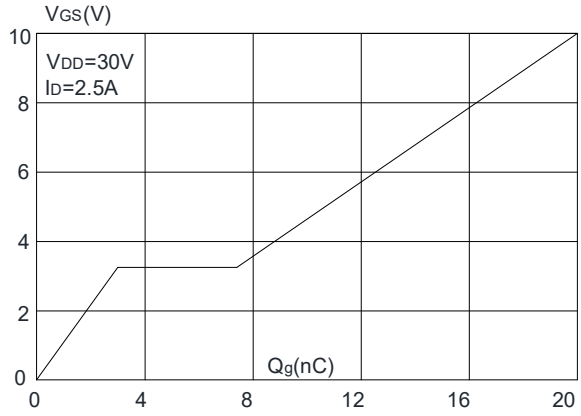



**Figure 6:** Capacitance Characteristics

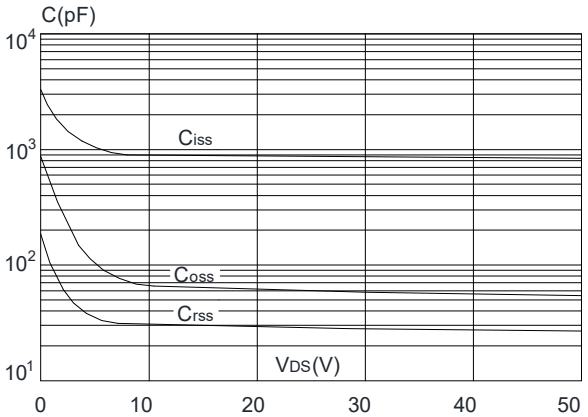


**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature

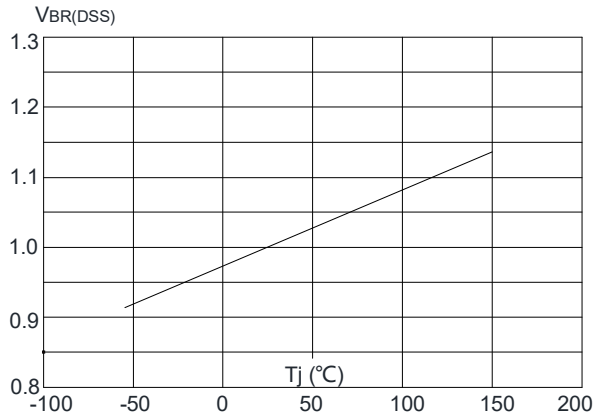



**Figure 8:** Normalized on Resistance vs. Junction Temperature

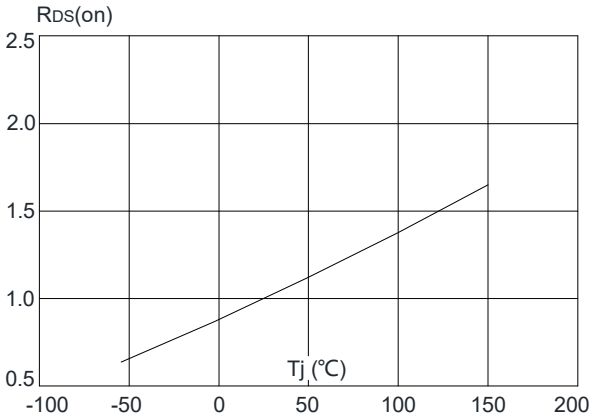



**Figure 9:** Maximum Safe Operating Area

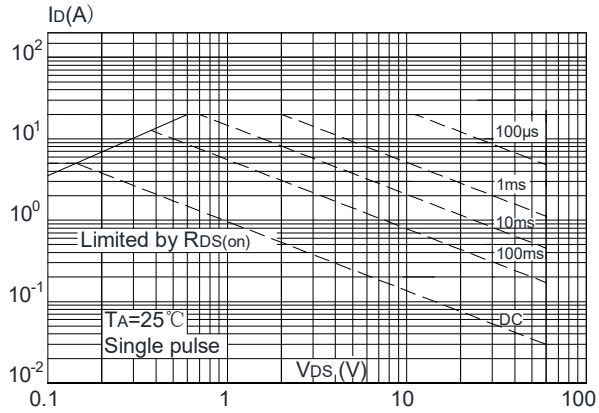



**Figure 10:** Maximum Continuous Drain Current vs. Ambient Temperature

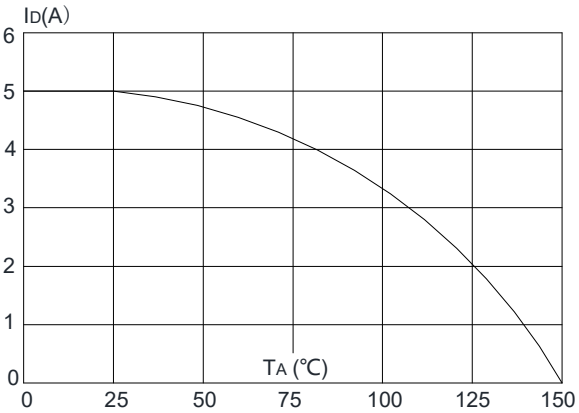
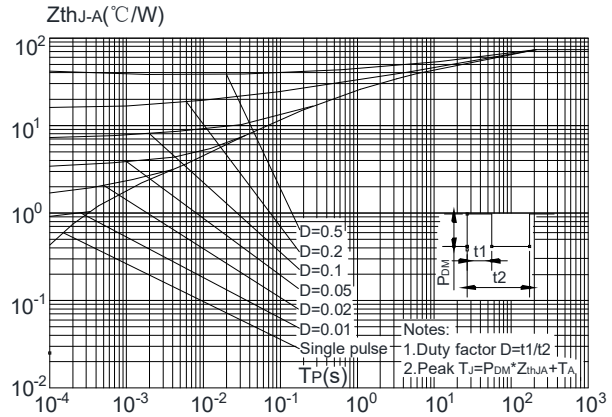



**Figure 11:** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



## Test Circuit

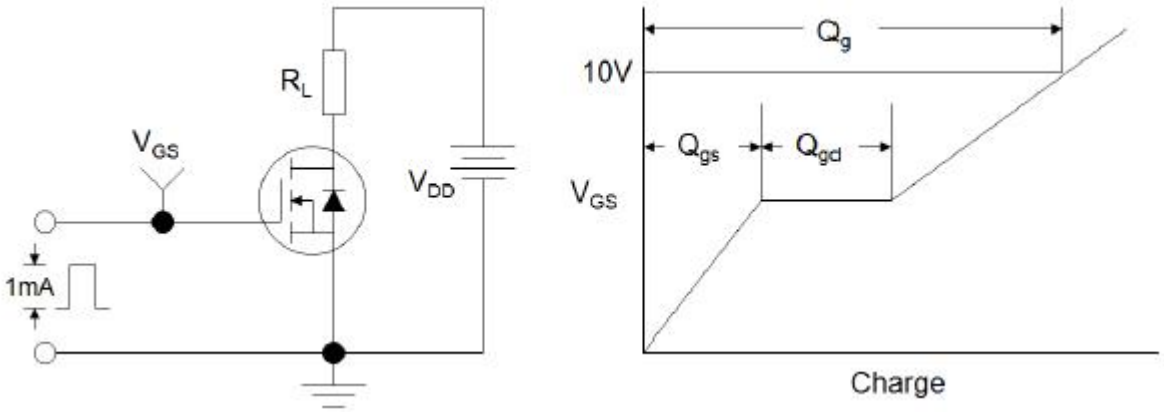



**Figure1:Gate Charge Test Circuit & Waveform**

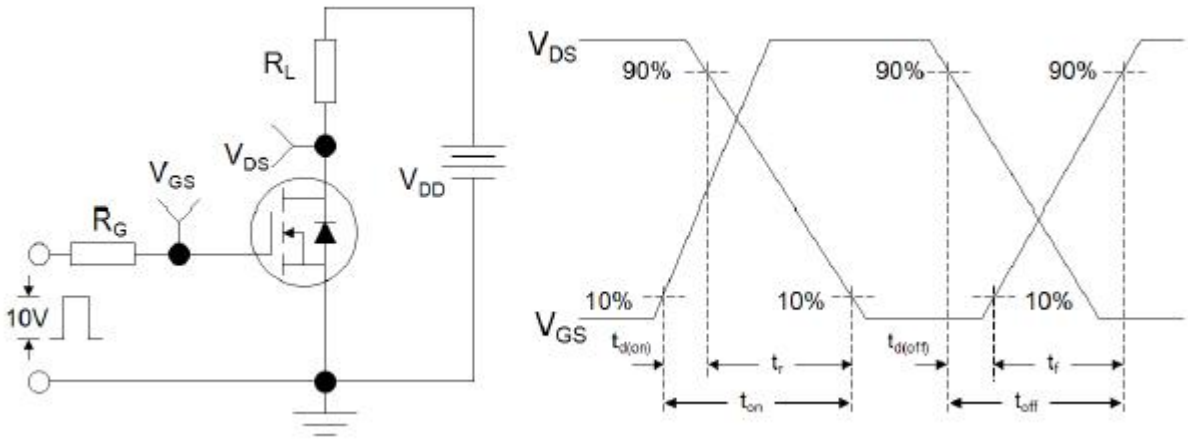



**Figure 2: Resistive Switching Test Circuit & Waveforms**

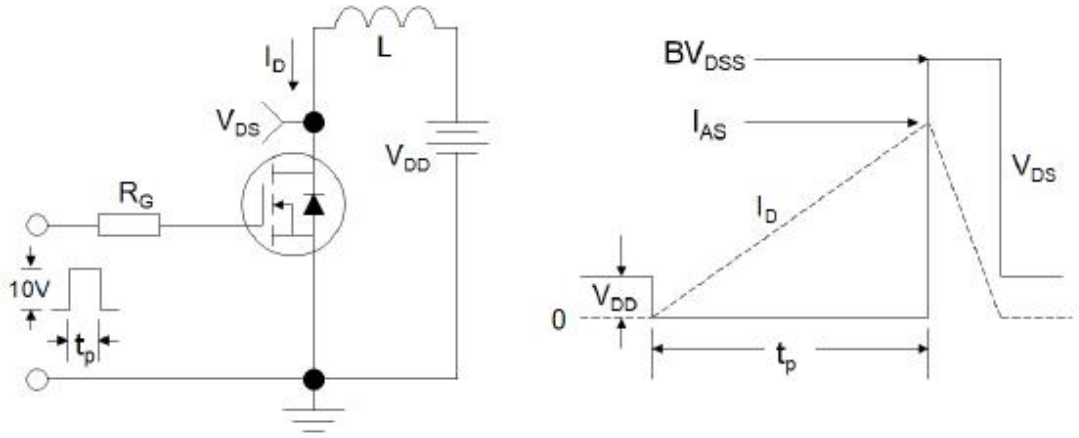



**Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms**