bq25071-Q1 1-A, Automotive Qualified, Single-Cell LiFePO$_4$ Linear Battery Charger with 50-mA LDO

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C5
- Single Cell LiFePO$_4$ Charging Algorithm
- 30-V Input Rating, With 10.5-V Overvoltage Protection (OVP)
- 50-mA Integrated Low Dropout Linear Regulator (LDO)
- Programmable Charge Current Through ISET and EN Terminals
- Thermal Regulation and Protection
- Soft-Start Feature to Reduce Inrush Current
- Battery NTC Monitoring
- Charging Status Indication
- 10-Pin SON (2mm x 3mm) Package with Wettable Flanks

2 Applications

- E-call for Cars
- Automotive Telematics
- Vehicle GPS Tracking
- Car Network Video Recorder
- Smart Key
- Automotive Entertainment backup battery

3 Description

The bq25071-Q1 is a highly integrated, linear, LiFePO$_4$ battery charger targeted at space-limited automotive applications. It accepts power from either a USB port or AC adapter and charges a single-cell LiFePO$_4$ battery with up to 1 A of charge current. The 30-V input rating supports low-cost unregulated adapters.

The bq25071-Q1 has a single power output that simultaneously charges the battery and powers the system. The input current is programmable from 100 mA up to 1 A using the ISET input or configurable for USB500. There is also a 4.9 V ±10% 50 mA LDO integrated into the IC for supplying low power external circuitry.

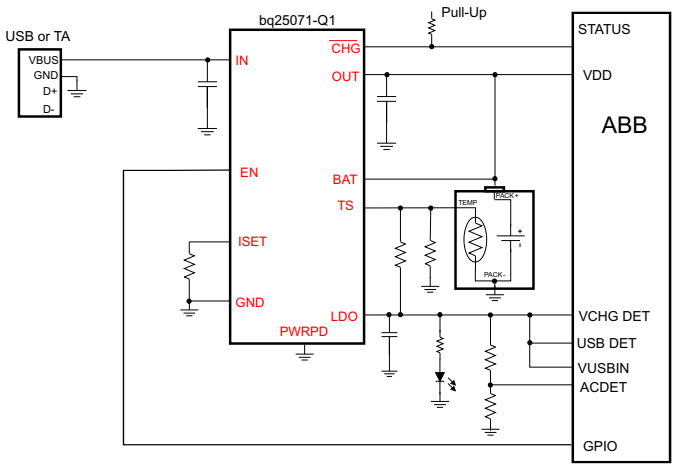
The LiFePO$_4$ charging algorithm removes the current taper typically seen as part of the constant voltage mode control used in Li-Ion battery charge cycles which reduces charge time significantly. Instead, the battery is fast charged to the overcharge voltage and then allowed to relax to a lower float charge voltage threshold. The charger integrates the power stage with the charge current and voltage sense to achieve a high level of accuracy in the current and voltage regulation loops. An internal control loop monitors the IC junction temperature through the charge cycle and reduces the charge current if an internal temperature threshold is exceeded.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq25071-Q1	WSON (10)	2.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Application Schematic



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4 Revision History

DATE	REVISION	NOTES
April 2016	*	Initial release.

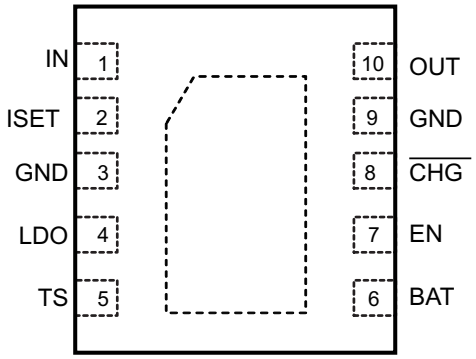
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5 Device Comparison Table

PART NUMBER	$V_{BAT(OVCH)}$	$V_{BAT(FLOAT)}$	$V_{(OVP)}$	$V_{(LDO)}$
bq25071QWDQCRQ1	3.7 V	3.5 V	10.5 V	4.9 V
bq25071QWDQCTQ1	3.7 V	3.5 V	10.5 V	4.9 V

6 Pin Configuration and Functions

DQC Package
10-Pin WSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN	1	I	Input power supply. IN is connected to the external DC supply (AC adapter or USB port). Bypass IN to GND with at least a 0.1 µF ceramic capacitor.
ISET	2	O	Input current programming bias pin. Connect a resistor from ISET to GND to program the input current limit when the user programmable mode is selected by grounding the EN pin. The resistor range is between 1 kΩ and 10 kΩ to set the current between 100 mA and 1 A.
GND	3, 9	–	Ground pin. Connect to the thermal pad and the ground plane of the circuit.
LDO	4	O	LDO output. LDO is regulated to 4.9V and drives up to 50 mA. Bypass LDO to GND with a 0.1 µF ceramic capacitor. LDO is enabled when $V_{(UVLO)} < V_{IN} < V_{(OVP)}$.
TS	5	I	Battery pack NTC monitoring input. Connect a resistor divider from LDO to GND with TS connected to the center tap to set the charge temperature window. The battery pack NTC is connected in parallel with the bottom resistor of the divider. See the *Detailed Design Procedure* section for details on the selecting the proper component values.
BAT	6	I	BAT is the sense input for the battery voltage. Connect BAT and OUT to the battery.
EN	7	I	Enable input. Drive EN high to disable the IC. Connect EN to GND to place the bq25071-Q1Q in the user programmable mode using the ISET input where the input current is programmed. Leave EN floating to place the bq25071-Q1Q in USB500 mode. See the *Input Current Limit Control (EN)* section for details on using the EN interface.
$\overline{CHG}$	8	O	Charge status indicator open-drain output. $\overline{CHG}$ is pulled low while the device is charging the battery. $\overline{CHG}$ goes high impedance when the battery is fully charged.
OUT	10	O	System output connection. Bypass the OUT to GND with a 1 µF ceramic capacitor. Connect OUT and BAT together.
Thermal Pad	Pad	–	There is an internal electrical connection between the exposed thermal pad and the GND pin of the device. The thermal pad must be connected to the same potential as the GND pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. GND pin must be connected to ground at all times.

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7 Specifications

7.1 Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input Voltage	IN (with respect to GND)	–0.3	30	V
	EN, TS (with respect to GND)	–0.3	7	V
Output Voltage	BAT, OUT, LDO, $\overline{CHG}$, ISET (with respect to GND)	–0.3	7	V
Input Current (Continuous)	IN		1.2	A
Output Current (Continuous)	BAT		1.2	A
Output Current (Continuous)	LDO		100	mA
Output Sink Current	$\overline{CHG}$		5	mA
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{STG}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground pin unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per aec q100-002 (1)	±3000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

		MIN	MAX	UNITS
V_{IN}	IN operating voltage	3.75 (1)	8	V
I_{IN}	Input current, IN		1	A
I_{OUT}	Output Current in charge mode, OUT		1	A
T_J	Junction Temperature	-40	125	°C

(1) Charge current may be limited at low input voltages due to the dropout of the device.

7.4 Thermal Information

THERMAL METRIC (1)		bq25071-Q1 DQC (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	22.8	
ψ_{JT}	Junction-to-top characterization parameter	1.5	
ψ_{JB}	Junction-to-board characterization parameter	22.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.5	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

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7.5 Electrical Characteristics

Over junction temperature range–40°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT						
$V_{(UVLO)}$	Under-voltage lock-out	V_{IN}: 0 V → 4 V	3.15	3.30	3.55	V
$V_{HYS(UVLO)}$	Hysteresis on $V_{(UVLO)}$	V_{IN}: 4 V → 0 V		300		mV
$V_{IN(SLP)}$	Valid input source threshold $V_{IN(SLP)}$ above V_{BAT}	Input power good if V_{IN} > V_{BAT} + $V_{IN(SLP)}$ $V_{(BAT)}$ = 3.6 V, V_{IN}: 3.5 V → 4 V	30	75	150	mV
		Input power good if V_{IN} > V_{BAT} + $V_{IN(SLP)}$ $V_{(BAT)}$ = 3.6 V, V_{IN}: 4 V → 3.5 V	24	55	95	mV
$V_{HYS(INSLP)}$	Hysteresis on $V_{IN(SLP)}$	$V_{(BAT)}$ = 3.6 V, V_{IN}: 4 V → 3.5 V		32		mV
V_{OVP}	Input over-voltage protection threshold	V_{IN}: 5 V → 11 V	10.2	10.5	10.8	V
$V_{HYS(OVP)}$	Hysteresis on OVP	V_{IN}: 11 V → 5 V		100		mV
QUIESCENT CURRENT						
$I_{BAT(PDWN)}$	Battery current into BAT, No input connected	V_{IN} = 0 V (1), $V_{(\overline{CHG})}$ = Low			6	µA
$I_{IN(STDBY)}$	Standby current into IN pin	EN = HI, V_{IN} = 5.5V			0.25	mA
		EN = HI, V_{IN} ≤ $V_{(OVP)}$			0.5	
		EN = HI, V_{IN} > $V_{(OVP)}$			2	
BATTERY CHARGER FAST-CHARGE						
$V_{BAT(REG)}$	Battery charge regulation voltage	T_A = -40°C to 125°C, I_{OUT} = 50 mA, V_{IN} = 5 V	3.455	3.5	3.545	V
		T_A = 25°C, V_{IN} = 5 V, I_{OUT} = 50 mA	3.455	3.5	3.539	
$V_{BAT(OVCH)}$	Battery overcharge voltage threshold		3.55	3.7	3.81	V
$I_{IN(RANGE)}$	User programmable input current limit range	$R_{(ISET)}$ = 1 kΩ to 1 0kΩ, EN = V_{SS}	100		1000	mA
$I_{IN(LIM)}$	Input current limit, or fast-charge current	EN = FLOAT	435	467	500	mA
		EN = V_{SS}	K_{ISET}/R_{ISET}			
K_{ISET}	Fast charge current factor T_A ≤ 85°C	$R_{(ISET)}$ = 1 kΩ to 10 kΩ, EN = V_{SS} , 4.35 V < V_{IN} ≤ 8 V	860	1000	1130	AΩ
		$R_{(ISET)}$ = 1 kΩ to 10 kΩ, EN = V_{SS} , 3.75 V < V_{IN} ≤ 4.35 V	815	1000	1185	AΩ
$V_{DO(IN-OUT)}$	V_{IN} – V_{OUT}	V_{IN} = 4.2 V, I_{OUT} = 0.75 A		500	900	mV
ISET SHORT CIRCUIT PROTECTION						
$R_{ISET(MAX)}$	Highest resistor value considered a short fault	$R_{(ISET)}$: 900 Ω → 300 Ω, I_{OUT} latches off, Cycle power to reset, Fault range > 1.10 A			720	Ω
$I_{OUT(CL)}$	Maximum OUT current limit regulation (Clamp)		1		2	A
PRE-CHARGE AND CHARGE DONE						
$V_{(LOWV)}$	Pre-charge to fast-charge transition threshold		0.5	0.7	0.9	V
$I_{(PRECHARGE)}$	Precharge current to BAT during precharge mode	$V_{(BAT)}$ = 0 V to 0.7 V	41.5	45	49.5	mA
RECHARGE OR REFRESH						
$V_{(RCH)}$	Recharge detection threshold hysteresis	$V_{(BAT)}$ falling	150	200	350	mV
LDO						
$V_{(LDO)}$	LDO Output Voltage	V_{IN} = 5 V to 8 V, $I_{(LDO)}$ = 0 mA to 50 mA	4.7	4.9	5.1	V
$I_{(LDO)}$	Maximum LDO Output Current		60			mA
$V_{(DO)}$	Dropout Voltage	V_{IN} = 4.5V, $I_{(LDO)}$ = 50 mA		200	350	mV

(1) Force $V_{(CHG)}$

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Electrical Characteristics (continued)

Over junction temperature range–40°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC LEVELS ON EN						
V_{IL}	Logic low input voltage				0.4	V
V_{IH}	Logic high input voltage		1.4			V
$V_{(FLT)}$	Logic FLOAT input voltage		600	850	1100	mV
$I_{(FLTlkg)}$	Maximum leakage sink or source current to keep in FLOAT				1	µA
$I_{EN(DRIVE)}$	Minimal drive current from an external device for Low or High		8			µA
BATTERY-PACK NTC MONITOR (TS)						
$V_{(COLD)}$	TS Cold Threshold	$V_{(TS)}$ Rising	23.6	25	25.8	$\%V_{LDO}$
$V_{(CUTOFF)}$	TS Cold Cutoff Threshold	$V_{(TS)}$ Falling		1		$\%V_{LDO}$
$V_{(HOT)}$	TS Hot Threshold	$V_{(TS)}$ Falling	12	12.5	13.2	$\%V_{LDO}$
$V_{HOT(HYS)}$	TS Hot Cutoff Threshold	$V_{(TS)}$ Rising		1		$\%V_{LDO}$
$\overline{CHG}$ OUTPUT						
V_{OL}	Output LOW voltage	$I_{(SINK)}$ = 1 mA			0.45	V
I_{IH}	Leakage current	$\overline{CHG}$ = 5 V			1	µA
THERMAL REGULATION						
$T_{J(REG)}$	Temperature Regulation Limit	T_J rising		125		°C
$T_{J(OFF)}$	Thermal shutdown temperature	T_J rising		155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis	T_J falling		20		°C

7.6 Timing Requirements

			MIN	TYP	MAX	UNIT
INPUT						
$t_{BLK(OVP)}$	Input overvoltage blanking time			100		µs
$t_{REC(OVP)}$	Input overvoltage recovery time	Time measured from V_{IN}: 11 V → 5 V 1 µs fall-time to LDO = HI, $V_{(BAT)}$ = 3.5 V		100		µs
$t_{DGL(NO-IN)}$	Delay time, input power loss to charger turn-off	Time measured from V_{IN}: 5 V → 2.5 V 1 µs fall-time		32		ms
ISET SHORT CIRCUIT PROTECTION						
$t_{DGL(SHORT)}$	Deglitch time transition from $I_{(SET)}$ short to I_{OUT} disable	Clear fault by cycling $V_{(BUS)}$ or EN		1.5		ms
PRE-CHARGE AND CHARGE DONE						
$t_{DGL1(LOWV)}$	Deglitch time on pre-charge to fast-charge transition			25		ms
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to pre-charge transition			25		ms
RECHARGE OR REFRESH						
$t_{DGL(RCH)}$	Deglitch time, recharge threshold detected	$V_{(BAT)}$ falling to New Charge Cycle		25		ms
BATTERY-PACK NTC MONITOR (TS)						
$t_{dgl(TS)}$	Deglitch for TS Fault	Fault detected on TS to stop charge		25		ms

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7.7 Typical Characteristics

V_{IN} = 5 V, V_{BAT} = 3.2 V, $I_{\overline{(CHG)}}$ = 280 mA, Typical Application Circuit

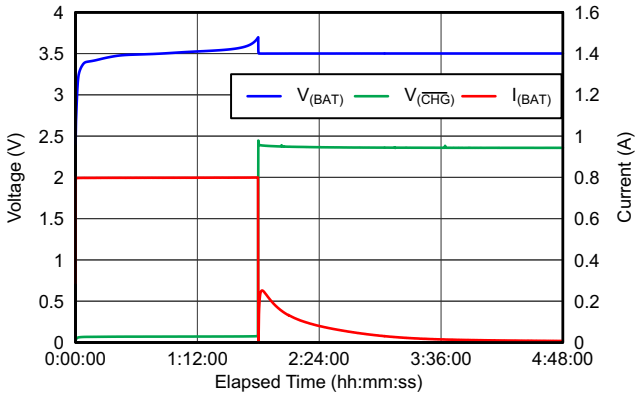
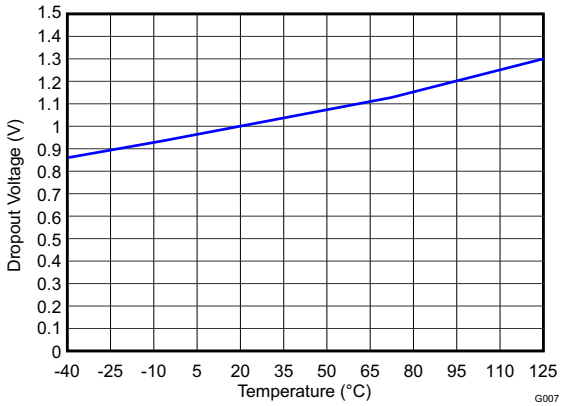


Figure 1. Voltage and Current vs Elapsed Time



V_{IN} = 4.5 V I_{OUT} = 1 A

T_A = –40°C to 125°C

Figure 2. Dropout Voltage vs Temperature

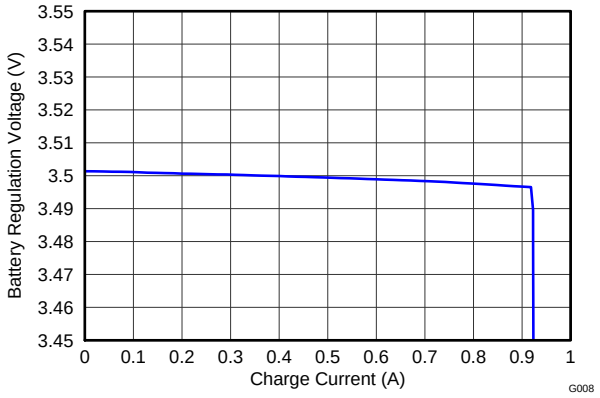
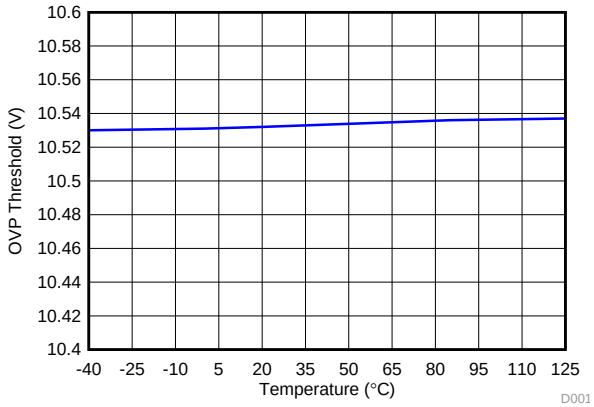


Figure 3. Battery Regulation Voltage vs Charge Current



T_A = –40°C to 125°C

Figure 4. OVP Threshold vs Temperature

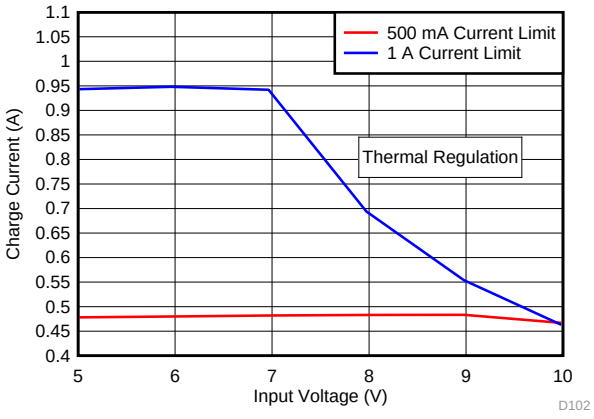
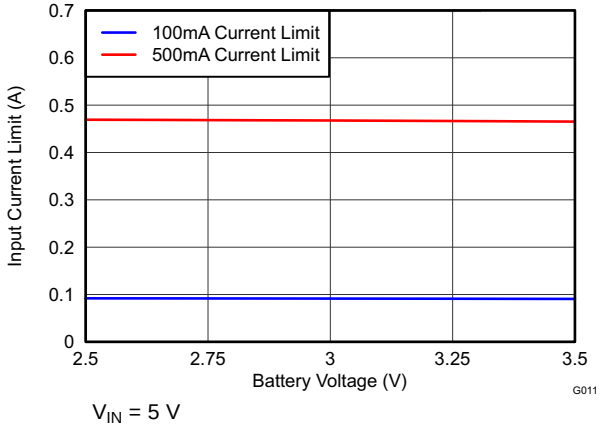


Figure 5. Charge Current vs Input Voltage



V_{IN} = 5 V

Figure 6. Input Current Limit vs Battery Voltage

7.8 Typical Characteristics

V_{BAT} = 3.2 V, $I_{\overline{(CHG)}}$ = 318 mA, Typical Application Circuit

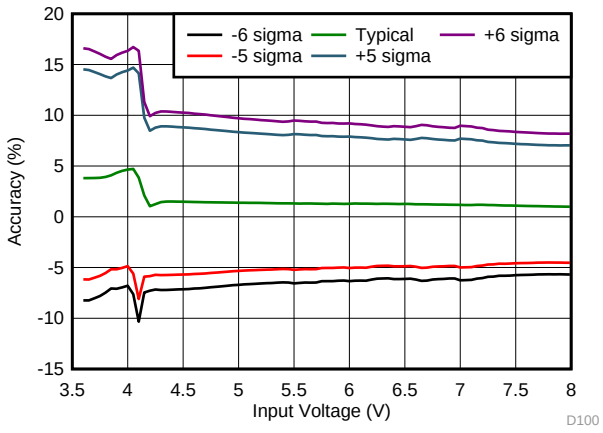


Figure 7. Charge Current Accuracy vs Input Voltage

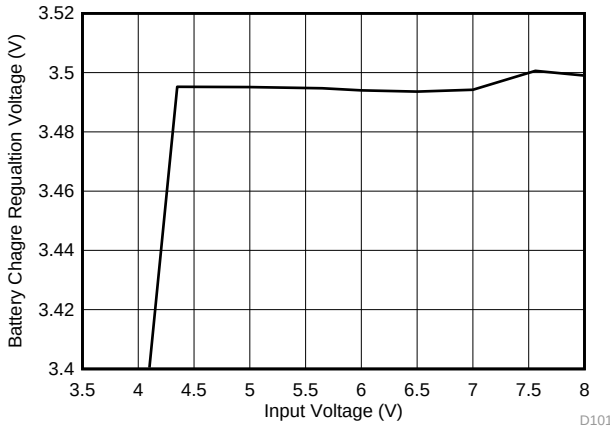


Figure 8. Input Voltage vs Battery Charge Regulation Voltage

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8 Detailed Description

8.1 Overview

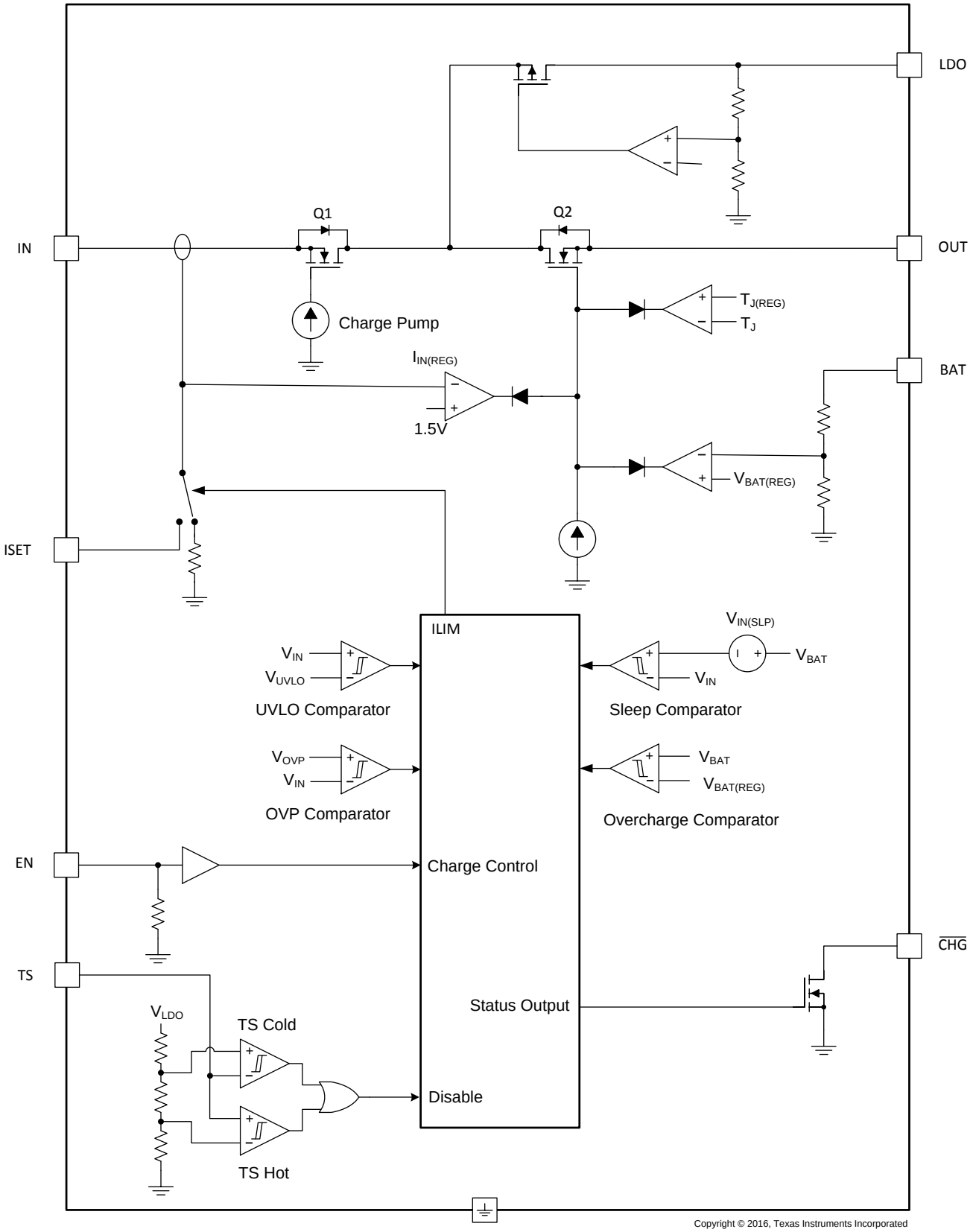
The bq25071-Q1 is a highly integrated, automotive qualified, linear, $LiFePO_4$ battery charger targeted at space-limited automotive applications. It accepts power from either a USB port or AC adapter and charges a single-cell $LiFePO_4$ battery with up to 1 A of charge current. The 30 V input rating with 10.5 V input overvoltage protection supports low-cost unregulated adapters.

The bq25071-Q1 has a single power output that simultaneously charges the battery and powers the system. The input current is programmable from 100 mA up to 1 A using the ISET input or configurable for USB500. There is also a 4.9 V ±10% 50 mA LDO is integrated into the IC for supplying low power external circuitry.

The $LiFePO_4$ charging algorithm removes the constant voltage mode control typically used in Li-Ion battery charge cycles which reduces charge time significantly. Instead, the battery is fast charged to the overcharge voltage and then allowed to relax to a lower float charge voltage threshold. The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops, and charge status display. During the charge cycle, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

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8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Input Overvoltage Protection

The bq25071-Q1 contains an input overvoltage protection circuit that disables the LDO output and charging when the input voltage rises above $V_{(OVP)}$. This prevents damage from faulty adapters. The OVP circuitry contains an 100 µs blanking period that prevents ringing on the input from line transients from tripping the OVP circuitry falsely. If an adapter with an output greater than $V_{(OVP)}$ is plugged in, the IC completes soft-start power up and then shuts down if the voltage remains above $V_{(OVP)}$ after 100 µs. The LDO remains off and charging remains disabled until the input voltage falls below $V_{(OVP)}$.

8.3.2 Undervoltage Lockout (UVLO)

The bq25071-Q1 remains in power down mode when the input voltage is below the undervoltage lockout threshold ($V_{(UVLO)}$). During this mode, the control input (EN) is ignored. The LDO, the charge FET connected between IN and OUT are off and the status output ($\overline{CHG}$) is high impedance. Once the input voltage rises above $V_{(UVLO)}$, the internal circuitry is turned on and the normal operating procedures are followed.

8.3.3 External NTC Monitoring (TS)

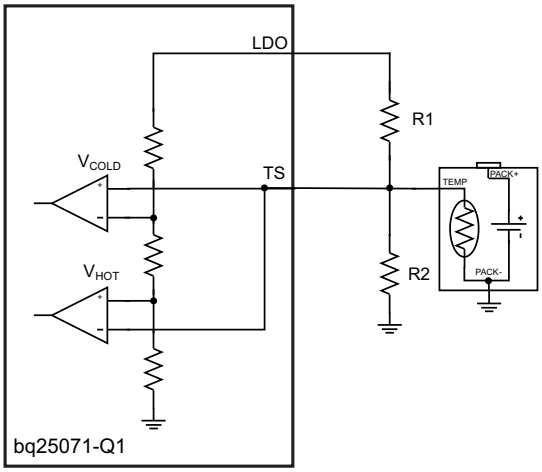
The bq25071-Q1 features a flexible, voltage based external battery pack temperature monitoring input. The TS input connects to the NTC thermistor in the battery pack to monitor battery temperature and prevent dangerous over-temperature conditions. During charging, the voltage at TS is continuously monitored. If the voltage at the TS pin is outside of the operating range ($V_{(HOT)}$ to $V_{(COLD)}$ for longer than the built in 25 ms deglitch time, charging is suspended. When the voltage measured at TS returns to within the operation window, charging resumes. When a battery pack temperature fault occurs charging is suspended, but the $\overline{CHG}$ output remains low and continues to indicate charging.

The temperature thresholds are programmed using a resistor divider from LDO to GND with the NTC thermistor connected to the center tap from TS to GND. See Figure 9 for the circuit example. The value of R1 and R2 are calculated using the following equations:

$$R1 = \frac{-R2 \times RHOT \times (0.125 - 1)}{0.125 \times (R2 + RHOT)} \quad (1)$$

$$R2 = \frac{-RHOT \times RCOLD \times (0.125 - 0.250)}{RHOT \times 0.250 \times (0.125 - 1) + RCOLD \times 0.125 \times (1 - 0.250)} \quad (2)$$

RHOT is the expected thermistor resistance at the programmed hot threshold; RCOLD is the expected thermistor resistance at the programmed cold threshold.



For applications that do not require the TS monitoring function, set R1 = 490 kΩ and R2 = 100 kΩ to set the TS voltage at a valid level and maintain charging.

Figure 9. NTC Monitoring Function

Feature Description (continued)

8.3.4 50-mA LDO (LDO)

The LDO output of the bq25071-Q1 is a low dropout linear regulator (LDO) that supplies up to 50 mA while regulating to $V_{(LDO)}$. The LDO is active whenever the input voltage is above $V_{(UVLO)}$ and below $V_{(OVP)}$. It is not affected by the EN input. The LDO output is used to power and protect circuitry such as USB transceivers from transients on the input supply.

8.3.5 Charge Status Indicator ($\overline{CHG}$)

The bq25071-Q1 contains an open drain $\overline{CHG}$ output that indicates charging state and faults. When charging a battery in precharge or fastcharge mode, the $\overline{CHG}$ output is pulled to GND. Once the BAT output reaches the overcharge voltage threshold, $\overline{CHG}$ goes high impedance to signal the battery is fully charged. When the battery voltage drops below the recharge voltage threshold the $\overline{CHG}$ output is pulled low to signal the host of a new charge cycle. Connect $\overline{CHG}$ to the required logic level voltage through a 1 kΩ to 100 kΩ resistor to use the signal with a microprocessor. $I_{(\overline{CHG})}$ must be below 5 mA.

The IC monitors the CHG pin when no input is connected to verify if the system circuitry is active. If the voltage at CHG is logic being drive low when no input is connected, the TS circuit is turned off for a low quiescent current state. Once the voltage at CHG increases above logic high, the TS circuit is turned on.

8.3.6 Input Current Limit Control (EN)

The bq25071-Q1 contains a 3-state that controls the input current limit. Drive EN low to program the input current limit to the user defined value programmed using ISET. Drive EN high to place the bq25071-Q1 in USB suspend mode. In USB suspend mode, the input current into bq25071-Q1 is reduced. Leaving EN unconnected or connected to a high impedance source programs the USB500 input current limit.

Table 1. EN Input Definition

EN	MODE
Low	ISET
Hi-Z	USB500
Hi	USB Suspend

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8.4 Device Functional Modes

8.4.1 Charging Operation

The bq25071-Q1 uses a charge algorithm that is unique to $LiFePO_4$ chemistry cells. The current taper typically seen as part of the constant voltage mode control usually present in Li-Ion battery charge cycles is replaced with a floating regulation voltage with minimal charging current. This dramatically decreases the charge time. When the bq25071-Q1 is enabled by EN, the battery voltage is monitored to verify which stage of charging must be used. When $V_{(BAT)} < V_{(LOWV)}$, the bq25071-Q1 charges in precharge mode; when $V_{(BAT)} > V_{(LOWV)}$, the normal charge cycle is used.

8.4.1.1 Charger Operation with Minimum System Voltage Mode Enabled

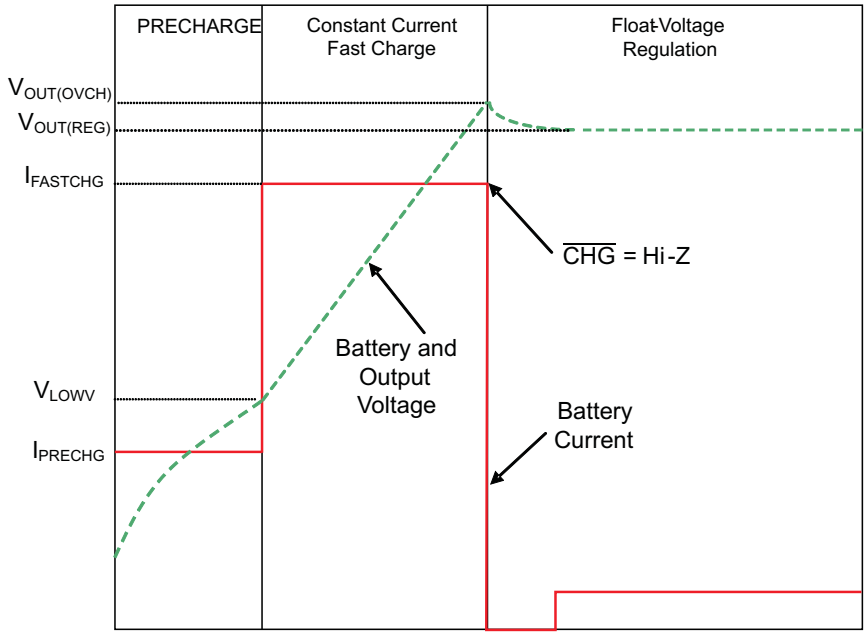


Figure 10. Typical Charging Cycle with Minimum System Voltage Enabled

8.4.1.2 Precharge Mode ($V_{(BAT)} \leq V_{(LOWV)}$)

The bq25071-Q1 enters precharge mode when $V_{BAT} \leq V_{(LOWV)}$. Upon entering precharge mode, the battery is charged with a 47.5 mA current and $\overline{CHG}$ goes low.

8.4.1.3 Fast Charge Mode

Once $V_{(BAT)} > V_{(LOWV)}$, the bq25071-Q1 enters constant current (CC) mode where charge current is regulated using the internal MOSFETs between IN and OUT. The total current is shared between the output load and the battery. Once the battery voltage charges up to $V_{BAT(OVCH)}$, the $\overline{CHG}$ output goes high indicating the charge cycle is complete and the bq25071-Q1 switches the battery regulation voltage to $V_{BAT(REG)}$. The battery voltage is allowed to relax down to $V_{BAT(REG)}$. The charger remains enabled and regulates the output to $V_{BAT(REG)}$. If at any time the battery falls below $V_{(RCH)}$, the charge cycle restarts.

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Device Functional Modes (continued)

8.4.2 Programmable Input Current Limit (ISET)

When the charger is enabled, and the user programmable current limit is selected by the EN input, internal circuits generate a current proportional to the input current at the ISET input. The current out of ISET is 1/1000 (±10%) of the charge current. This current, when applied to the external charge current programming resistor, R1 (Figure 11), generates an analog voltage that is regulated to program the fast charge current. Connect a resistor from ISET to GND to program the input current limit using the following equation:

$$I_{(IN_LIM)} = \frac{K_{(ISET)}}{R_{(ISET)}} = \frac{1000A \times \Omega}{R_{(ISET)}} \quad (3)$$

$I_{(IN_LIM)}$ is programmable from 100 mA to 1 A. The voltage at ISET can be monitored by an external host to calculate the charging current to the battery. The input current is related to the ISET voltage using the following equation:

$$I_{IN} = V_{(ISET)} \times \frac{1000}{R_{(ISET)}} \quad (4)$$

Monitoring the ISET voltage allows for the host to calculate the actual charging current and therefore perform more accurate termination. The input current to the system must be monitored and subtracted from the current into the bq25071-Q1 which is show by $V_{(ISET)}$.

8.4.3 Sleep Mode

If the IN pin voltage is between $V_{(UVLO)}$ and $V_{(BAT)}$+ $V_{IN(SLP)}$, the charge current is disabled, the safety timer counting stops (not reset) and the $\overline{CHG}$ pin is high impedance. As the input voltage rises and the charger exits sleep mode, the safety timer continues to count, charge is enabled and the $\overline{CHG}$ pin returns to its previous state.

8.4.4 Thermal Regulation and Thermal Shutdown

The bq25071-Q1 contains a thermal regulation loop that monitors the die temperature continuously. If the temperature exceeds $T_{J(REG)}$, the device automatically reduces the charging current to prevent the die temperature from increasing further. In some cases, the die temperature continues to rise despite the operation of the thermal loop, particularly under high V_{IN} conditions. If the die temperature increases to $T_{J(OFF)}$, the IC is turned off. Once the device die temperature cools by $T_{J(OFF-HYS)}$, the device turns on and returns to thermal regulation. Continuous overtemperature conditions result in the pulsing of the load current. If the junction temperature of the device exceeds $T_{J(OFF)}$, the charge FET is turned off. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} - T_{J(OFF-HYS)}$.

Note that these features monitor the die temperature of the bq25071-Q1. This is not synonymous with ambient temperature. Self heating exists due to the power dissipated in the IC because of the linear nature of the battery charging algorithm.

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9 Application and Implementation

NOTE

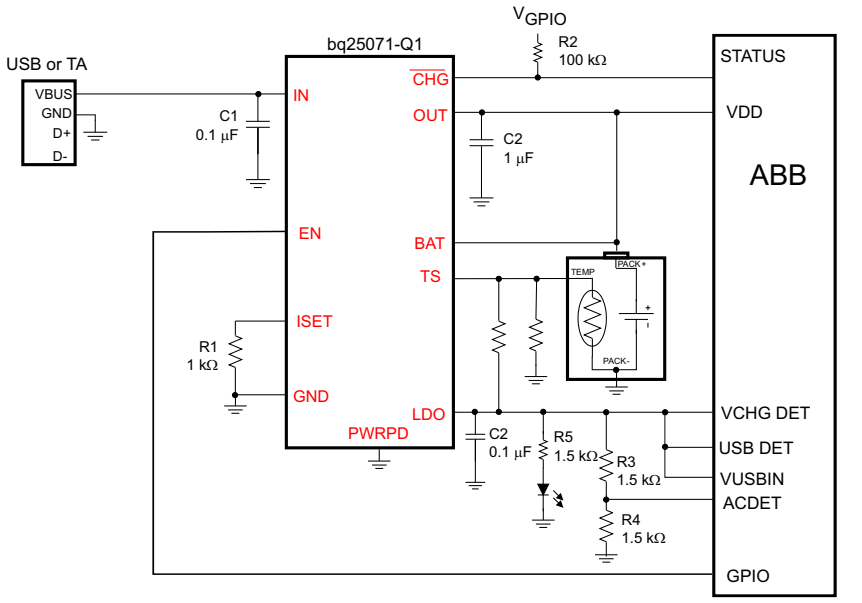
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The typical application circuit uses a single output which charges the battery and powers the system. Additionally a 50-mA LDO can supply a low power external circuit.

The bq25071EVM-658 evaluation module (EVM) is a complete charger module for evaluating the bq25071-Q1. Refer to SLUUB49.

9.2 Typical Application



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Figure 11. bq25071-Q1 Typical Application Circuit

9.2.1 Design Requirements

Table 2. Design Parameters

PARAMETER	EXAMPLE VALUE
Input supply range	5 V ±5%
Output voltage range	3.5 V
Output current rating	1000 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Selection of Input and Output Capacitors

In most applications, all that is needed is a high-frequency decoupling capacitor on the input power pin. For normal charging applications, a 0.1 µF ceramic capacitor, placed in close proximity to the IN pin and GND pad works best. In some applications, depending on the power supply characteristics and cable length, it may be necessary to increase the input filter capacitor to avoid exceeding the OVP voltage threshold during adapter hot plug events where the ringing exceeds the deglitch time.

The charger in the bq25071-Q1 requires a capacitor from OUT to GND for loop stability. Connect a 1 µF ceramic capacitor from OUT to GND close to the pins for best results. More output capacitance may be required to minimize the output drop during large load transients.

The LDO also requires an output capacitor for loop stability. Connect a 0.1 µF ceramic capacitor from LDO to GND close to the pins. For improved transient response, this capacitor may be increased.

9.2.2.2 Thermal Considerations

The bq25071-Q1 is packaged in a thermally enhanced QFN package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note* (SLUA271).

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

Where:

$$\theta_{JA} = \frac{T_J - T_A}{P_D} \quad (5)$$

T_J = chip junction temperature
T_A = ambient temperature
P_D = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

The device power dissipation, P_D, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Due to the charge profile of $LiFePO_4$ batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. See the charging profile, Figure 10. If the board thermal design is not adequate the programmed fast charge rate current may not be achieved under maximum input voltage and minimum battery voltage, as the thermal loop can be active, effectively reducing the charge current to avoid excessive IC junction temperature.

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9.2.3 Application Curves

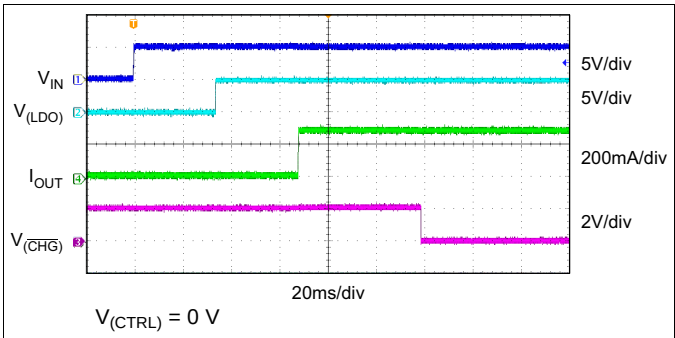


Figure 12. Adapter Plug-In With Battery Connected

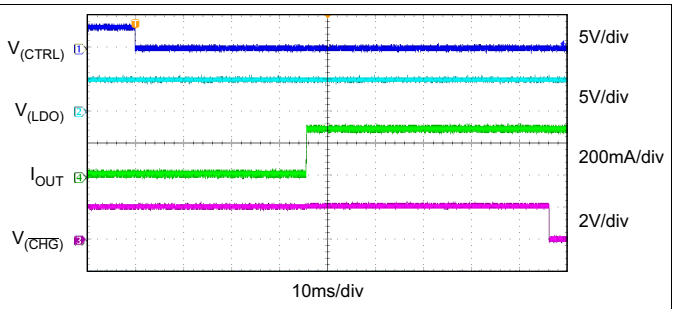


Figure 13. Charger Enable Using EN

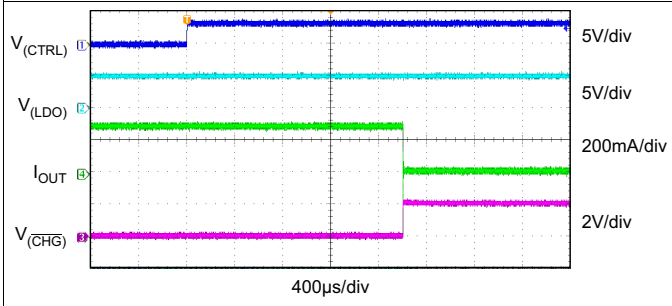


Figure 14. Charger Disable Using EN

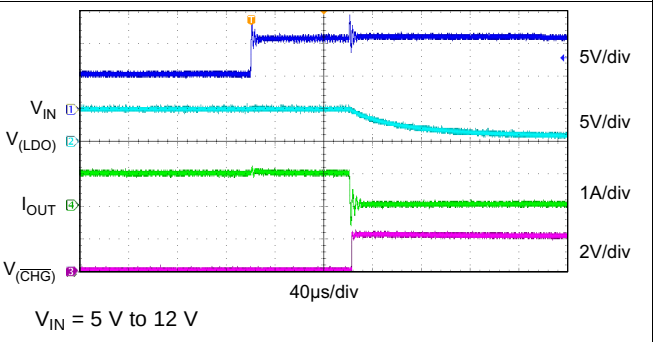
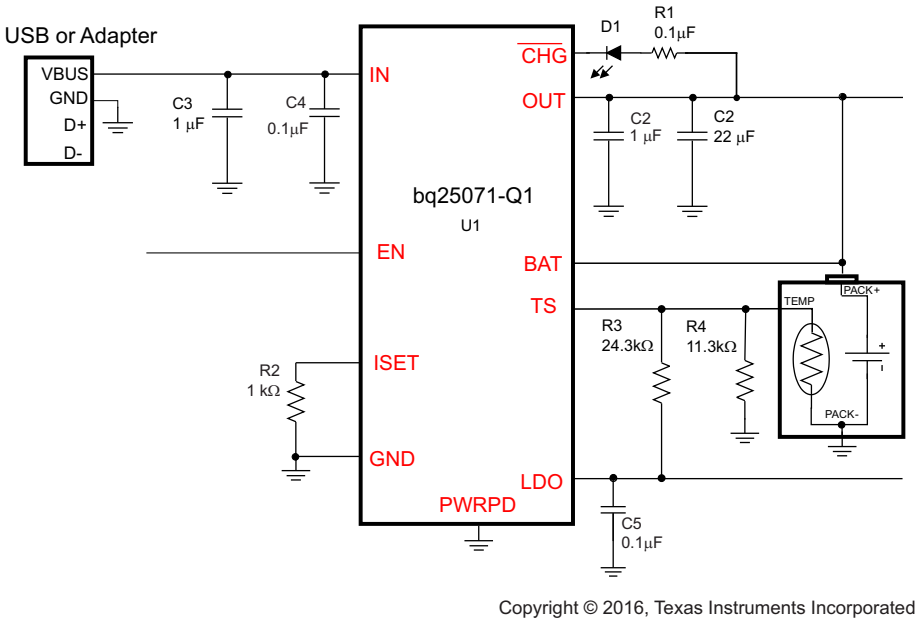


Figure 15. OVP Fault

9.3 System Examples



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Figure 16. Schematic

10 Power Supply Recommendations

In a typical application, the system is powered by a USB port or USB wall adapter.

The wide input voltage range supports low cost and unregulated adapters.

The minimum input voltage - where the charging process starts with a reduced charging current - could be 3.75 V when the battery voltage is below 3.5 V. The minimum input voltage can be up to 3.875 V when the battery is close to be fully charged (Please refer to the Sleep Mode) or there is no battery presented. The maximum recommended operating input voltage is up to 8 V; the overvoltage protection kicks in at 10.5 V and the maximum input voltage rating is 30 V Input Rating.

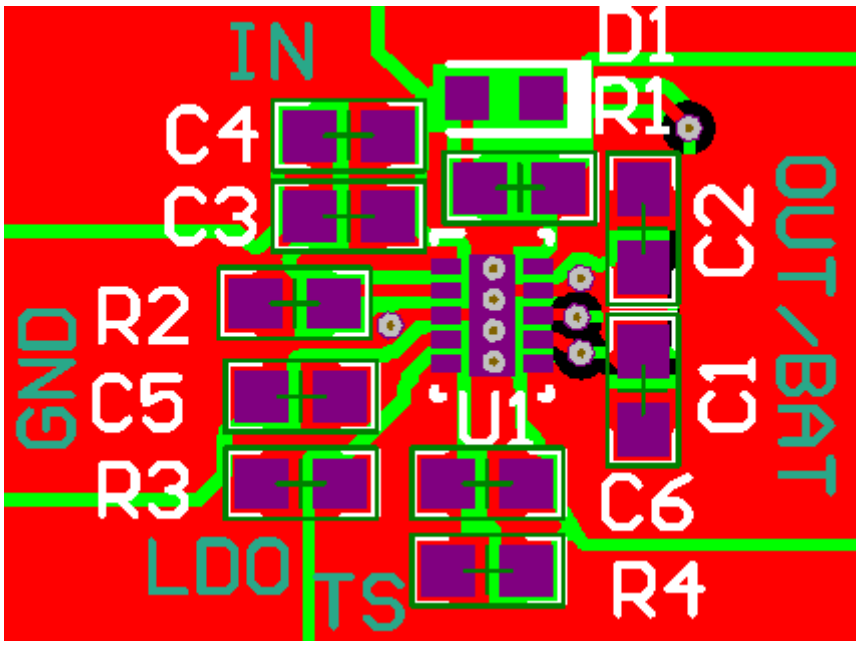
11 Layout

11.1 Layout Guidelines

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the bq25071-Q1, with short trace runs to both IN, OUT and GND (thermal pad).
- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The bq25071-Q1 is packaged in a thermally enhanced SON package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note* (SLUA271).

11.2 Layout Example



The bottom plane is a ground plane that is connected to the top through vias.

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12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

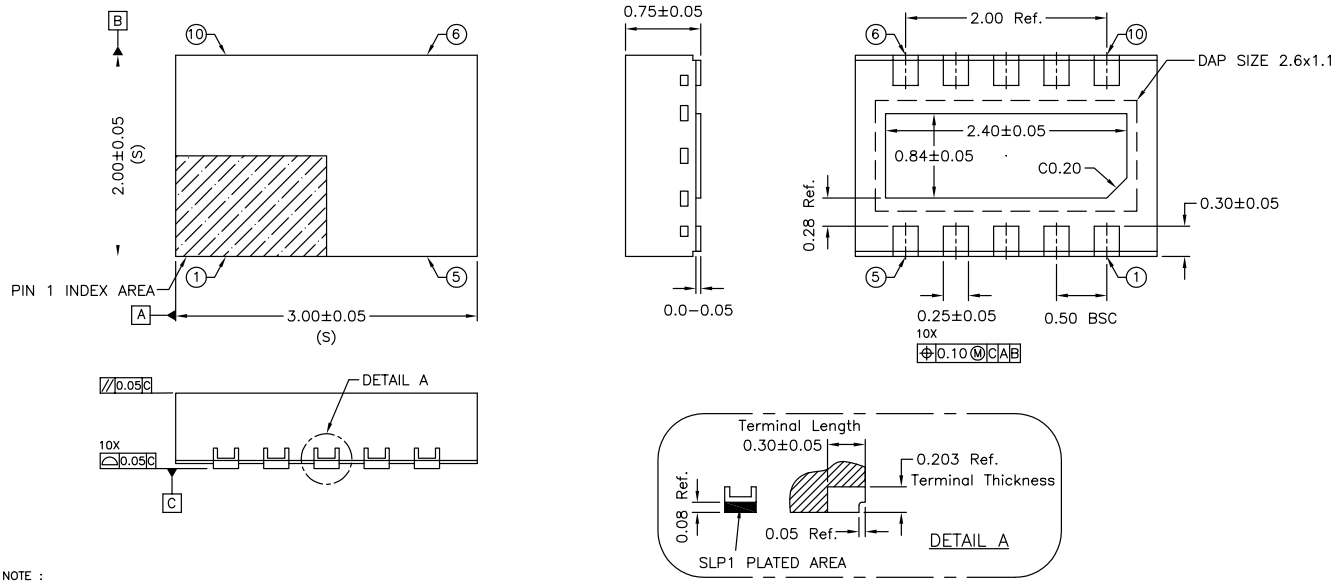
12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



NOTE :

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.05 mm.
3. WARPAGE SHALL NOT EXCEED 0.05 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)
5. REFER JEDEC MO–229.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25071QWDQCRQ1	ACTIVE	WSON	DQC	10	3000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	11V	Samples
BQ25071QWDQCTQ1	ACTIVE	WSON	DQC	10	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	11V	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF BQ25071-Q1 :

- Catalog: BQ25071

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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