

钍地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65HVD78DGK

SN65HVD7x 3.3V power RS-485 with IEC ESD protection

网址 www.sztdbdt.com

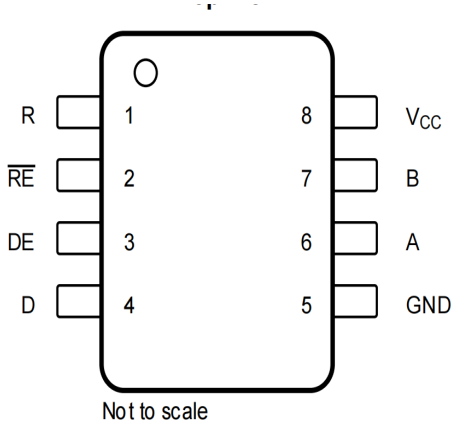
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semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

● Available in small-size VSSOP and SOIC packages, the former saves PCB space, while the latter provides universal compatibility
Bus I/O protection
– >±15kV Human Body Model (HBM) protection
– >±12kV IEC 61000-42 contact discharge
– >±4kV IEC 61000-4-4 fast transient burst
● Extended industrial temperature range
-40 ° C to125 ° C
●Larger receiver hysteresis (80mV) for noise suppression
● Low unit load enables connections of over 200 nodes
●Low power consumption
– Low standby supply current: <2μA
– ICC static current during operation <1mA
●5V tolerant logic inputs compatible with 3.3V or5V controllers
●Optimized for the following signal transmission rates: 250kbps, 20Mbps, 50Mbps
●Glitch-free powerup and power-down bus inputs and outputs



Not to scale

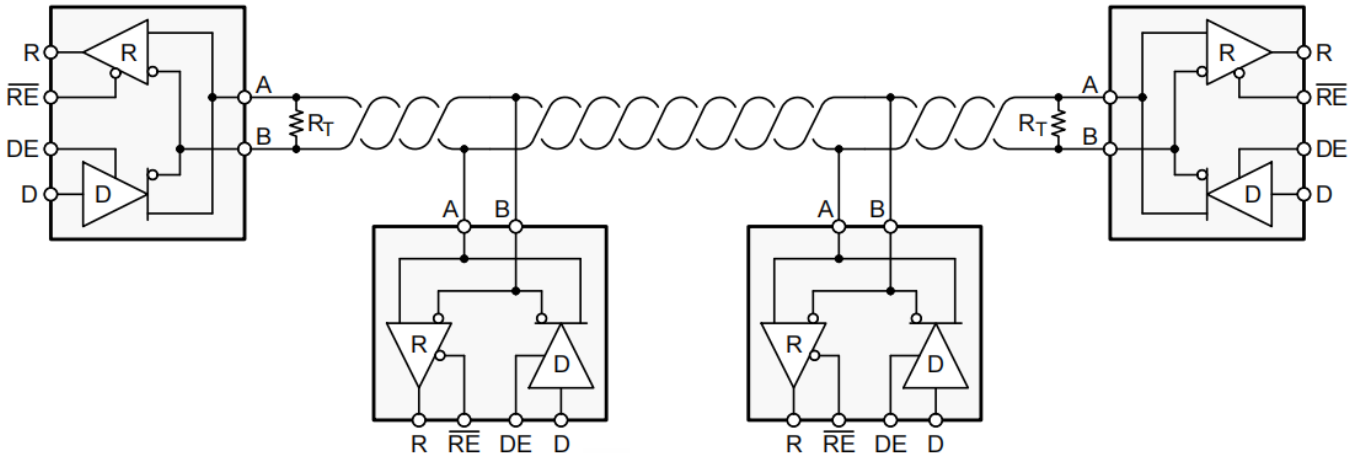
Applications

●Factory automation
●Telecommunications infrastructure
●Motion control

Description

These devices feature robust and durable 3.3V drivers and receivers, and are available in small packages to meet industrial applications. These pins are ESD-tolerant, providing high-level protection against Human Body Model and IEC Contact Discharge specifications.
Each device is equipped with a differential driver and a differential receiver. These two are powered by a 3.3V single supply. The driver's differential output and the receiver's differential input are internally connected to form a bus port suitable for halfduplex (two-wire bus) communication. These devices have a wide common-mode voltage range, making them suitable for long-cable applications. These devices have a rated operating range of -40 ° C to 125 ° C.

典型应用图



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
A	6	Bus I/O	Driver output or receiver input (complementary to B)
B	7	Bus I/O	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Active-high driver enable
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Active-low receiver enable
V_{CC}	8	Supply	3-V to 3.6-V supply

7 Specifications

7.1 Absolute Maximum Ratings

over recommended operating range (unless otherwise specified) (1)

	MIN	MAX	UNIT
Supply voltage, V_{CC}	–0.5	5	V
Voltage at A or B inputs	–13	16.5	
Voltage at D, DE, or $\overline{RE}$	–0.3	5.7	
Voltage input, transient pulse, A and B, through 100 Ω	–100	100	
Receiver output current	–24	24	mA
Junction temperature, T_J		170	°C
Continuous total power dissipation	See *Power Dissipation*		
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002, all pins (2)	±1500	
		JEDEC Standard 22, Test Method A115 (Machine Model), all pins	±300	
		IEC 61000-4-2 ESD (Air-Gap Discharge), bus pins and GND (3)	±12000	
		IEC 61000-4-2 ESD (Contact Discharge), bus pins and GND	±12000	
		IEC 61000-4-4 EFT (Fast transient or burst) bus pins and GND	±4000	
		IEC 60749-26 ESD (Human Body Model), bus pins and GND	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) By inference from contact discharge results, see *Application and Implementation*.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC} (1)	Supply voltage		3	3.3	3.6	V
V_I	Input voltage at any bus terminal (separately or common mode) (2)		–7		12	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)		0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_O	Output current, driver		–60		60	mA
I_O	Output current, receiver		–8		8	mA
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
$1/t_{UI}$	Signaling rate	SN65HVD72			250	kbps
		SN65HVD75			20	Mbps
		SN65HVD78			50	Mbps
T_A (3)	Operating free-air temperature (See *Thermal Information*)		–40		125	°C
T_J	Junction temperature		–40		150	°C

(1) Exposure to conditions beyond the recommended operation maximum for extended periods may affect device reliability.
(2) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.
(3) Operation is specified for internal (junction) temperatures up to 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shutdown (TSD) circuit which disables the driver outputs when the junction temperature reaches 170°C.

7.4 Thermal Information

THERMAL METRIC(1)		SN65HVD72, SN65HVD75, SN65HVD78			UNIT
		D (SOIC)	DGK (VSSOP)	DRB (VSON)	
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.7	168.7	40	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.7	62.2	49.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	3.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.3	89.5	15.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.2	7.4	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.7	87.9	15.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over recommended operating range (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OD}\rvert$	Driver differential output voltage magnitude	R_L = 60 Ω, 375 Ω on each output to –7 V to 12 V	See Figure 10	1.5	2		V
		R_L = 54 Ω (RS-485)	See Figure 11	1.5	2		
		R_L = 100 Ω (RS-422), $T_J \geq 0°C$ $V_{CC} \geq 3.2$ V		2	2.5		
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of driver differential output voltage	R_L = 54 Ω, C_L = 50 pF		–50	0	50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	Center of two 27-Ω load resistors		1	$V_{CC}/2$	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage	Center of two 27-Ω load resistors		–50	0	50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors			200		mV
C_{OD}	Differential output capacitance				15		pF
V_{IT+}	Positive-going receiver differential input voltage threshold			See (1)	–70	–20	mV
V_{IT-}	Negative-going receiver differential input voltage threshold			–200	–150	See (1)	mV
V_{HYS}	Receiver differential input voltage threshold hysteresis ($V_{IT+} - V_{IT-}$)			50	80		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA		2.4	V_{CC} – 0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA			0.2	0.4	V
I_I	Driver input, driver enable, and receiver enable input current			–2		2	µA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}		–1		1	µA
I_{OS}	Driver short-circuit output current			–160		160	mA

Electrical Characteristics (continued)

over recommended operating range (unless otherwise specified)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_I	Bus input current (disabled driver)	V_{CC} = 3 to 3.6 V or V_{CC} = 0 V DE at 0 V	SN65HVD72 SN65HVD75	V_I = 12 V		75	150	µA
				V_I = –7 V	–100	–40		
			SN65HVD78	V_I = 12 V		240	333	
				V_I = –7 V	–267	–180		
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V_{CC}, $\overline{RE}$ = GND No load			750	950	µA
		Driver enabled, receiver disabled	DE = V_{CC}, $\overline{RE}$ = V_{CC} No load			300	500	
		Driver disabled, receiver enabled	DE = GND, $\overline{RE}$ = GND No load			600	800	
		Driver and receiver disabled	DE = GND, D = open $\overline{RE}$ = V_{CC}, No load			0.1	2	
	Supply current (dynamic)	See *Typical Characteristics*						
T_{TSD}	Thermal shutdown junction temperature					170		°C

7.6 Power Dissipation

PARAMETER			TEST CONDITIONS		VALUE	UNIT
PD	Power Dissipation driver and receiver enabled, V_{CC} = 3.6 V, T_J = 150°C 50% duty cycle square-wave signal at signaling rate: • SN65HVD72 at 250 kbps • SN65HVD75 at 20 Mbps • SN65HVD78 at 50 Mbps	Unterminated	R_L = 300 Ω C_L = 50 pF (driver)	SN65HVD72	120	mW
				SN65HVD75	160	
				SN65HVD78	200	
		RS-422 load	R_L = 100 Ω C_L = 50 pF (driver)	SN65HVD72	155	mW
				SN65HVD75	195	
				SN65HVD78	230	
		RS-485 load	R_L = 54 Ω C_L = 50 pF (driver)	SN65HVD72	190	mW
				SN65HVD75	230	
				SN65HVD78	260	

7.7 Switching Characteristics: 250 kbps Device (SN65HVD72) Bit Time ≥ 4 µs

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise or fall time	R_L = 54 Ω C_L = 50 pF	See Figure 12	0.3	0.7	1.2	µs
t_{PHL}, t_{PLH}	Driver propagation delay				0.7	1	µs
$t_{SK(P)}$	Driver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					0.2	µs
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 13 and Figure 14		0.1	0.4	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			0.5	1	µs
		Receiver disabled			3	9	
RECEIVER							
t_r, t_f	Receiver output rise or fall time	C_L = 15 pF	See Figure 15		12	30	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				75	100	ns
$t_{SK(P)}$	Receiver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$				3	15	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				40	100	ns
$t_{PZL(1)}$, $t_{PZH(1)}$, $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled	See Figure 16		20	50	ns
		Driver disabled	See Figure 17		3	8	µs

7.8 Switching Characteristics: 20 Mbps Device (SN65HVD75) Bit Time ≥50 ns

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise or fall time	R_L = 54 Ω, C_L = 50 pF	See Figure 12	2	7	14	ns
t_{PHL}, t_{PLH}	Driver propagation delay			7	11	17	ns
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$				0	2	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 13 and Figure 14		12	50	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			10	20	ns
		Receiver disabled			3	7	µs
RECEIVER							
t_r, t_f	Receiver output rise or fall time	C_L = 15 pF	See Figure 15		5	10	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				60	70	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$				0	6	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				15	30	ns
$t_{pZL(1)}$, $t_{PZH(1)}$, $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled	See Figure 16		10	50	ns
		Driver disabled	See Figure 17		3	8	µs

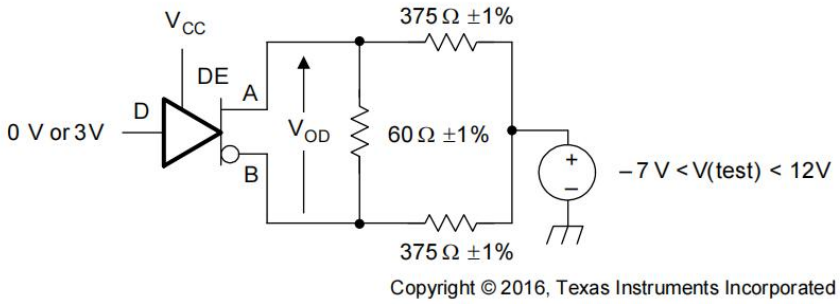
7.9 Switching Characteristics: 50 Mbps Device (SN65HVD78) Bit Time ≥20 ns

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise or fall time	R_L = 54 Ω, C_L = 50 pF	See Figure 12	1	3	6	ns
t_{PHL}, t_{PLH}	Driver propagation delay				9	15	ns
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$				0	1	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 13 and Figure 14		10	30	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			10	30	ns
		Receiver disabled				8	µs
RECEIVER							
t_r, t_f	Receiver output rise or fall time	C_L = 15 pF	See Figure 15	1	3	6	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time					35	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$					2.5	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				8	30	ns
$t_{pZL(1)}$, $t_{PZH(1)}$, $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled	See Figure 16		10	30	ns
		Driver disabled	See Figure 17		3	8	µs

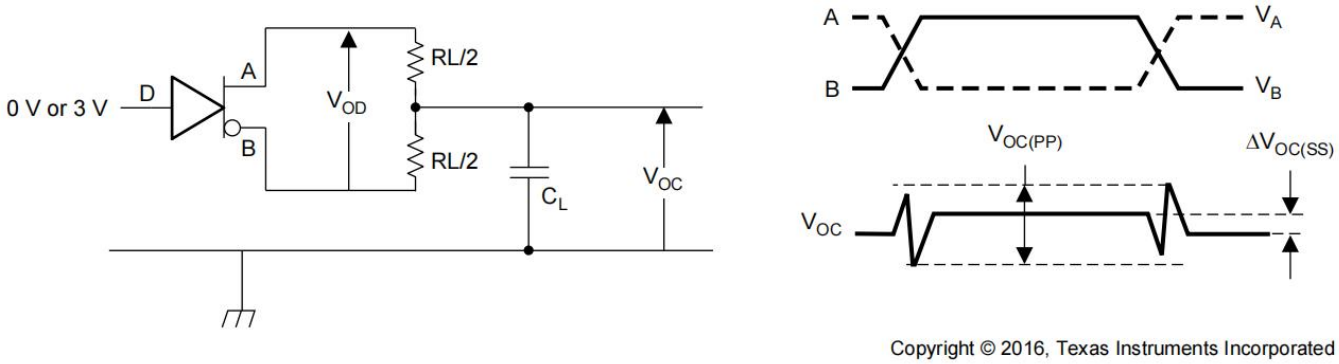
8 Parameter Measurement Information

Input generator rate is 100 kbps, 50% duty cycle, rise or fall time is less than 6 ns, output impedance is 50 Ω.



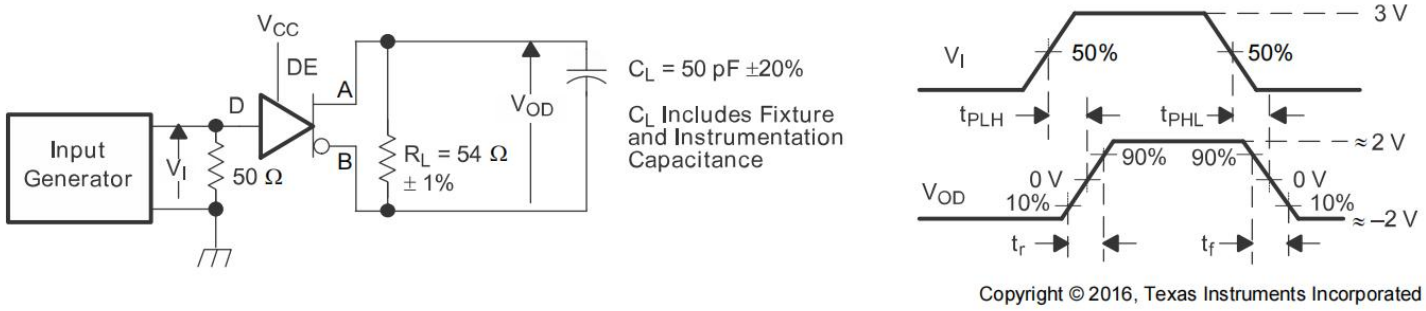
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Figure 10. Measurement of Driver Differential Output Voltage With Common-Mode Load



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Figure 11. Measurement of Driver Differential and Common-Mode Output With RS-485 Load



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Figure 12. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

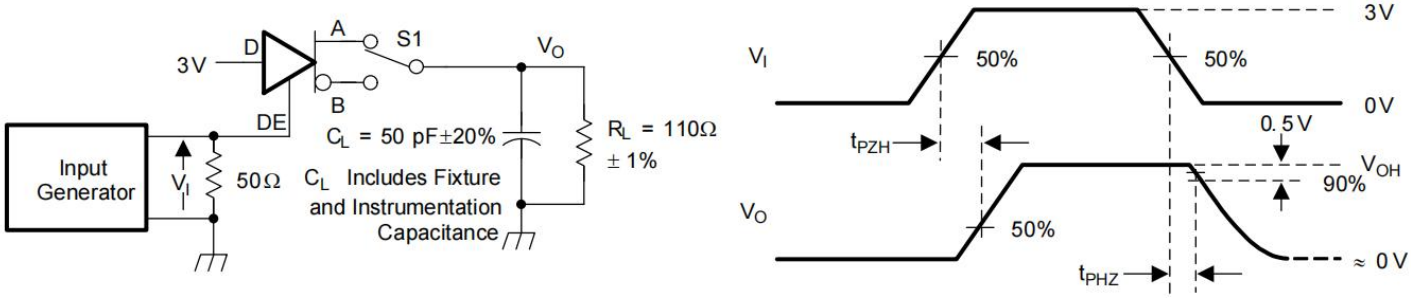
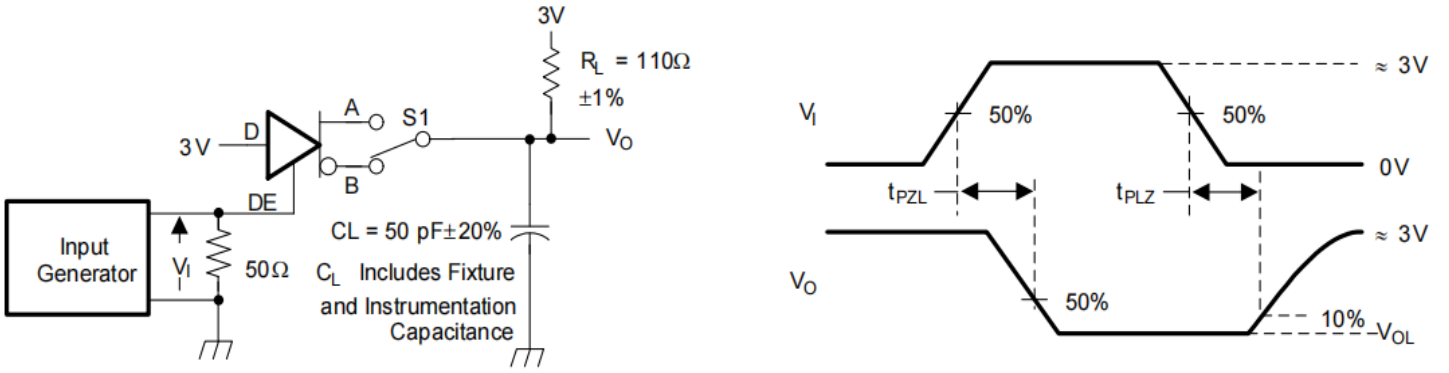


Figure 13. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load

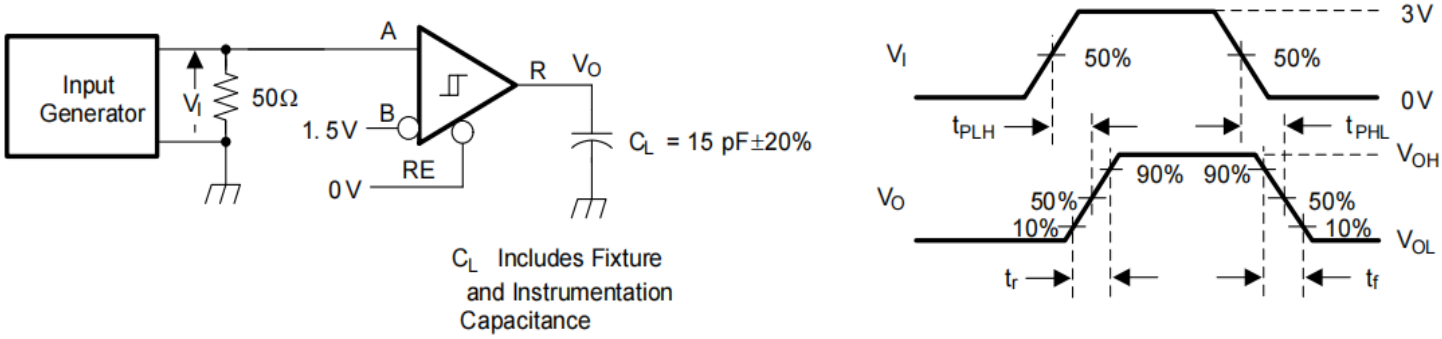
Parameter Measurement Information (continued)



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D at 0 V to test non-inverting output, D at 3 V to test inverting output.

Figure 14. Measurement of Driver Enable and Disable Times With Active Low Output and Pullup Load



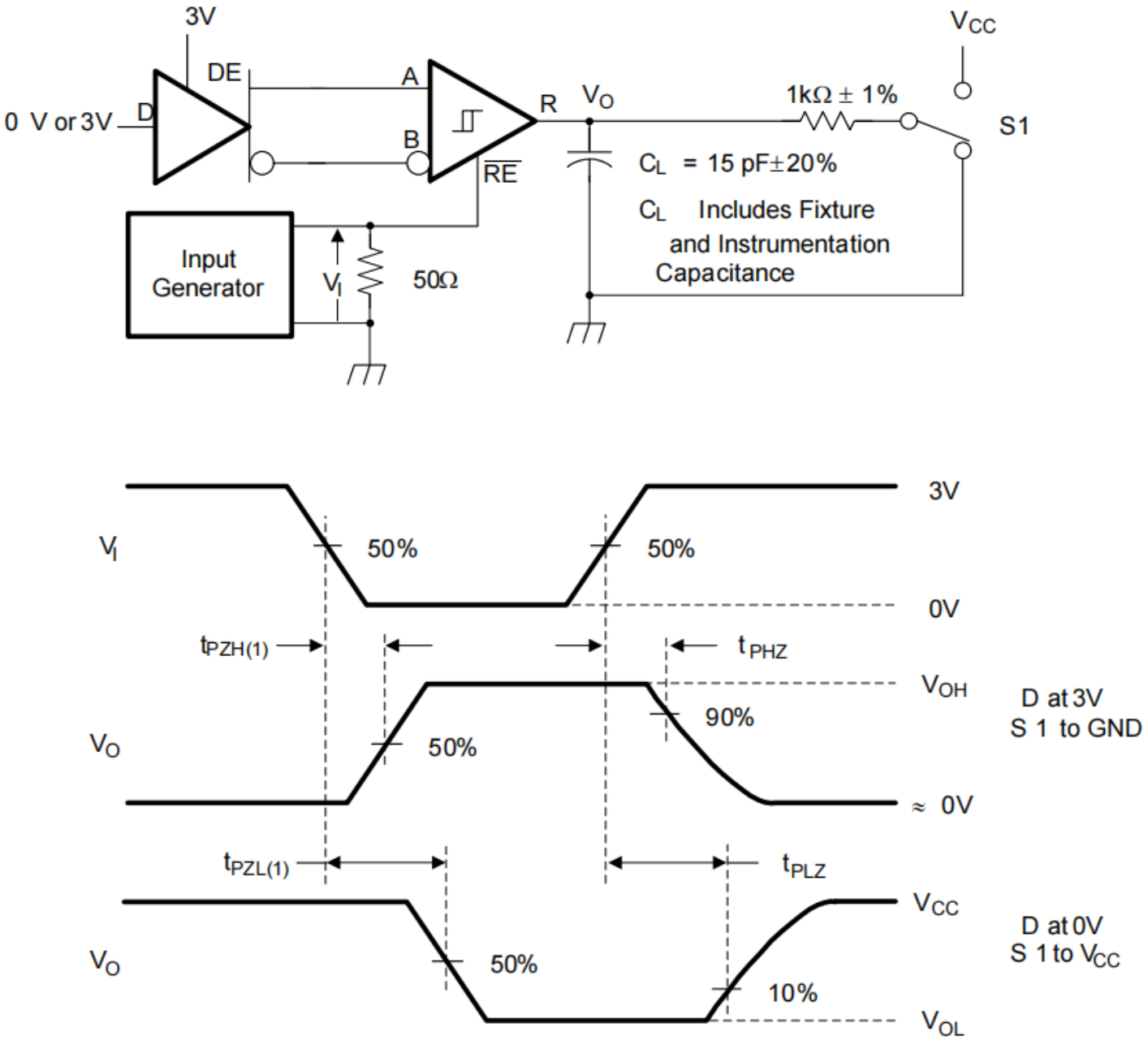


Figure 16. Measurement of Receiver Enable and Disable Times With Driver Enabled

Parameter Measurement Information (continued)

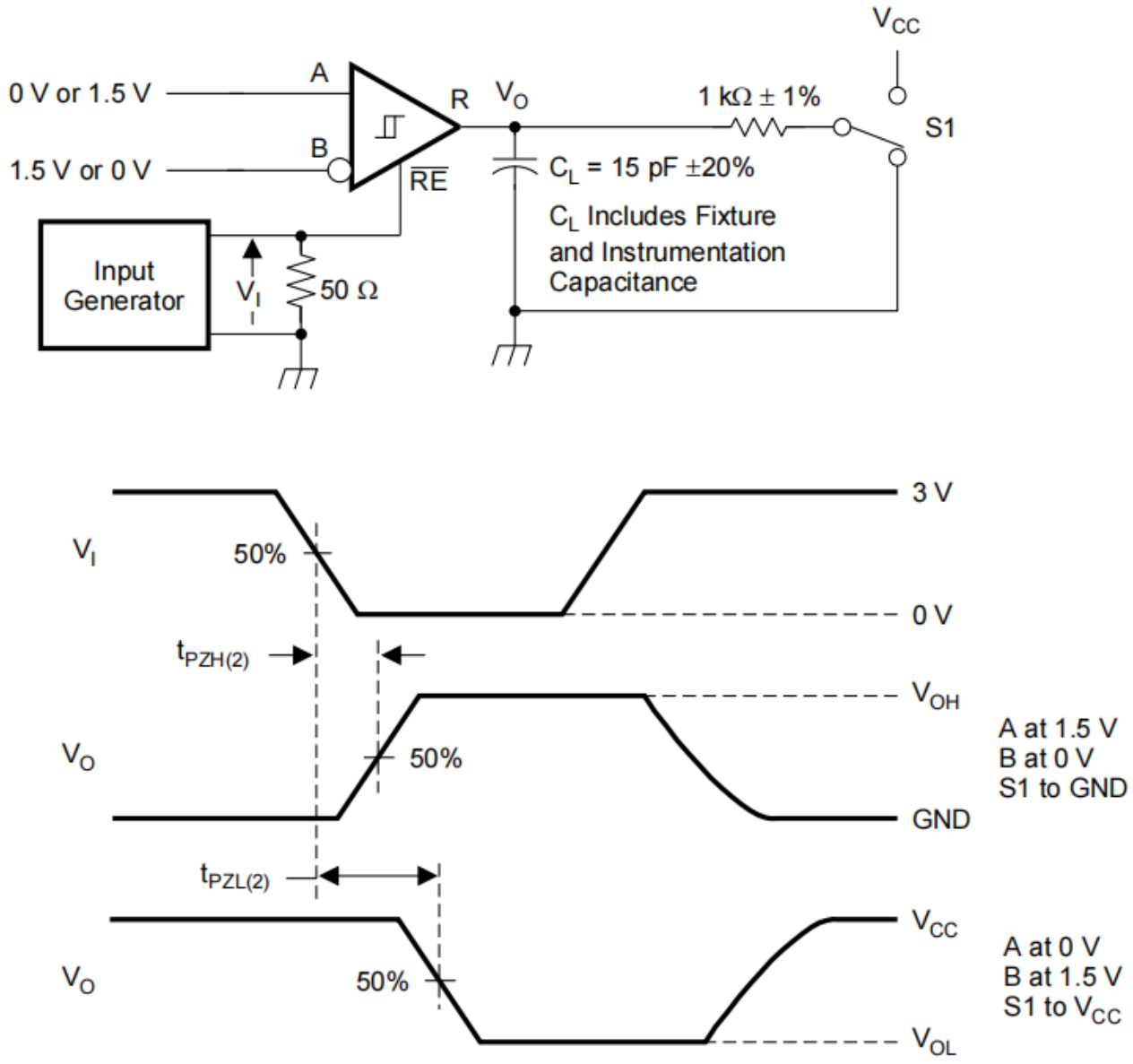


Figure 17. Measurement of Receiver Enable Times With Driver Disabled

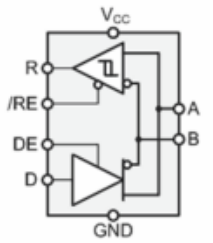
9 Detailed Description

9.1 Overview

The SN65HVD72, SN65HVD75, and SN65HVD78 are low-power, half-duplex RS-485 transceivers available in 3 speed grades suitable for data transmission up to 250 kbps, 20 Mbps, and 50 Mbps.

These devices have active-high driver enables and active-low receiver enables. A standby current of less than 2 µA can be achieved by disabling both driver and receiver.

9.2 Functional Block Diagram



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9.3 Feature Description

Internal ESD protection circuits protect the transceiver against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to ±12 kV, and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4 kV.

The SN65HVD7x half-duplex family provides internal biasing of the receiver input thresholds in combination with large input threshold hysteresis. At a positive input threshold of V_{IT+} = –20 mV and an input hysteresis of V_{HYS} = 50 mV, the receiver output remains logic high under a bus-idle or bus-short condition even in the presence of 140-mV_{PP} differential noise without the need for external failsafe biasing resistors.

Device operation is specified over a wide ambient temperature range from –40°C to 125°C.

9.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground; thus, when left open, the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC}; thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 1. Driver Function Table

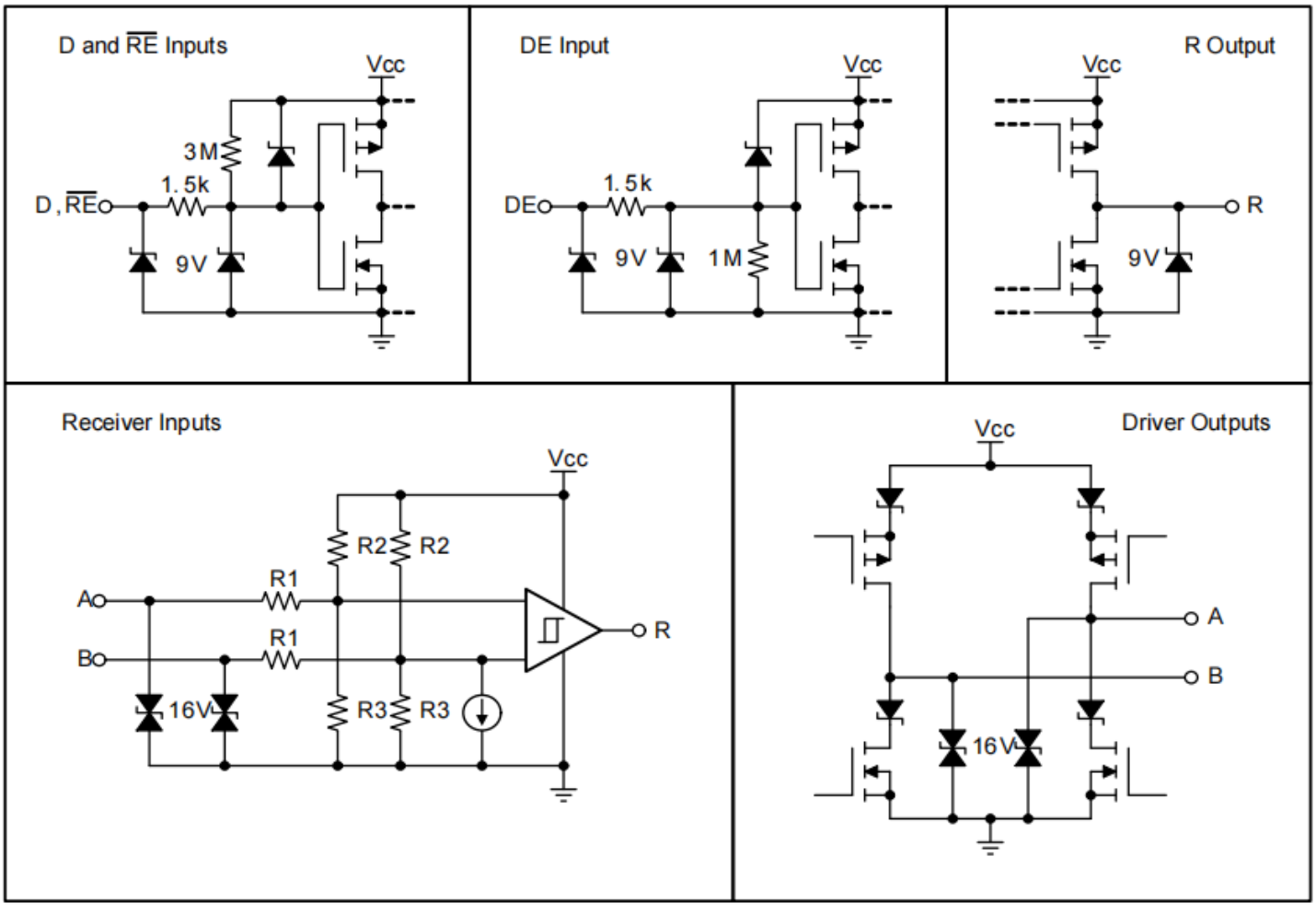
INPUT	ENABLE	OUTPUTS		DESCRIPTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, RE, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-}, the receiver output turns low. If V_{ID} is between V_{IT+} and V_{IT-}, the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Table 2. Receiver Function Table

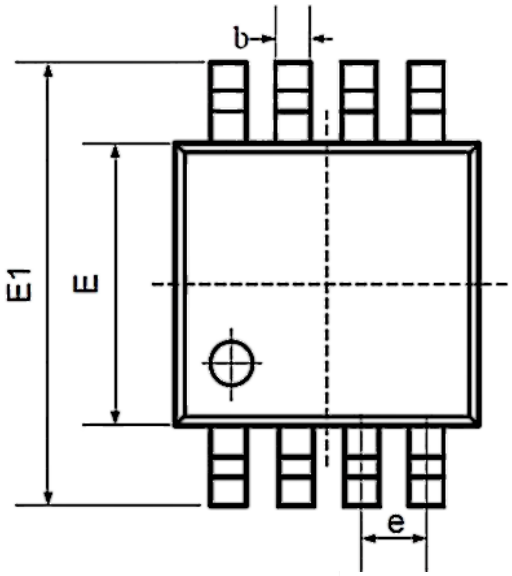
DIFFERENTIAL INPUT	ENABLE	OUTPUT	DESCRIPTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus high
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Failsafe high output
Short-circuit bus	L	H	Failsafe high output
Idle (terminated) bus	L	H	Failsafe high output

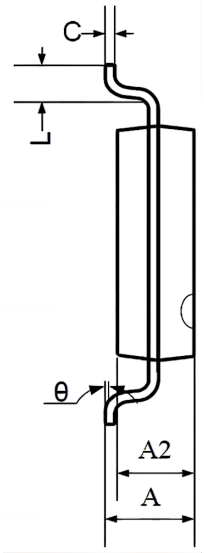


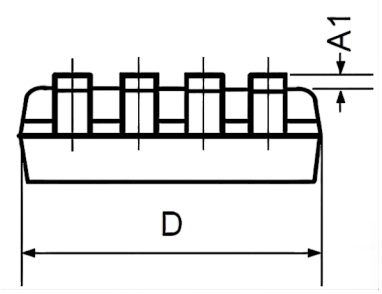
Order information

Order Number	Package	Package Quantity	Marking On The park
SN65HVD78DGK-TUDI	MSOP8	Tape,Reel,2500	SN65HVD78DGK

Package MSOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026 TYP	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

Important statement:

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